

## POWER SUPPLY REJECTION FOR LOW-JITTER CLOCKS

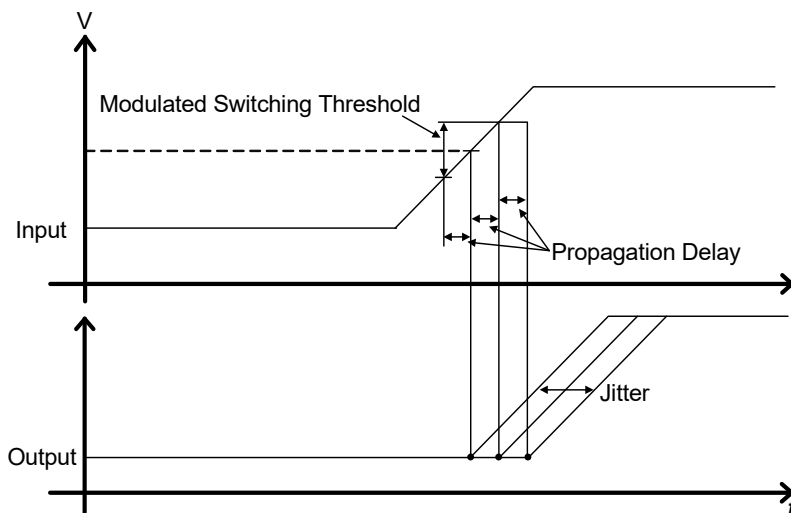
### 1. Introduction

Hardware designers are routinely challenged to increase functional density while shrinking the overall PCB footprint of each new design. One significant challenge is minimizing clock jitter through careful board design while meeting the design's functional and space requirements. Since jitter is a measure of signal fidelity, it requires an understanding of diverse analog concepts, such as transmission line theory, interference, bandwidth, and noise, in order to manage their impact on performance. Among these, density impacts sensitivity to external noise and interference the most. Since noise and interference are everywhere and since multiple components share a common power supply, the power supply is a direct path for noise and interference to impact the jitter performance of each device. Therefore, achieving the lowest clocking jitter requires careful management of the power supply.

Sensitivity to power supply is commonly referred to as power supply ripple rejection or power supply rejection ratio (PSRR). For jitter, ripple rejection is more appropriate.

### 2. Impact

The effect of power supply ripple on jitter is quite straightforward. Power supply influences the propagation delay by affecting both the switching voltage threshold of logic gates as well as the output resistance. As the switching voltage threshold is modulated, the time at which the output transitions is modulated because the input signal has a finite slope as shown in Figure 1.



**Figure 1. Changing Thresholds Due to Power Supply Noise**

Varying output resistance affects the propagation delay of the CMOS gate through the parasitic RC filter. When combined, these two effects change the propagation delay through the CMOS gate. The effect is amplified as more gates are placed in series.

The degree of the impact is highly dependent on the "speed" of the transistors involved. By having a faster slope at the CMOS gate input, the impact from a changing threshold can be minimized. In addition, faster circuits require that capacitance be minimized in order to achieve small propagation delays; so, the delay variation due to supply variations can be minimized by making the routing capacitance as small as possible. However, there are trade-offs; the downside to faster circuits is power consumption. To make a faster edge, more current is required to charge the capacitors given a constant voltage.

## 3. Overcoming Supply Sensitivities

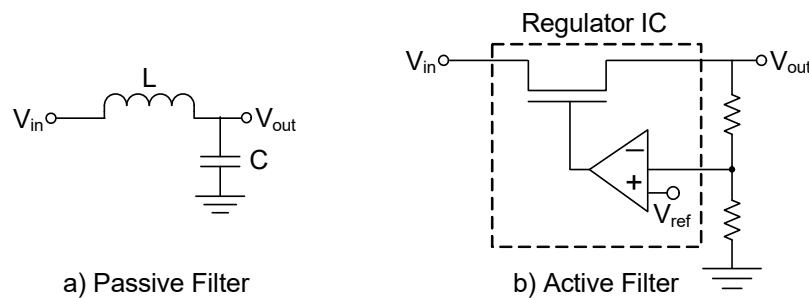
Common methods used to reduce supply sensitivity are supply filtering and minimizing circuit sensitivities.

### 3.1. Filtering

Power supply ripple rejection is often managed for an integrated circuit using both external and internal methods. Externally, board designers use active and passive filters to attenuate ripple and differential interfaces to reject common-mode ripple. Internally, architecture choices, linear regulators, and differential circuits are used to reduce circuit sensitivities to the power supply.

Direct filtering of the power supply can be achieved using passive filters or linear regulators. A common external filter solution relies upon a ferrite bead and discrete surface-mount ceramic capacitors (see Figure 2a).

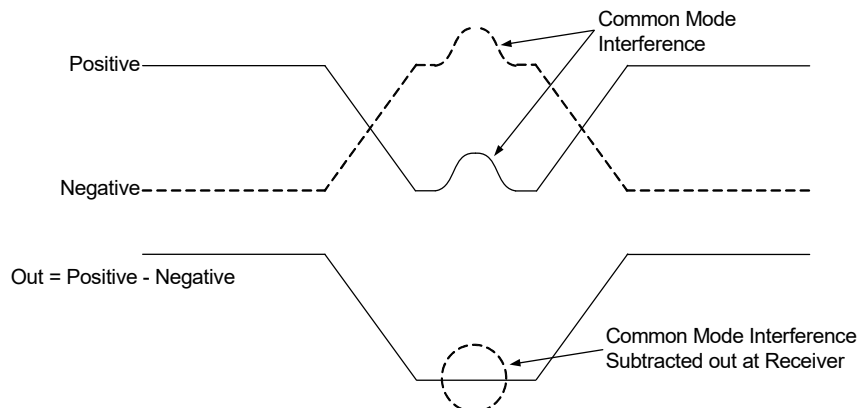
With this approach, series resistance must be minimized to avoid reducing the supply voltage at the IC. Unfortunately, the filtering is highly dependent on the series impedance (resistance plus reactance); so, ensure that the ferrite bead can handle the device current. Linear regulators can also filter supply noise by using the regulator as a high-pass filter (see Figure 2b). Often, these techniques are combined to provide filtering across the entire band of concern.



**Figure 2. Typical Supply Filter Topologies**

Depending on the level of performance desired and the cost targets associated with a given design, one should consider the cost and power trade-offs associated with external filtering. Ferrite beads are much less expensive than active regulators and waste almost no power, but they cannot achieve the same level of filtering at low frequencies as that achieved by regulators. Consequently, pre-design evaluation of timing hardware should include power supply ripple rejection testing.

Differential circuits help reject power supply noise by allowing the supply interference to occur in the common mode and eliminating the interference by subtracting the common-mode signal. As the positive and negative legs are degraded by supply ripple, they accumulate the noise in common, as shown in Figure 3.



**Figure 3. Differential Signalling Helps Eliminate Interference**

By subtracting these signals, the supply noise is rejected. A concern here is the receiver's ability to reject common-mode noise. This is referred to as common-mode ripple rejection (CMRR). Just as in the CMOS gate, fast rise/fall times help.

External filtering may be necessary for designs that do not support differential signaling. Many timing devices with CMOS/TTL interfaces fail to account for power supply ripple. System designers should verify ripple rejection on the bench.

## 3.2. Circuit Choices

Architectural choices also play a role in ensuring good jitter performance when subjected to power supply ripple. Timing devices often rely on phase-locked loops (PLLs) to perform various functions, such as jitter filtering and frequency multiplication. One of the primary challenges in PLL design is associated with its voltage-controlled oscillator (VCO). To meet the frequency requirements for a variety of applications, it is often necessary to have a wide tuning range oscillator, but oscillator jitter is proportional to the noise at its control input (often its most sensitive port). To reduce the jitter, it is necessary to have a low-gain control input, but the lower limit for the gain is set by the range of frequencies required and the frequency impairments of the oscillator (e.g., process variation, temperature, strain, etc.) This gain limitation can be overcome with novel circuit techniques, such as those employed by Skyworks Solutions' DSPLL™ technology. DSPLL utilizes a digitally-controlled, variable-gain oscillator; DSPLL can provide both a large tuning range and low gain, thereby minimizing its sensitivity during operation.

Furthermore, most timing integrated circuits operate from low supply voltages (less than 5 V). As the voltage is reduced with shrinking process geometries, the control port tuning range is limited as well. To achieve all of the output frequencies, the tuning port gain must be increased. Also, as the supply voltage is reduced, the tuning signal amplitude decreases relative to the noise (i.e., reduced SNR). Higher gain and reduced SNR yields poor jitter performance. It is critical to choose timing devices, such as those employing DSPLL™ by Skyworks Solutions, which have solved these problems.

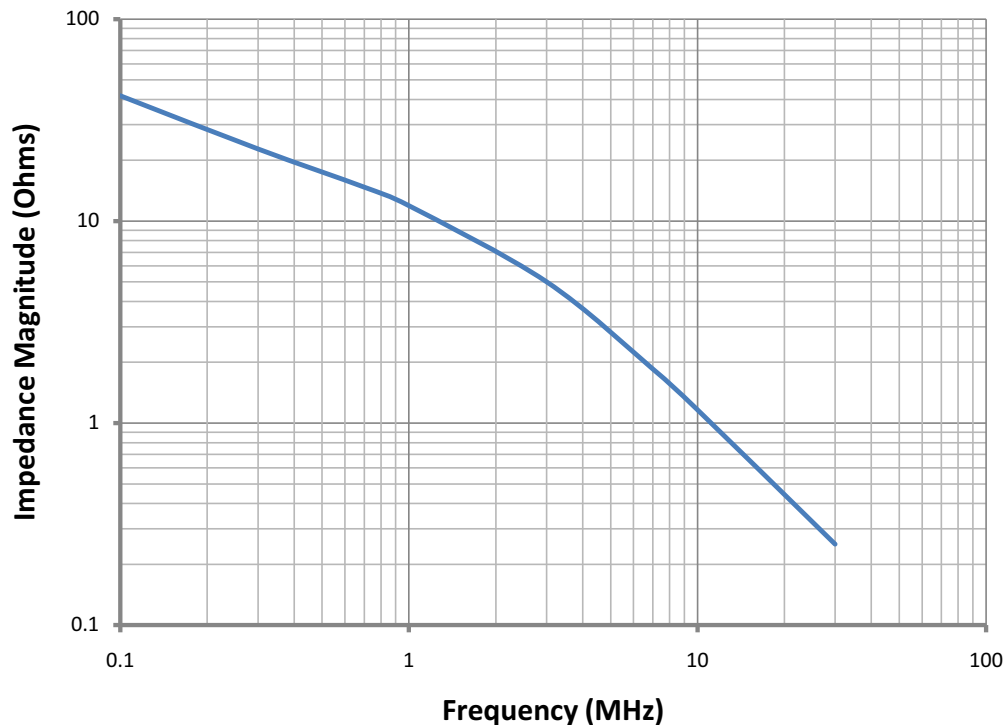
DSPLL™ supports both low-voltage supplies and improved SNR by using a digital interface for its controlled oscillator. A digital interface allows the SNR to remain high and the gain to be set arbitrarily low regardless of the supply voltage level. The SNR remains high because the tuning range is not limited by the supply voltage.

Other architecture choices also help: eliminating VCOs removes the concern over the tuning gain and interference altogether. Skyworks Solutions MultiSynth technology provides any-frequency synthesis simultaneously on multiple outputs using only a single VCO per IC. By employing only one VCO, Skyworks Solutions has increased functional density without increasing interference.

## 4. Measurement of Supply Sensitivity

Benchmarking the system performance can be as difficult as building in ripple rejection. Two common challenges are universally present. First, power supplies have low impedance in order to maintain constant voltage regardless of the load and, second, jitter/phase noise test equipment usually only supports "single-ended" analog signals instead of differential and/or rail-to-rail signals associated with high-performance timing circuits. To properly evaluate the jitter performance, accounting for the low impedance supply rails and the signaling requirements is necessary.

Having a low impedance network to analyze implies that high current will be necessary to achieve the desired ripple voltage (e.g., 100 mVpp), and high current signal sources are not common. To place a constant voltage ripple signal on a node that has a low impedance requires the ripple source to have a high drive strength. An easy way to achieve sufficient dc current for device operation and sufficient ac current for ripple generation is to source these requirements from separate supplies. This separation can be achieved by using a standard power supply and ac couple in parallel with a sinusoidal signal source (ripple source). The ripple source will need high impedance at dc to avoid sinking significant current from the power supply and potentially damaging the ripple source. Low impedance is also nebulous as a description since impedance is a function of frequency (see Figure 4).

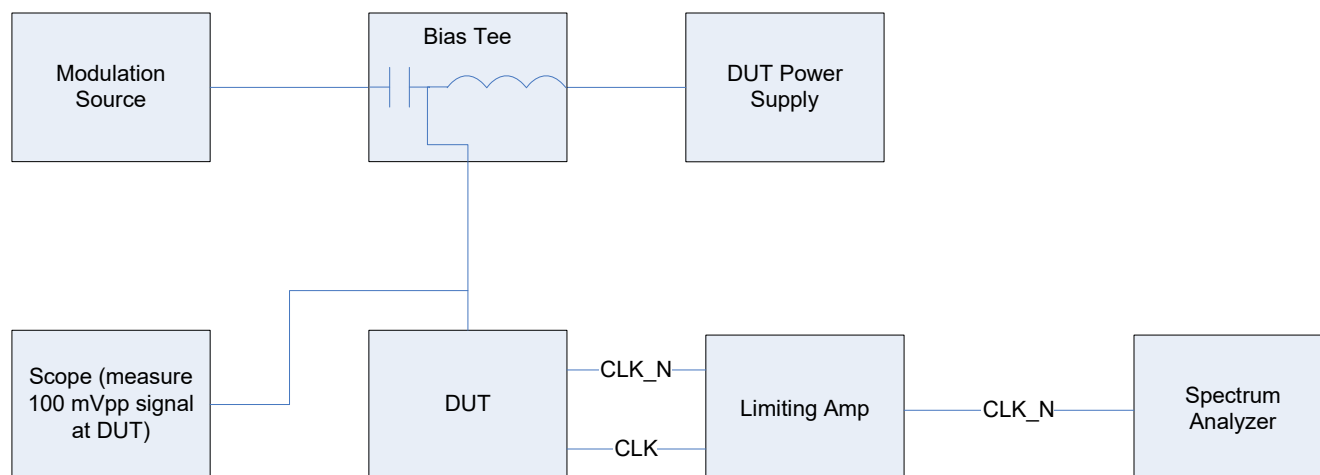


**Figure 4. Magnitude Response (MHz) of the PCB and IC Power to Ground Impedance**

Consequently, the ripple source must be adjusted for each interference frequency to achieve a constant ripple voltage. The phase of the ripple signal is often ignored since it does not provide actionable data (i.e., the goal is to limit the magnitude of the ripple response; therefore, focus on the magnitude response).

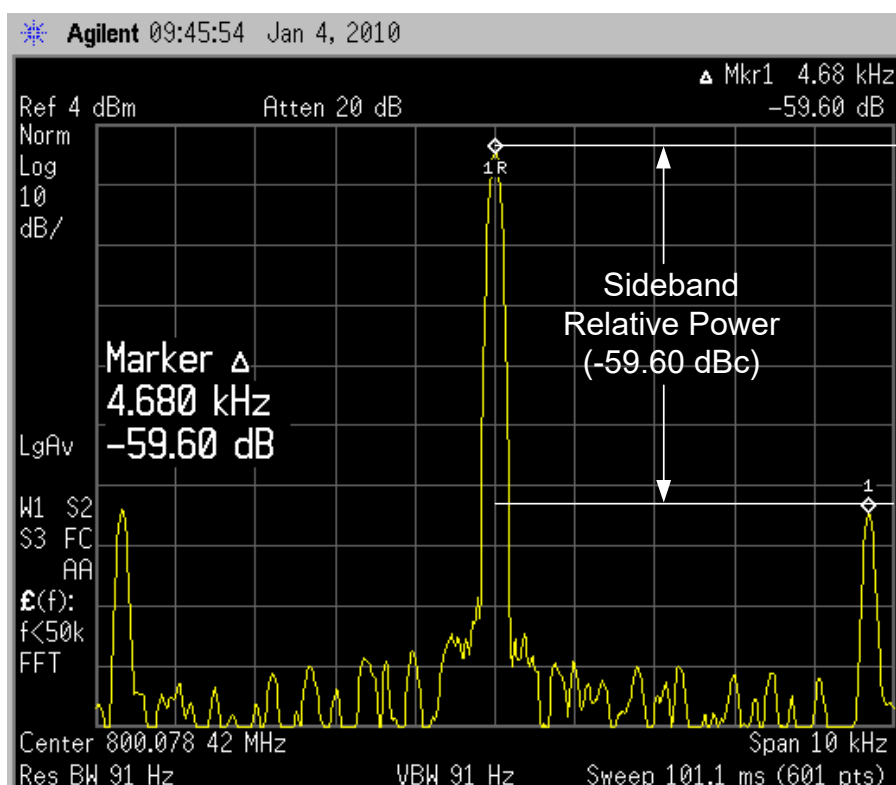
To overcome a single-ended analyzer input, use a differential amplifier or limiting amplifier. The phase noise (i.e., jitter) is convoluted with amplitude noise and must be separated. A limiting amplifier rejects the common-mode interference so that a spectrum will only report the phase response.

Figure 5 shows a typical PSRR setup for timing products. The setup includes a power supply, ripple source (function generator), oscilloscope, device under test, limiting amplifier, and spectrum analyzer. Together, this equipment forms the basis for measuring the ripple sensitivity of a timing IC.



**Figure 5. PSRR Setup**

The primary measurement is the relative power of the side-band tones (spurs) induced by the ripple source shown in Figure 6.



**Figure 6. Sideband Spurious Measurement Example**

Relative power is expressed in decibels (dB) relative to the output frequency (carrier) with units expressed as dBc (decibels relative to the carrier power). Because the limiting amplifier removes most of the amplitude noise and interference, it can be assumed that the measured side-band spurs can be attributed entirely to phase jitter. This allows a direct measurement of the RMS jitter induced by the ripple source. Equation 1 shows the relationship between side-band relative power and RMS jitter. The spurs are measured across a desired frequency range after setting the ripple voltage to a desired level (e.g., 100 mVpp).

$$\text{Jitter}_{\text{RMS}} = \frac{10^{\frac{x}{20}}}{(\sqrt{2})(\pi)(f_{\text{carrier}})}$$

where x is the spurious amplitude relative to the carrier in dBc

## Equation 1. RMS Jitter Calculated for Phase-Induced Spurious Signals

### 4.1. Example

A common scenario to consider is the jitter resulting from 100 mVpp sinusoidal ripple across the 10 kHz to 30 MHz range. Such a comparison was made with Skyworks Solutions' Si530 XO products and a competing product (see Figure 7).

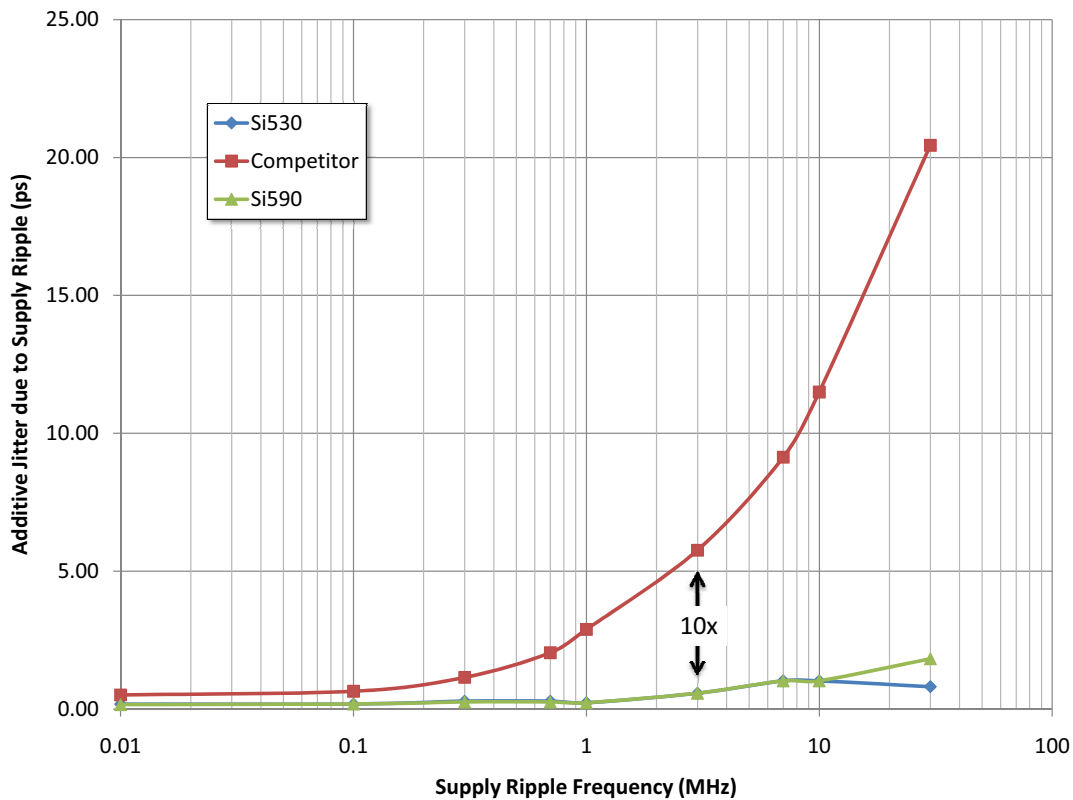


Figure 7. Additive RMS Jitter Comparison at 155.52 MHz with 100 mVpp Supply Ripple

## 5. Conclusion

Power supply ripple rejection performance is dependent on the internal power supply filtering and architectural choices within timing ICs. Designers can evaluate timing ICs through a simple frequency sweep and compare devices for a constant ripple voltage. Such comparisons can help designers select the best device for their system, which is especially important when differences in performance are dramatic (e.g., 10x worse for crystal oscillators).

**NOTES:**



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