ACA1206

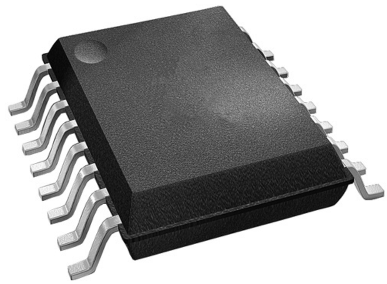
1 GHz CATV Line Amplifier
PRELIMINARY DATA SHEET

FEATURES

- 15 dB Gain
- Very Low Distortion
- Excellent Input/Output Match
- Low DC Power Consumption
- Good RF Stability with High VSWR Load Conditions
- RoHS-compliant Surface Mount Package Compatible with Automatic Assembly
- Repeatability of Monolithic Fabrication
- Meets Cenelec Standards
- 1 GHz Specified Performance

APPLICATIONS

- CATV Distribution Amplifier
- High Linearity CATV Amplifier



S7 Package
16 Pin Wide Body SOIC
with Heat Slug

PRODUCT DESCRIPTION

The ACA1206 is a surface mount monolithic GaAs RF Linear Amplifier that has been developed to replace, in new designs, the standard CATV Hybrid amplifiers currently in use. The MMIC consist of two parallel amplifiers, each with 15 dB gain. The amplifier is optimized for exceptionally low distortion and noise figure while providing flat gain and excellent input and output return loss for applications up to 1 GHz. The device requires single +12 V supply and is offered in a RoHS-compliant package.

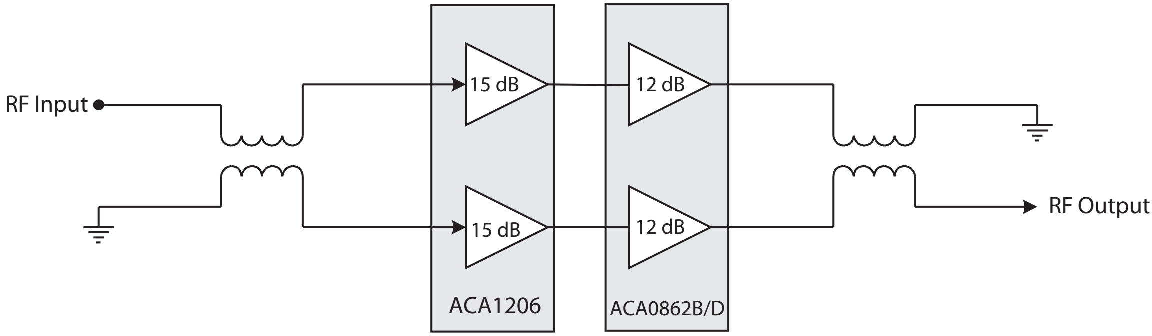


Figure 1: Hybrid Application Diagram

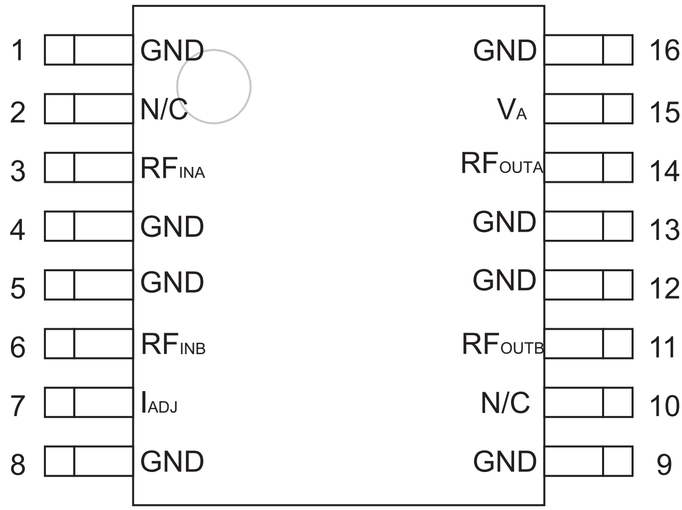


Figure 2: Pin Out

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	GND	Ground	9	GND	Ground
2	N/C	No Connection	10	N/C	No Connection
3	RF_{INA}	Input to Amplifier A	11	RF_{OUTB}	Output from Amplifier B
4	GND	Ground	12	GND	Ground
5	GND	Ground	13	GND	Ground
6	RF_{INB}	Input to Amplifier B	14	RF_{OUTA}	Output from Amplifier A
7	I_{ADJ}	Current Adjust	15	V_A	Supply for Amplifier A
8	GND	Ground	16	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Mimimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Amplifier Supplies (pins 10, 11, 14, 15)	0	+15	VDC
RF Input Power (pins 3, 6)	-	+70	dBmV
Storage Temperature	-65	+150	°C
Soldering Temperature	-	+260	°C
Soldering Time	-	5.0	sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:
(1) Pins 3 and 6 should be AC-coupled. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
RF Frequency	40	-	1000	MHz
Supply: V_{DD} (pins 10, 11, 14, 15)	-	+12	-	VDC
Operating Temperature	-40	-	+110	^{O}C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications
(T_A = +25 °C, V_{DD} = +12 VDC)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain at 1 GHz (1)	13.7	14.2	14.7	dB	
Gain Flatness	- - -	0.1□0.1 □0.3 0.1 □0.1	- - -	dB	45 to 100 MHz 100 to 800 MHz 800 to 1002 MHz
Noise Figure at 1 GHz (1)	-	3.0	3.5	dB	
CTB 195 mA (1), (3), (4)	- - -	-72 -75 -	-69 - -	dBc	77 Channels 110 Channels 128 Channels
CTB 325 mA (1), (2), (5)	- - -	-75 -74 -	-72 - -	dBc	77 Channels 110 Channels 128 Channels
CSO 195 mA (1), (3), (4)	- - -	-75 -77 -	-68 - -	dBc	77 Channels 110 Channels 128 Channels
CSO 325 mA (1), (2), (5)	- - -	-75 -72 -	-64 - -	dBc	77 Channels 110 Channels 128 Channels
XMOD 195 mA (1), (3), (4)	- - -	-64 -68 -	-61 - -	dBc	77 Channels 110 Channels 128 Channels
XMOD 325 mA (1), (2), (5)	- - -	-69 -70 -	-67 - -	dBc	77 Channels 110 Channels 128 Channels
Supply Current (I_{DD})	185 300	195 325	205 350	mA	R1 = 5.2 k□ R1 = 2 k□
Cable Equivalent Slope (1)	-	TBD	-	dB	
Return Loss (1)	18	22	-	dB	
Thermal Resistance	-	-	6.0	°C/W	

Notes:
(1) Measured with a balun on the input and output of the device. See Figure 25 for test setup.
(2) 15.6 dB tilt, 49 dBmV output (per channel) at 1002 MHz plus QAM set 6 dBmV down from carrier.
(3) 3 dB tilt, 37 dBmV output (per channel) at 1002 MHz plus QAM set 6 dBmV down from carrier.
(4) Tested with R1 = 5.2 kΩ
(5) Tested with R1 = 2 kΩ

Performance DATA

Figure 3: Gain vs. Frequency (VDD = +12 V, IDD = 195 mA)

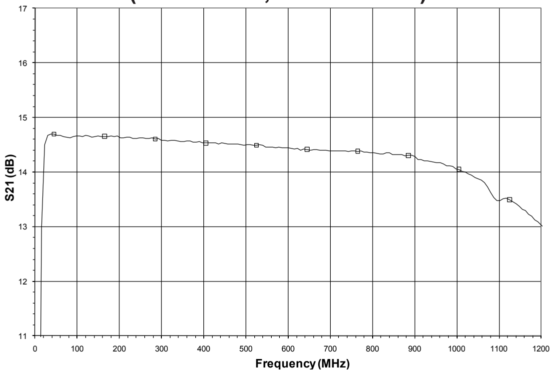


Figure 4: Reverse Isolation vs. Frequency (VDD = +12 V, IDD = 195 mA)

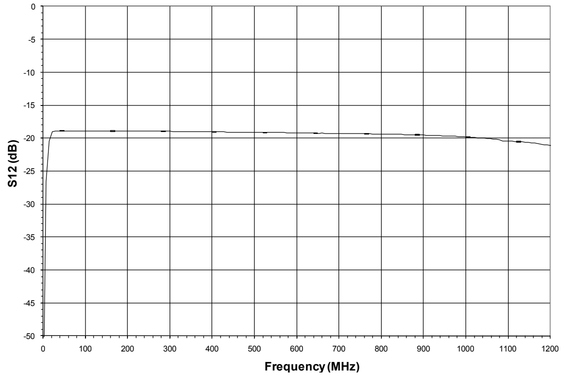


Figure 5: Input Return Loss vs. Frequency (VDD = +12 V, IDD = 195 mA)

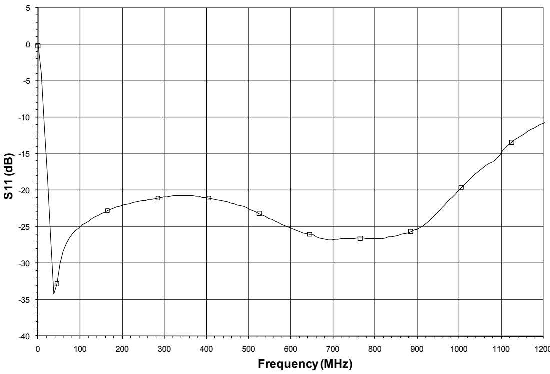


Figure 6: Output Return Loss vs. Frequency (VDD = +12 V, IDD = 195 mA)

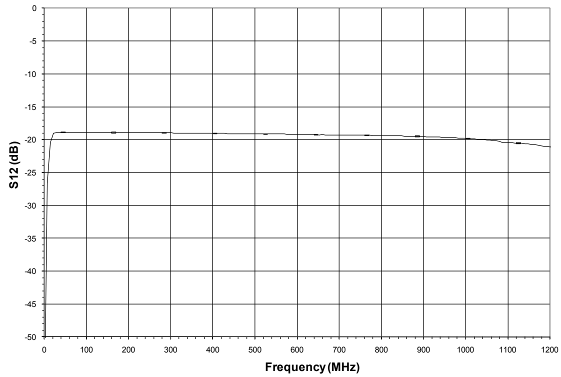


Figure 7: Noise Figure vs. Frequency (VDD = +12 V, IDD = 195 mA)

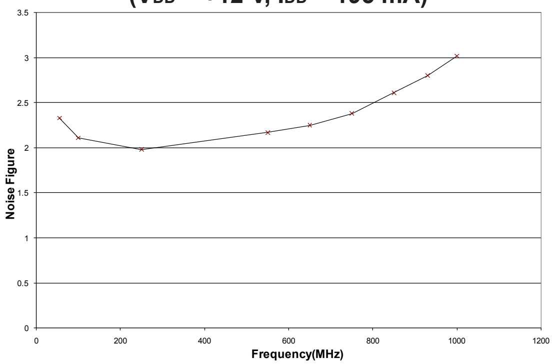


Figure 7a: ACA1206 P1dB vs. Frequency (IDD = 195 mA)

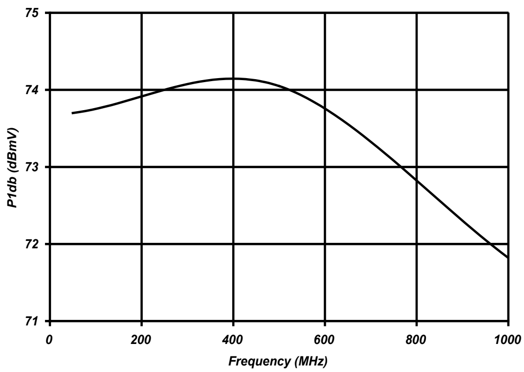


Figure 8: CTB vs. Frequency
(V_{DD} = +12 V, I_{DD} = 195 mA, 79 Analog Channels, 3 dB Tilt, +37 dBmV output power at 1 GHz)

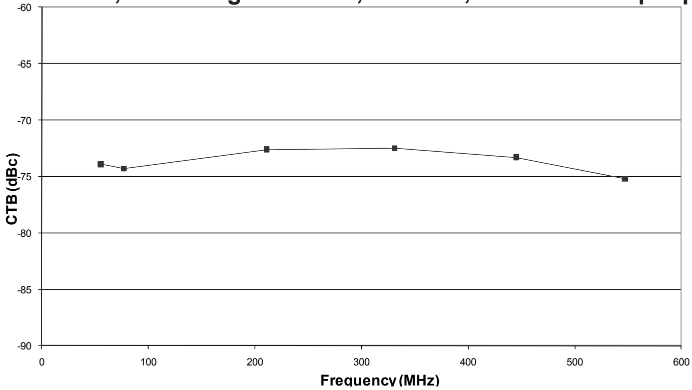


Figure 9: CSO vs. Frequency
(V_{DD} = +12 V, I_{DD} = 195 mA, 79 Analog Channels, 3 dB Tilt, +37 dBmV output power at 1 GHz)

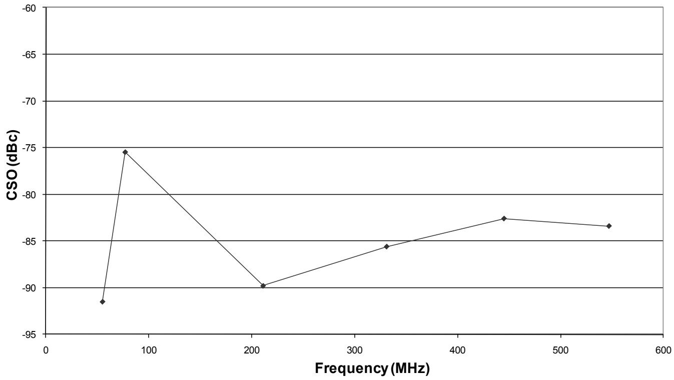


Figure 10: XMOD vs. Frequency
(V_{DD} = +12 V, I_{DD} = 195 mA, 79 Analog Channels, 3 dB Tilt, +37 dBmV output power at 1 GHz)

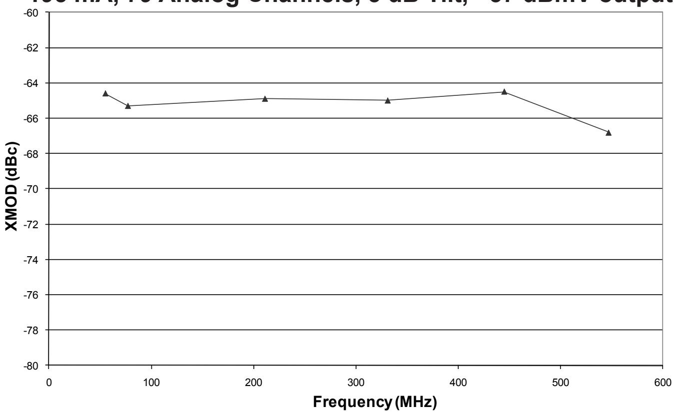


Figure 11: CTB vs. Frequency
(V_{DD} = +12 V, I_{DD} = 195 mA, 112 Analog Channels, 3 dB Tilt, +37 dBmV output power at 1 GHz)

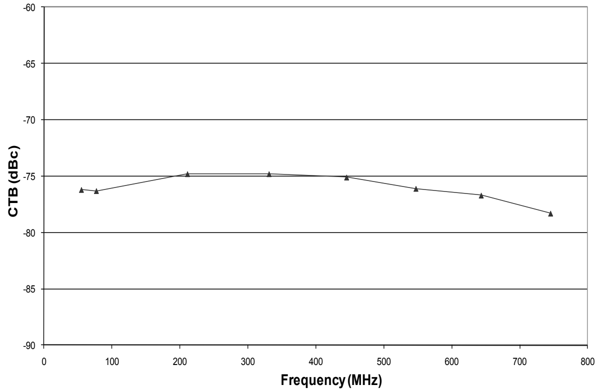


Figure 12: CSO vs. Frequency
(V_{DD} = +12 V, I_{DD} = 195 mA, 112 Analog Channels, 3 dB Tilt, +37 dBmV output power at 1 GHz)

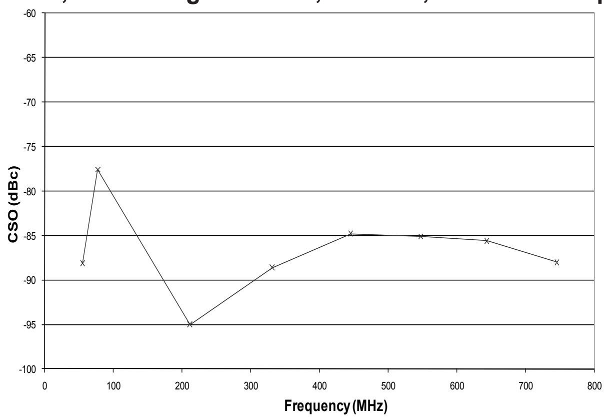


Figure 13: XMOD vs. Frequency
(V_{DD} = +12 V, I_{DD} = 195 mA, 112 Analog Channels, 3 dB Tilt, +37 dBmV output power at 1 GHz)

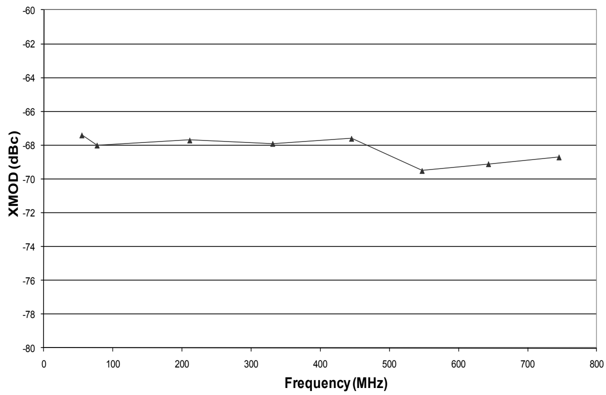


Figure 13a: ACA1206 MER – 64 QAM @ 85 MHz (I_{DD} = 195 mA)

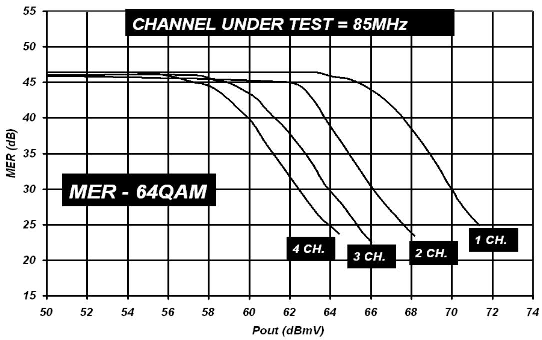


Figure 13b: ACA1206 MER – 64 QAM @ 543 MHz (I_{DD} = 195 mA)

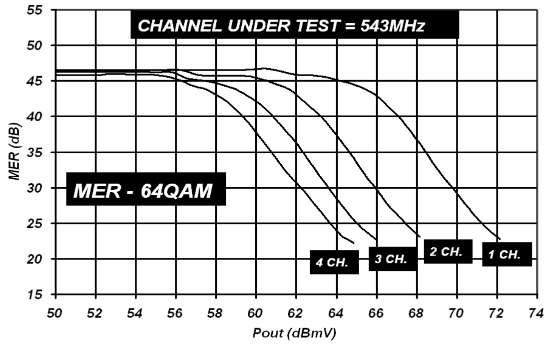


Figure 13c: ACA1206 MER – 64 QAM @ 987 MHz (I_{DD} = 195 mA)

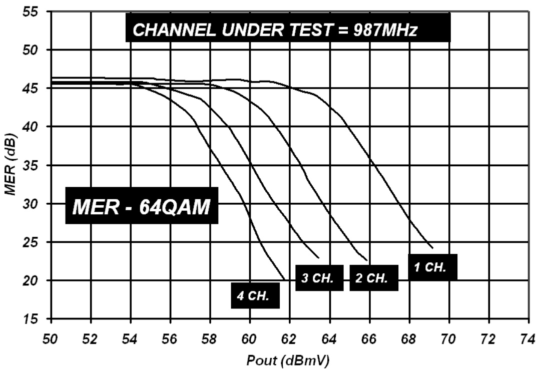


Figure 13d: ACA1206 MER – 256 QAM @ 85 MHz (I_{DD} = 195 mA)

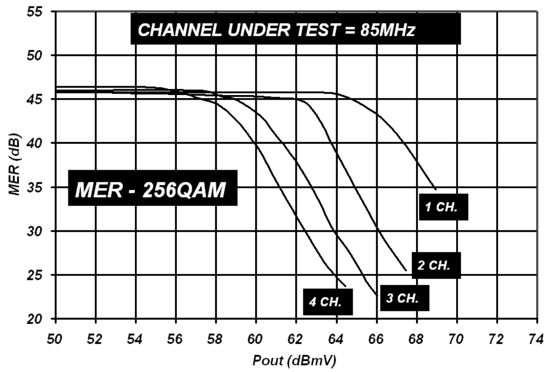


Figure 13e: ACA1206 MER – 256 QAM @ 543 MHz (I_{DD} = 195 mA)

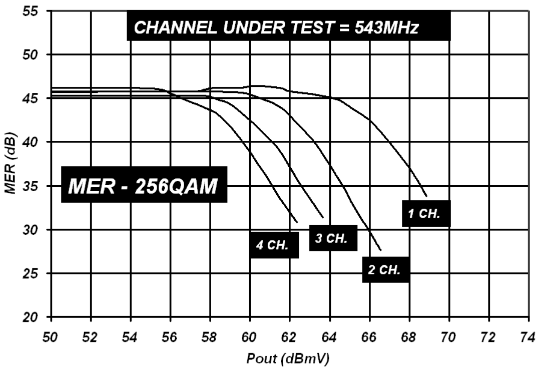


Figure 13f: ACA1206 MER – 256 QAM @ 987 MHz (I_{DD} = 195 mA)

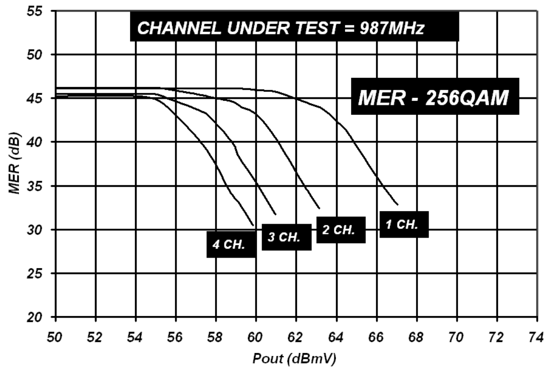


Figure 14: Gain vs. Frequency (V_{DD} = +12 V, I_{DD} = 325 mA)

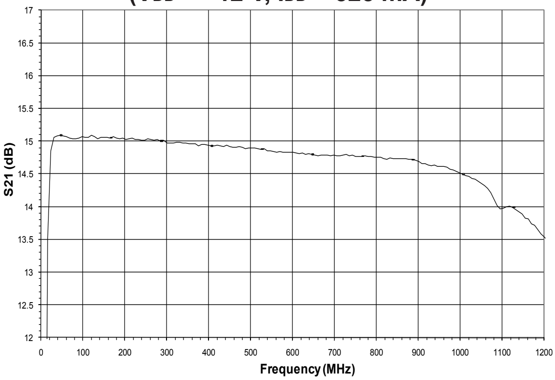


Figure 15: Reverse Isolation vs. Frequency (V_{DD} = +12 V, I_{DD} = 325 mA)

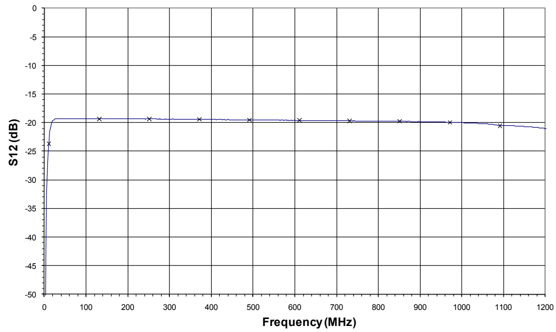


Figure 16: Input Return Loss vs. Frequency (V_{DD} = +12 V, I_{DD} = 325 mA)

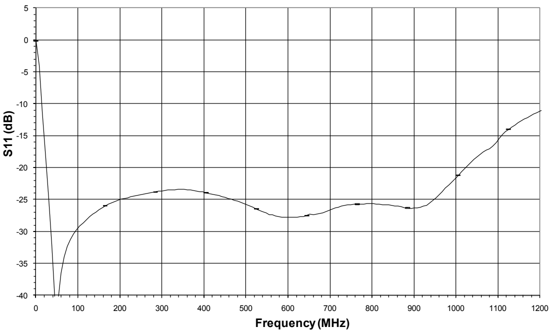


Figure 17: Output Return Loss vs. Frequency (V_{DD} = +12 V, I_{DD} = 325 mA)

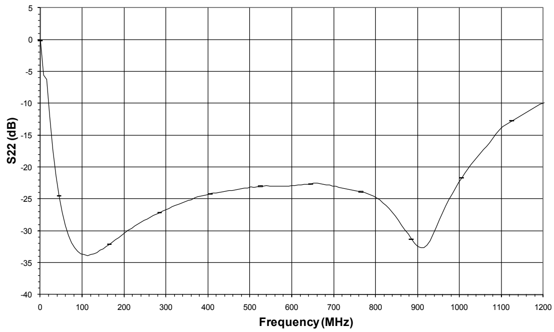


Figure 18: Noise Figure vs. Frequency (V_{DD} = +12 V, I_{DD} = 325 mA)

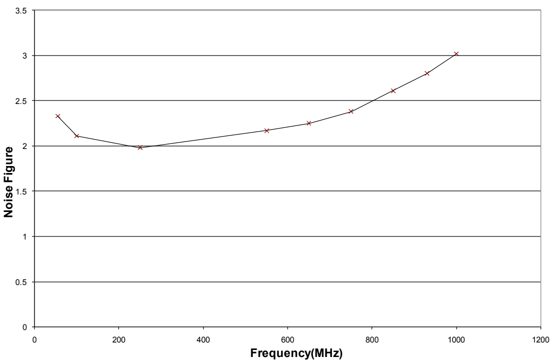


Figure 18a: ACA1206 P1dB vs. Frequency (I_{DD} = 325 mA)

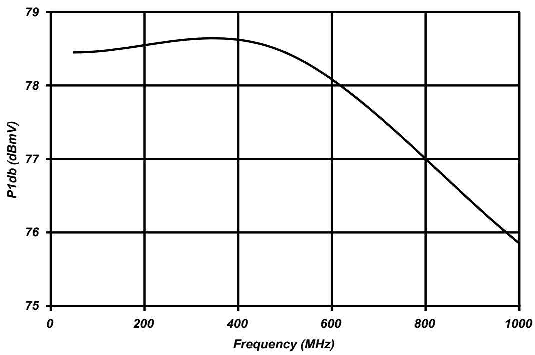


Figure 19: CTB vs. Frequency
(V_{DD} = +12 V, I_{DD} = 325 mA, 79 Analog Channels, 15.6 dB Tilt, +49 dBmV output power at 1 GHz)

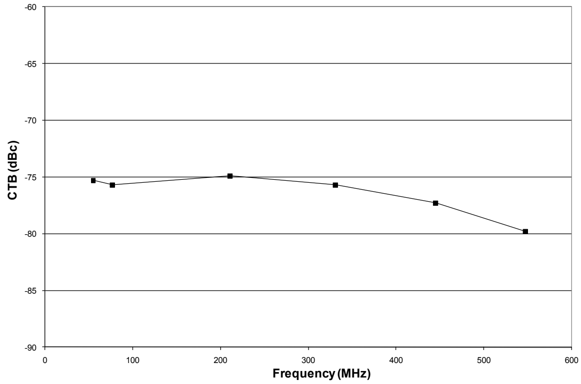


Figure 20: CSO vs. Frequency
(V_{DD} = +12 V, I_{DD} = 325 mA, 79 Analog Channels, 15.6 dB Tilt, +49 dBmV output power at 1 GHz)

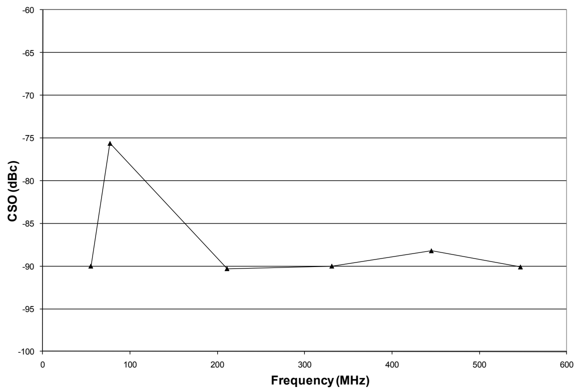


Figure 21: XMOD vs. Frequency
(V_{DD} = +12 V, I_{DD} = 325 mA, 79 Analog Channels, 15.6 dB Tilt, +49 dBmV output power at 1 GHz)

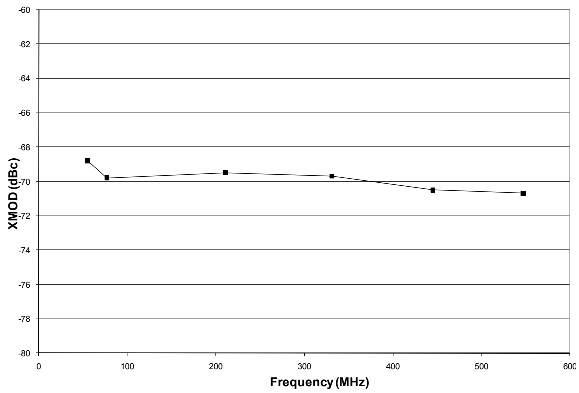


Figure 22: CTB vs. Frequency
(V_{DD} = +12 V, I_{DD} = 325 mA, 112 Analog Channels, 15.6 dB Tilt, +49 dBmV output power at 1 GHz)

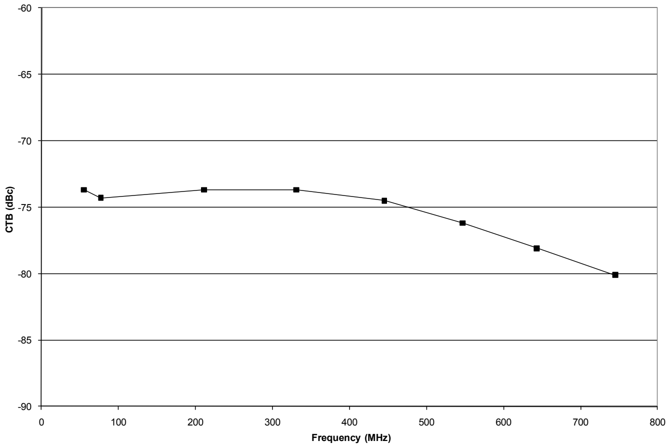


Figure 23: CSO vs. Frequency
(V_{DD} = +12 V, I_{DD} = 325 mA, 112 Analog Channels, 15.6 dB Tilt, +49 dBmV output power at 1 GHz)

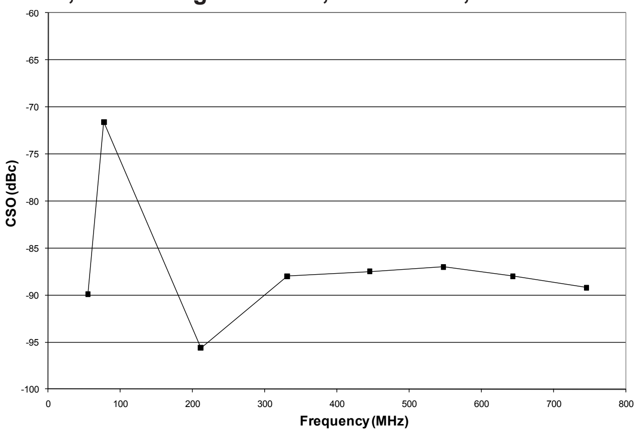
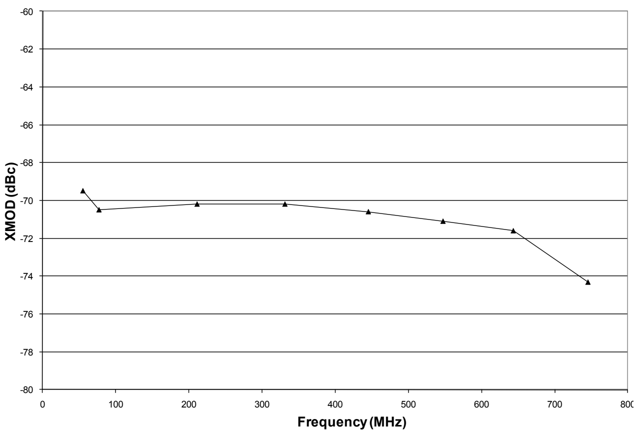


Figure 24: XMOD vs. Frequency
(V_{DD} = +12 V, I_{DD} = 325 mA, 112 Analog Channels, 15.6 dB Tilt, +49 dBmV output power at 1 GHz)



Performance DATA

Figure 24a: ACA1206 MER – 64 QAM @ 85 MHz (IDD = 325 mA)

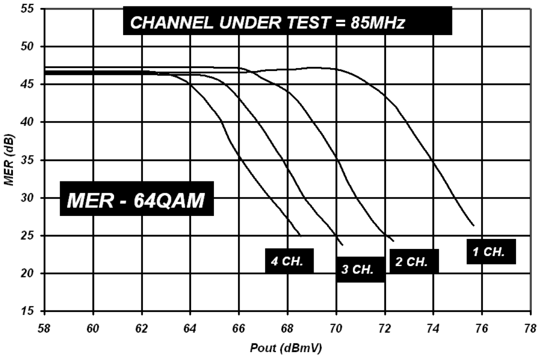


Figure 24b: ACA1206 MER – 64 QAM @ 543 MHz (IDD = 325 mA)

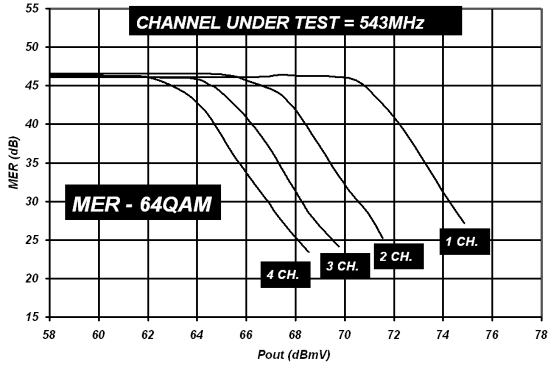


Figure 24c: ACA1206 MER – 64 QAM @ 987 MHz (IDD = 325 mA)

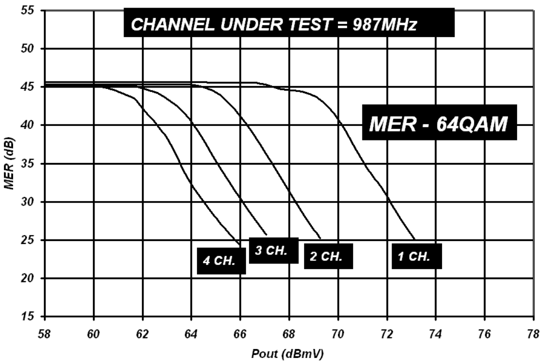


Figure 24d: ACA1206 MER – 256 QAM @ 85 MHz (IDD = 325 mA)

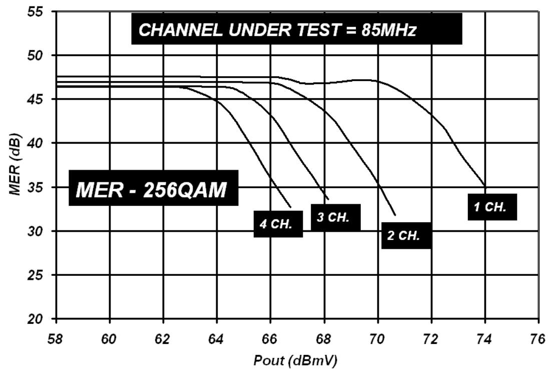


Figure 24e: ACA1206 MER – 256 QAM @ 543 MHz (IDD = 325 mA)

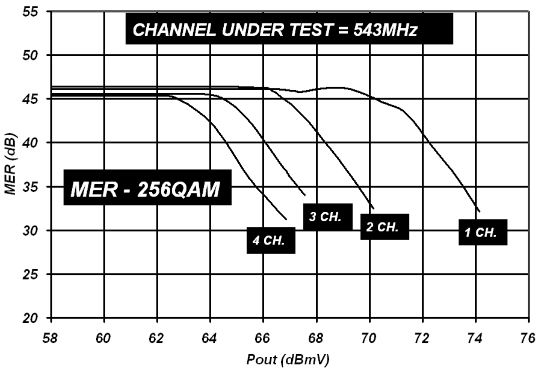
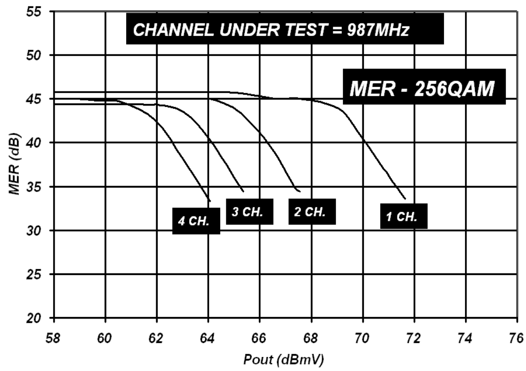


Figure 24f: ACA1206 MER – 256 QAM @ 987 MHz (IDD = 325 mA)



APPLICATION INFORMATION

The ACA1206 is designed as an input stage. This part can be used alone for low gain, low output level applications or can be cascaded with one of the ACA0862 output stages for higher gain and output signal drive level. The ACA1206 is a low power dissipation part designed as a driver for the ACA0862B output stage.

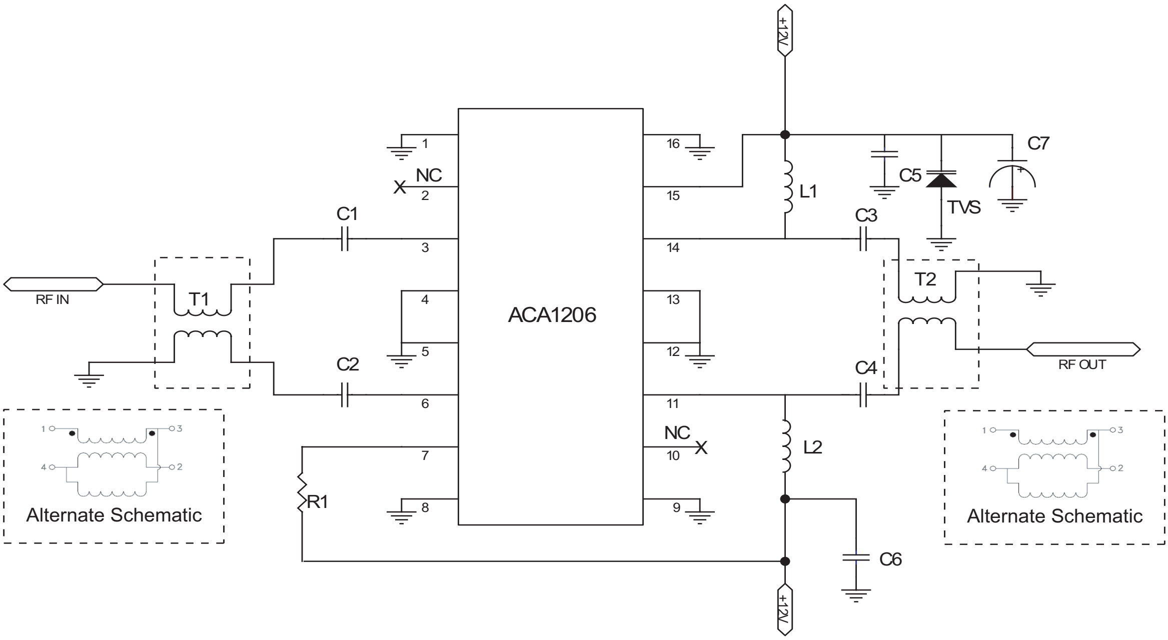


Figure 25: Evaluation Board Schematic

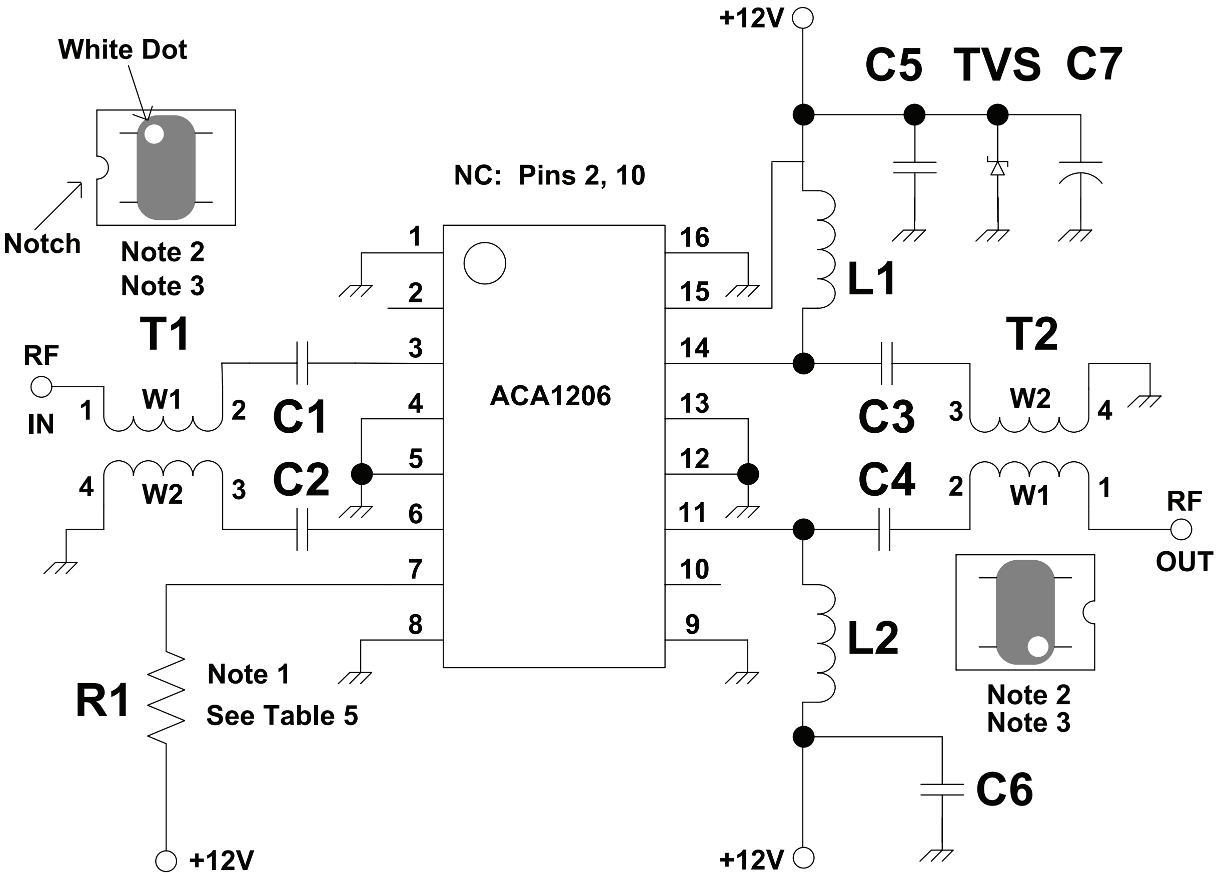


Figure 26: Test Circuit Schematic

Table 5

NOMINAL CURRENT(1)	R1
195 mA	5.2 kΩ
325 mA	2 kΩ

Notes:
(1) Values are approximate for resistors specified.
(2) W1/W2 indicate balun (Figure 27) orientation.
(3) 1, 2, 3, 4 indicate orientation of alternate balun (Figure 28). Note the position of the notch and the white dot at pin 1.

Table 6: Evaluation Board Bill of Materials

ITEM	DESCRIPTION	QTY	VENDOR	VENDOR P/N
C1,C2,C5,C6	0.01uF. CHIP CAP.	4	MURATA	GRM39X7R1103K25V
C3,C4	330 pF. CHIP CAP.	2	MURATA	GRM1555C1H331JA01D
C7	47 uF ELECT.CAP.	1	DIGI-KEY CORP.	P5275-ND
L1,L2	470 nH CHIP IND.	2	Coil Craft	1008CS-471X_L_
T1,T2- BALUN	CORE	2	Fair-Rite	2843002702
	WIRE		MWS Wire Ind.	T-2361429-20
T1, T2 BALUN (alternate)	Transmission Line BALUN	1	MPS Industries Torrance, CA	R3591
R1 (4)	2 k□ 5.2k□	1	Panasonic	ERJ-3EKF2001V ERJ-3EKF5231V
TVS	TVS 12 VOLT. 600 WATT	1	Little Fuse	SMBJ12A
CONNECTOR	75 □N MALE PANEL MOUNT.	2	PASTERNACK ENTERP.	PE4504
PCB	PRINTED CIRCUIT BOARD	1	ANADIGICS	
INDIUM	300 x 160 MILS	1	INDIUM CORP. OF AMERICA	14996Y

Notes:
(1) T1, T2 (balun) wind 5.5 turns thru core as shown (Figure 26).
(2) “N” connector, center pin, should be approximately 80 mils in length.
(3) Due to the higher power dissipation of this device the PC board should be mounted/attached to a large heat sink.
(4) See Table 5

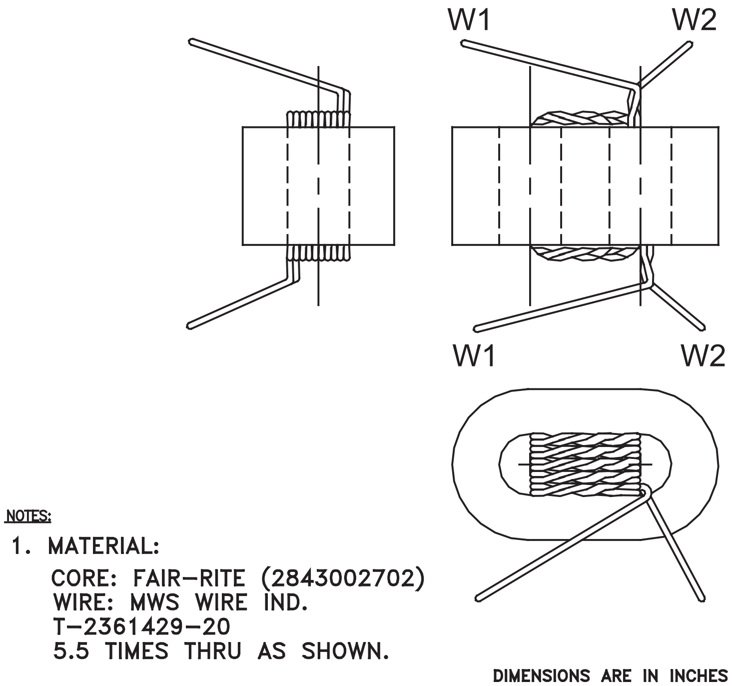


Figure 27: Balun Drawing

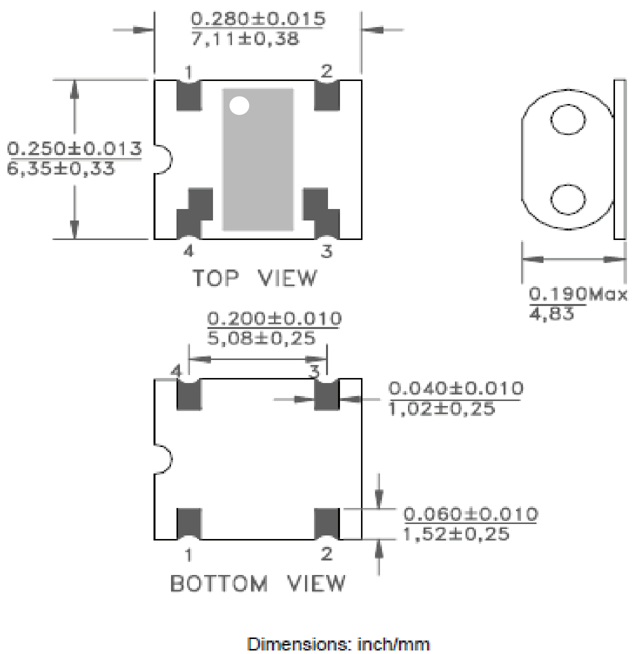


Figure 28: Alternate Balun Drawing

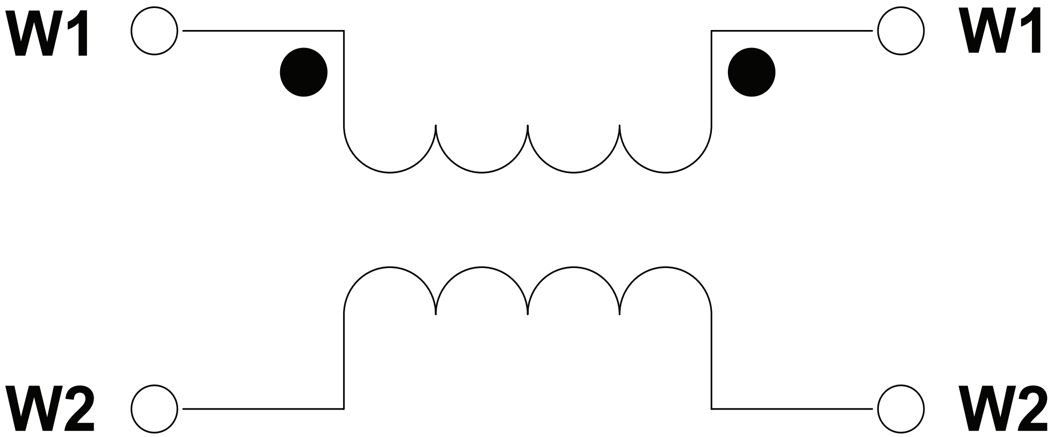


Figure 29: Hand-Wound Balun Schematic

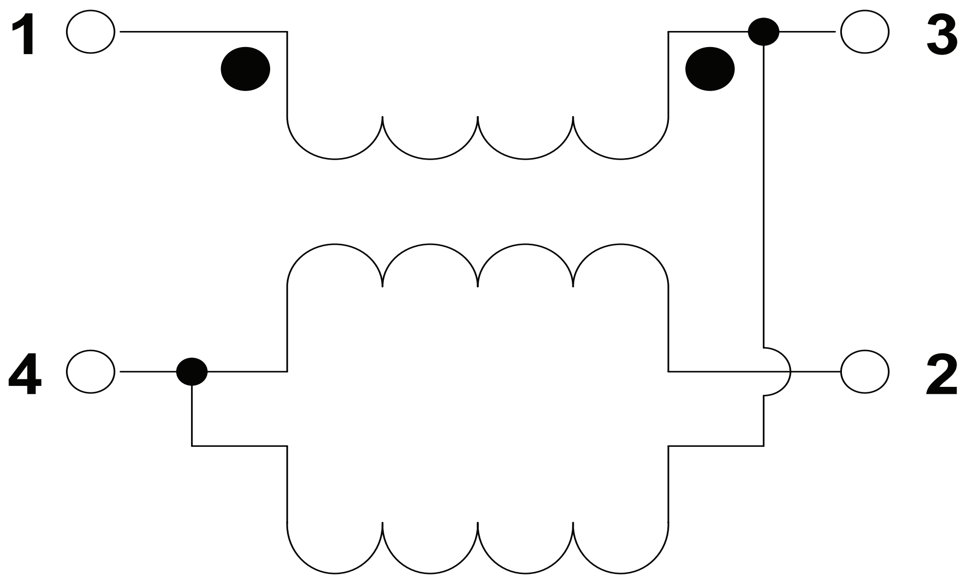
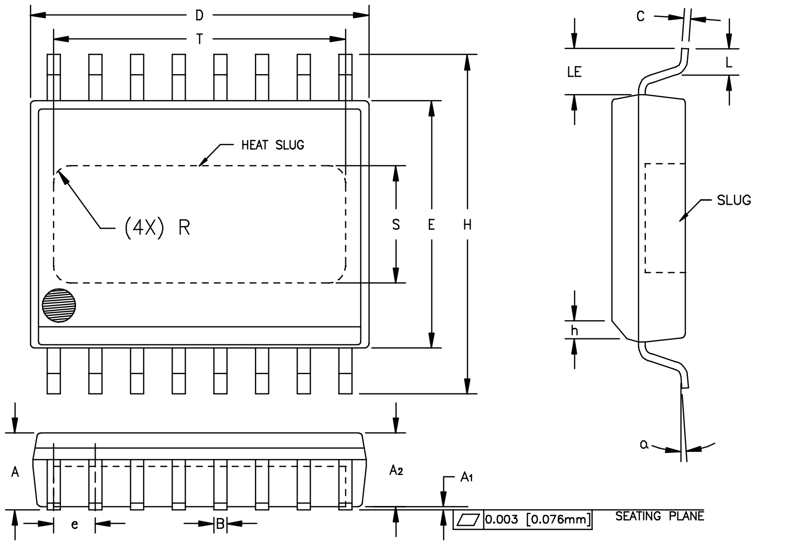


Figure 30: Alternate Balun Schematic

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.087	0.098	2.21	2.49	
A_1	0.000	0.004	0.00	0.10	6
A_2	0.087	0.094	2.21	2.39	
B	0.013	0.019	0.33	0.48	
C	0.007	0.009	0.18	0.23	
D	0.398	0.412	10.11	10.46	2
E	0.290	0.300	7.37	7.62	3
e	0.050 BSC		1.27 BSC		4
H	0.394	0.418	10.01	10.62	
h	0.010	0.028	0.25	0.71	
L	0.024	0.040	0.61	1.02	
LE	0.052	—	1.32	—	
α	0°	8°	0°	8°	
S	0.120	0.140	3.05	3.56	5
T	0.330	0.350	8.38	8.89	5
R	REF. 0.015		REF. 0.38		5

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE 0.002 [0.05mm]
5. DIMENSIONS "S", "T" AND "R" INDICATE EXPOSED SLUG AREA.
6. STANDOFF HEIGHT (A_1) MEASURED FROM BOTTOM OF SLUG.

Figure 31: S7 Package Outline - 16 Pin Wide Body SOIC with Heat Slug

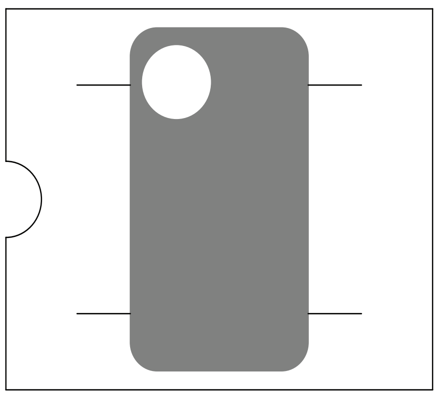
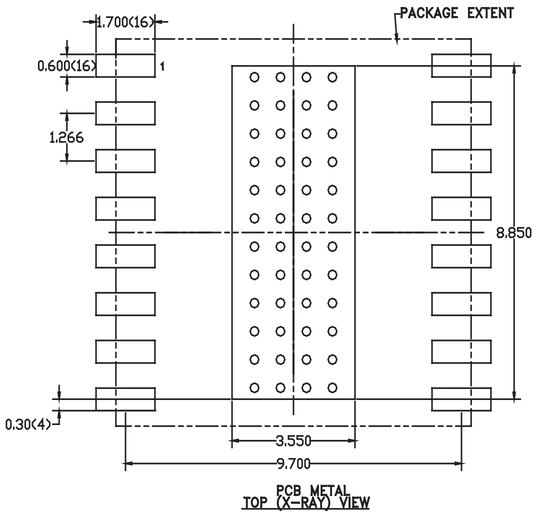


Figure 32: Package Outline - Alternate Balun



Notes:

(1) OUTLINE DRAWING REFERENCE:
FIGURE 29, S7 PACKAGE.

(2) UNLESS SPECIFIED DIMENSIONS
ARE SYMMETRICAL ABOUT CENTER
LINES SHOWN.

(3) DIMENSIONS IN MILLIMETERS.

(4) VIAS SHOWN IN PCB METAL VIEW
ARE FOR REFERENCE ONLY.
NUMBER & SIZE OF THERMAL VIAS
REQUIRED DEPENDENT ON HEA
DISSIPATION REQUIREMENT AND THE
PC PROC SS CAPABILITY.

(5) RECOMMENDED STENCIL THICKNESS:
APPROX. 0.125 mm (5 Mils)

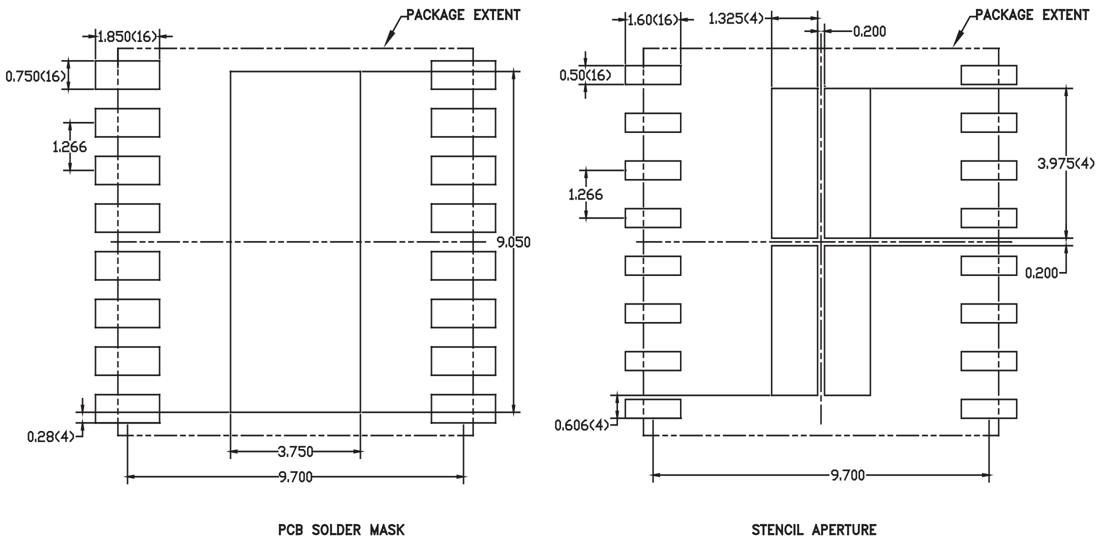


Figure 33: PCB Pad Layout and Solder Mask Detail

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ACA1206RS7P2	-40°C to 110°C	RoHS-Compliant 16 Pin Wide Body SOIC with Heat Sink	1,500 Piece Tape & Reel

NOTES

Skyworks Solutions, Inc.
Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com