

**DATA SHEET**

# SKY12340-364LF: 300 kHz – 2.0 GHz Five-Bit Digital Attenuator with Serial-to-Parallel Driver

**Applications**

- Cellular infrastructure
- Wireless receivers

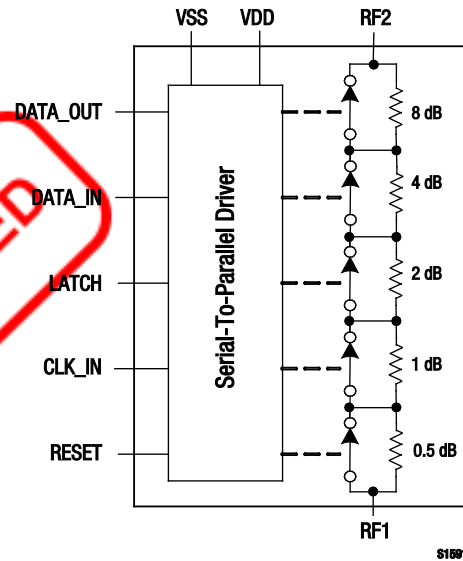
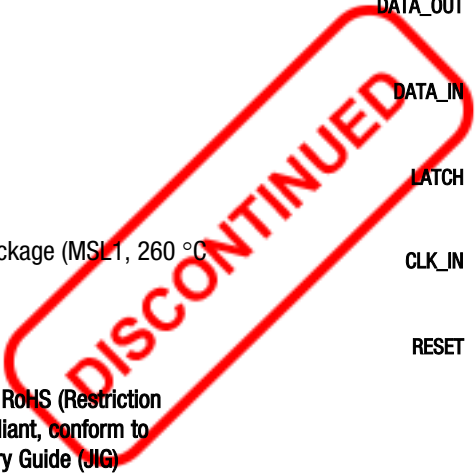
**Features**

- Single, +5 V DC supply voltage
- Integrated silicon serial-to-parallel driver
- Attenuation: 0.5 dB steps to 15.5 dB
- Small, QFN (32-pin, 5 x 5 mm) Pb-free package (MSL1, 260 °C per JEDEC J-STD-020)

**NEW**



Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.



**Figure 1. SKY12340-364LF Block Diagram**

**Description**

The SKY12340-364LF is a GaAs FET five-bit digital attenuator I/C with a serial-to-parallel driver. The device is provided in a 5 x 5 mm, 32-pin Quad Flat No-Lead (QFN) package.

The SKY12340-364LF is particularly suited at IF frequencies for which high attenuation accuracy, low insertion loss, and low intermodulation products are required.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

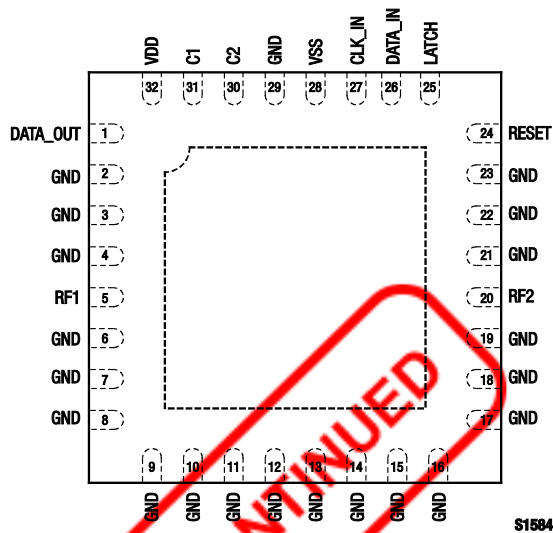


Figure 2. SKY12340-364LF Pinout – 32-Pin QFN (Top View)

Table 1. SKY12340-364LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	DATA_OUT	Serial data output	17	GND	Ground
2	GND	Ground	18	GND	Ground
3	GND	Ground	19	GND	Ground
4	GND	Ground	20	RF2	RF input/output
5	RF1	RF input/output	21	GND	Ground
6	GND	Ground	22	GND	Ground
7	GND	Ground	23	GND	Ground
8	GND	Ground	24	RESET	Reset
9	GND	Ground	25	LATCH	Latch enable
10	GND	Ground	26	DATA_IN	Serial data input
11	GND	Ground	27	CLK_IN	Serial clock input
12	GND	Ground	28	VSS	Low output voltage level
13	GND	Ground	29	GND	Ground
14	GND	Ground	30	C2	Charge pump capacitor 2
15	GND	Ground	31	C1	Charge pump capacitor 1
16	GND	Ground	32	VDD	Supply voltage

**Functional Description**

The SKY12340-364LF is a five bit digital attenuator comprised of a GaAs attenuator and a silicon CMOS driver. The attenuation setting is controlled by a serial-to-parallel interface. Attenuation is set by a stream of data that is clocked into the shift registers of the silicon chip by the clock signal.

To set the attenuation state, a latch signal is sent to the appropriate pin to send the correct bias voltages to the GaAs attenuator. The silicon chip generates a negative voltage using a negative voltage generator that requires two external components: a charge pump capacitor connected between pins 30 (C2) and 31 (C1) and a voltage hold capacitor connected from pin 28 (VSS) to ground.

More than one attenuator can be cascaded together and the data may be passed through one device to the other using the DATA\_OUT signal (pin 1). To reset the attenuator to the insertion loss state, a logic low signal may be sent to the reset pin. DC bias voltage to the silicon CMOS chip is applied to pin 32 (VDD).

**Power-Up/Power-Down Timing**

Serial data (SDA) is shifted into the register on the rising edge of the clock (SCK), least significant bit (LSB) first. The attenuator

changes states on the rising edge of the latch-enable (LE) signal, according to the most recent five bits of shifted data accepted since the previous falling edge of the LE signal. Refer to the timing diagram in Figure 3 and timing parameter specifications in Table 2.

Power-up sequence is as follows:

0. Connect ground
1. Apply VDD
2. Set all inputs (SCK, SDA, LE)

The power-down sequence is the reverse of above.

**Electrical and Mechanical Specifications**

The absolute maximum ratings of the SKY12340-364LF are provided in Table 3. Electrical specifications are provided in Tables 4 and 5.

Typical performance characteristics of the SKY12340-364LF are illustrated in Figures 4 through 10.

The state of the SKY12340-364LF is determined by the logic provided in Table 6.

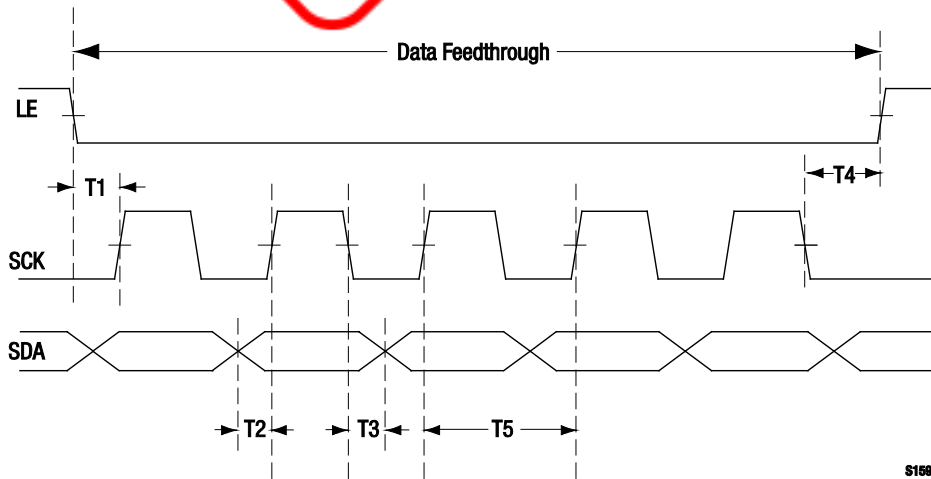


Figure 3. Power-Up/Power-Down Timing

Table 2. Power-Up/Power-Down Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
LE setup time	T1	7.5	15		ns
SDA setup time	T2	7.5	15		ns
SDA hold time	T3	5	10		ns
LE hold time	T4	5	10		ns
Clock frequency	f <sub>CLK</sub>		16	100	MHz
Clock period	T5		1/f <sub>CLK</sub>		

**Table 3. SKY12340-364LF Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V <sub>DD</sub>	-0.5		+6.0	V
Input voltage	V <sub>I</sub>	-0.5 – V <sub>DD</sub>		+0.5	V
RF input power	P <sub>IN</sub>			+25	dBm
Storage temperature	T <sub>STG</sub>	-65		+150	°C
Operating temperature	T <sub>OP</sub>	-40		+85	°C

**Note:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

**Table 4. SKY12340-364LF Electrical Specifications (Note 1)**  
**(T<sub>OP</sub> = +25 °C, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, V<sub>DD</sub> = 5 V, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss (Note 2)	IL	300 kHz to 1.0 GHz		1.4	1.5	dB
		300 kHz to 2.0 GHz		1.8	2.0	dB
Attenuation range (Note 3)				15.5		dB
Attenuation accuracy (Note 3)		300 kHz to 2.0 GHz	±(0.35 + 2% of attenuation setting in dB)			
Return loss	IS11I	300 kHz to 2.0 GHz	12	20		dB
Switching characteristics: Rise, fall On, off Video feedthrough		10/90% or 90/10% RF 50% control to 90/10% RF T <sub>RISE</sub> = 1 ns, bandwidth = 500 MHz		50 100 50		ns ns mV
1 dB input compression point	IP1dB	Insertion loss state				
		0.5 to 2.0 GHz 0.05 GHz	+27 +26	+30 +30		dBm dBm
3 <sup>rd</sup> Order Intercept Point	IP3	1 MHz spacing, P <sub>IN</sub> = +5 dBm/tone				
		Insertion loss state:				
		0.05 GHz	+43	+45		dBm
		0.5 to 2.0 GHz	+47	+50		dBm
Attenuation states:						
0.05 GHz	+41	+45		dBm		
0.5 to 2.0 GHz	+47	+50		dBm		
Input voltage: High Low	V <sub>H</sub> V <sub>L</sub>		1.7 0	3.5 0.3	5.0 0.6	V V
	Input leakage current	I <sub>L</sub>		±0.5		μA
Quiescent current	I <sub>DD</sub>			500		μA
Supply voltage	V <sub>DD</sub>			5		V

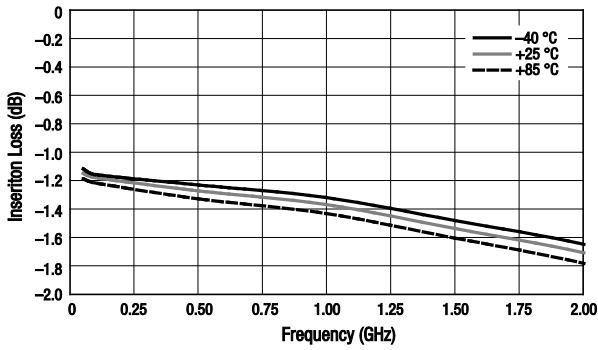
**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

**Note 2:** Insertion loss changes by 0.003 dB/°C.

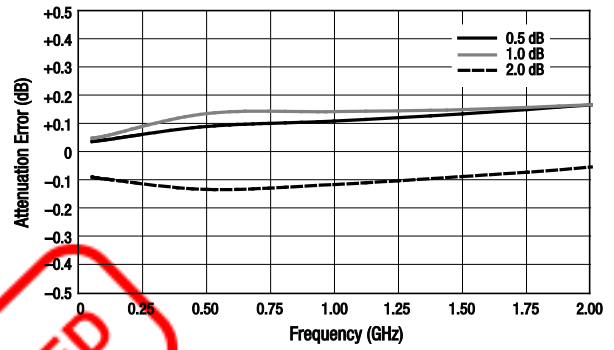
**Note 3:** Attenuation value referenced above insertion loss. Exposed pad must be connected to RF ground to obtain specified attenuation.

**Typical Performance Characteristics**

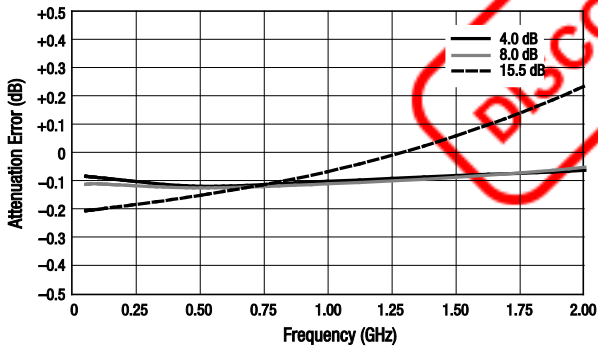
( $T_{OP} = +25\text{ }^{\circ}\text{C}$ , Characteristic Impedance [ $Z_0$ ] =  $50\ \Omega$ ,  $V_{DD} = 5\ \text{V}$ , Unless Otherwise Noted)



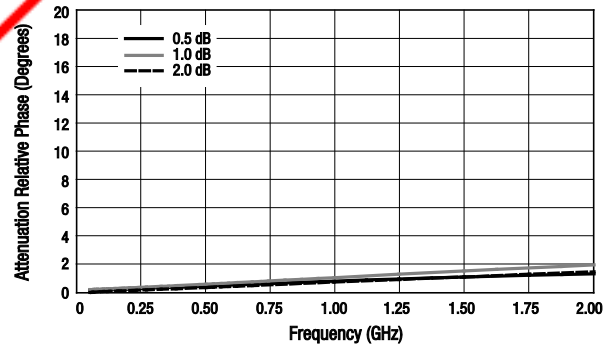
**Figure 4. Insertion Loss vs Frequency**



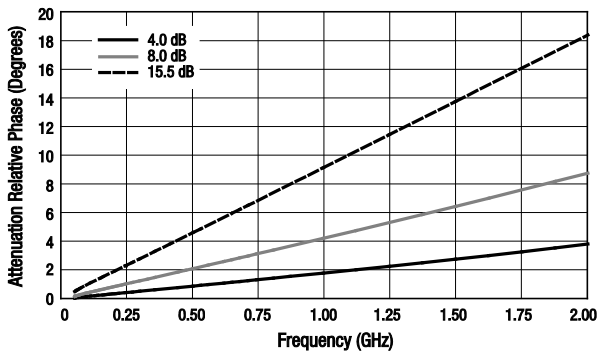
**Figure 5. Attenuation Error vs Frequency (0.5, 1.0, and 2.0 dB States)**



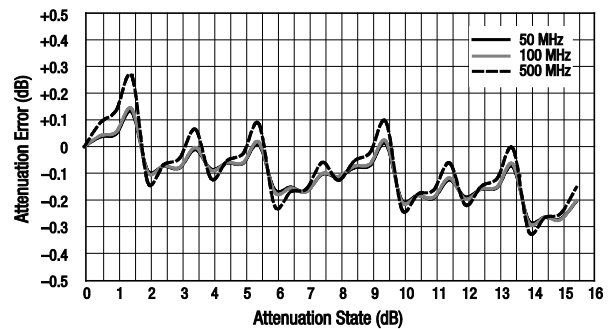
**Figure 6. Attenuation Error vs Frequency (4.0, 8.0, and 15.5 dB States)**



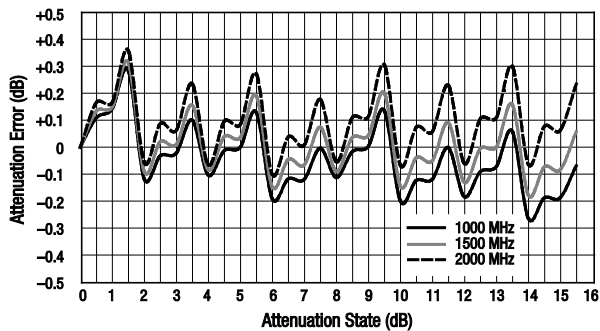
**Figure 7. Attenuation Relative Phase vs Frequency, Normalized to Insertion Loss (0.5, 1.0, and 2.0 dB States)**



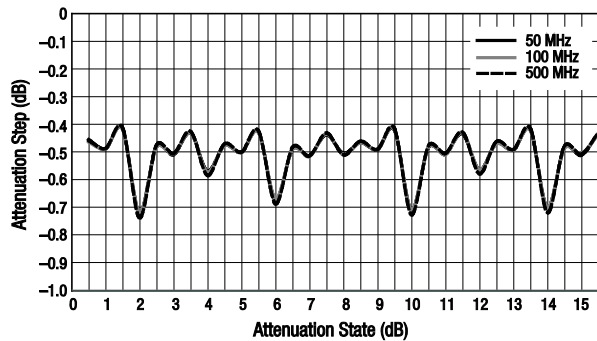
**Figure 8. Attenuation Relative Phase vs Frequency, Normalized to Insertion Loss (4.0, 8.0, and 15.5 dB States)**



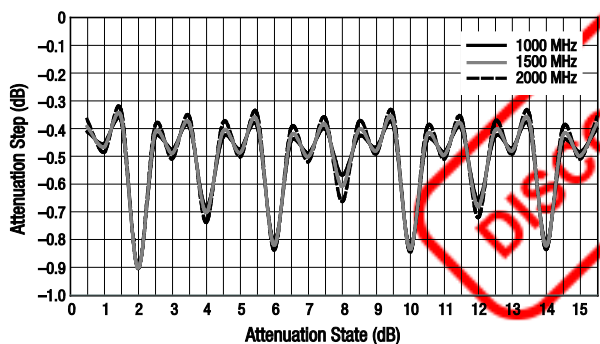
**Figure 9. Attenuation Error vs Attenuation State (@ 50, 100, and 500 MHz)**



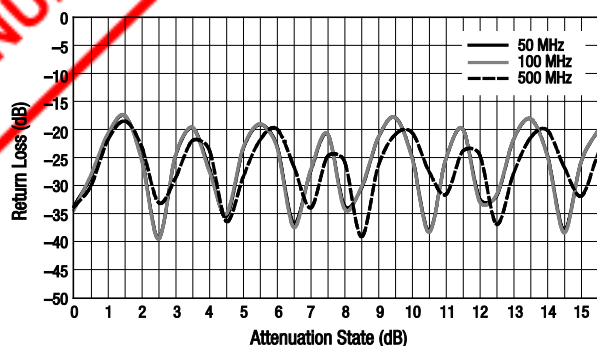
**Figure 10. Attenuation Error vs Attenuation State (@ 1000, 1500, and 2000 MHz)**



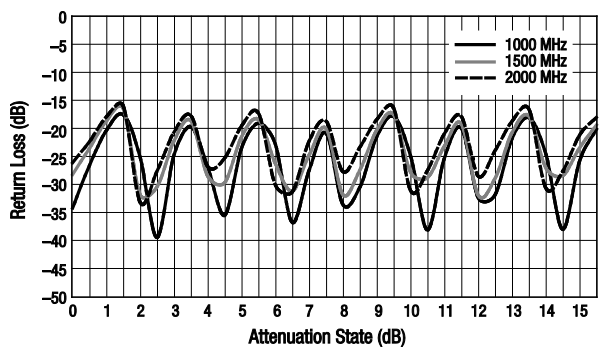
**Figure 11. Attenuation Step vs Attenuation State (@ 50, 100, and 500 MHz)**



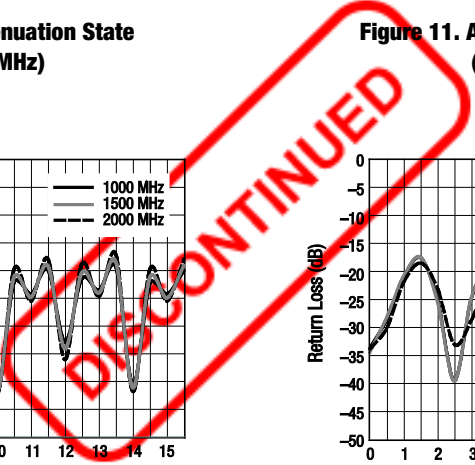
**Figure 12. Attenuation Step vs Attenuation State (@ 1000, 1500, and 2000 MHz)**



**Figure 13. Return Loss vs Attenuation State (@ 50, 100, and 500 MHz)**



**Figure 14. Return Loss vs Attenuation State (@ 1000, 1500, and 2000 MHz)**



**Table 6. SKY12340-364LF Truth Table**

J1 to J2 Attenuation	Reset	Serial Data Input				
		0.5 dB	1.0 dB	2.0 dB	4.0 dB	8.0 dB
Insertion loss	1	0	0	0	0	0
0.5 dB	1	1	0	0	0	0
1.0 dB	1	0	1	0	0	0
2.0 dB	1	0	0	1	0	0
4.0 dB	1	0	0	0	1	0
8.0 dB	1	0	0	0	0	1
15.5 dB	1	1	1	1	1	1
Insertion loss	0	X	X	X	X	X

**Note:** "1" =  $V_H = +1.7\text{ V to }+5\text{ V}$ . "0" =  $V_L = 0\text{ to }+0.6\text{ V}$ . "X" = don't care. This Table shows the logic required for the major bits and full attenuation. Bit states need to be used in combination to set the sum of the bits selected.

### Evaluation Board Description

The SKY12340-364LF Evaluation Board is used to test the performance of the SKY12340-364LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 15 and an Evaluation Board schematic diagram is shown in Figure 16. Table 7 provides the Evaluation Board Bill of Materials (BOM) list.

The Evaluation Board includes the required charge pump capacitor between pins 30 and 31. It also includes the negative voltage holding capacitor required from pin 28 to ground.

A capacitor is added to pin 31 to ground any noise on the DC supply line.

### Package Dimensions

The PCB layout footprint for the SKY12340-364LF is shown in Figure 17. Typical case markings are noted in Figure 18. Package dimensions for the 32-pin QFN are shown in Figure 19, and tape and reel dimensions are provided in Figure 20.

### Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY12340-364LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

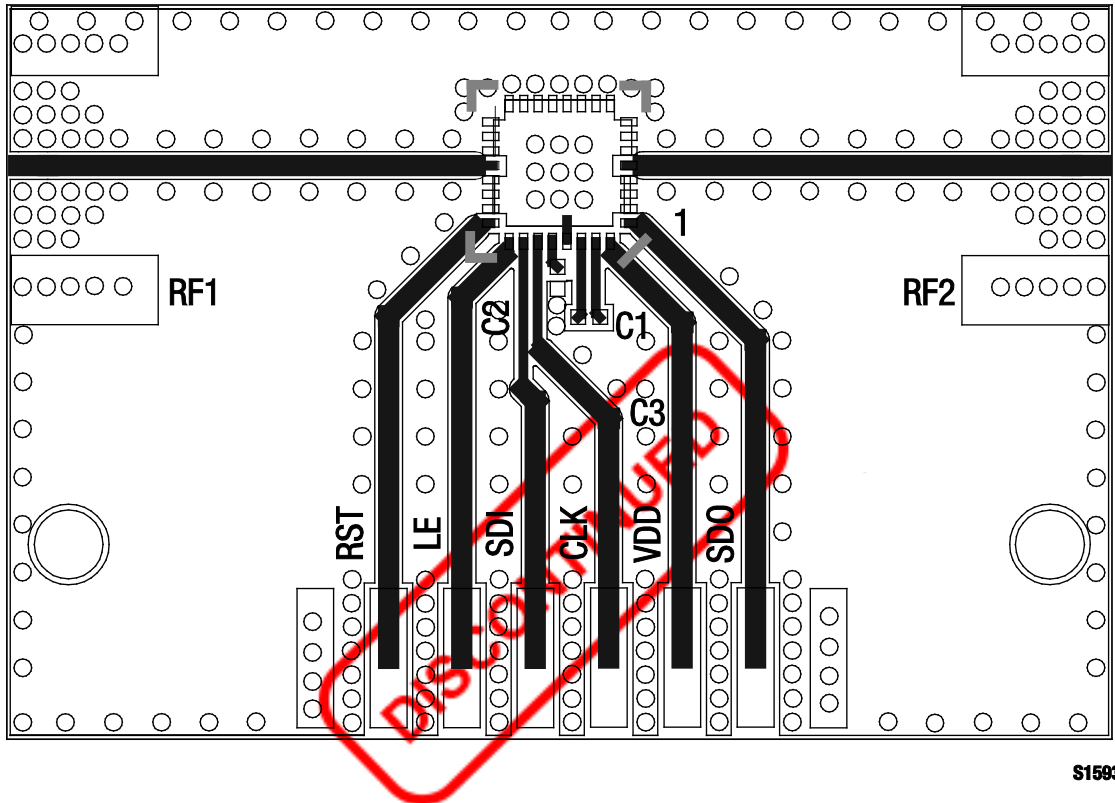
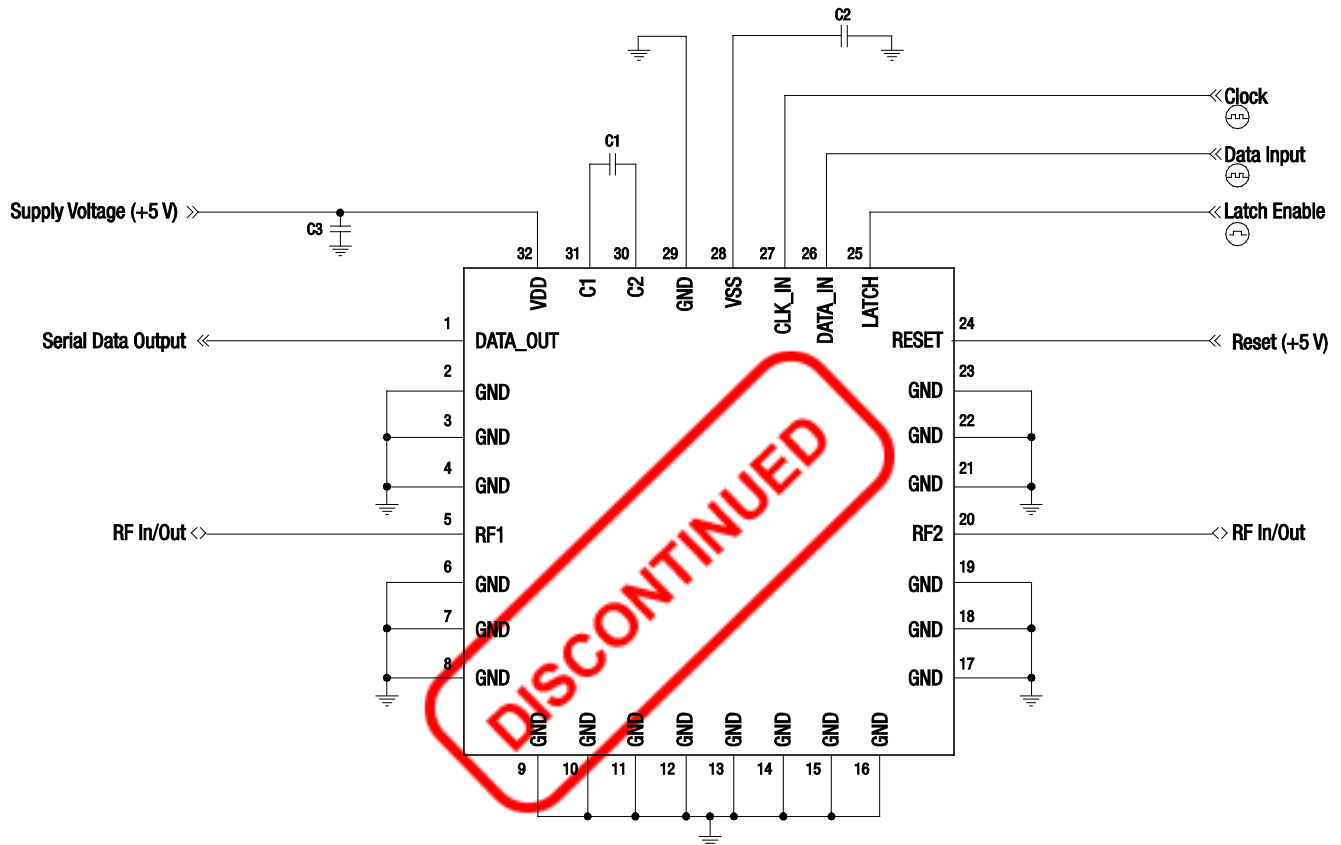


Figure 15. SKY12340-364LF Evaluation Board Assembly Diagram





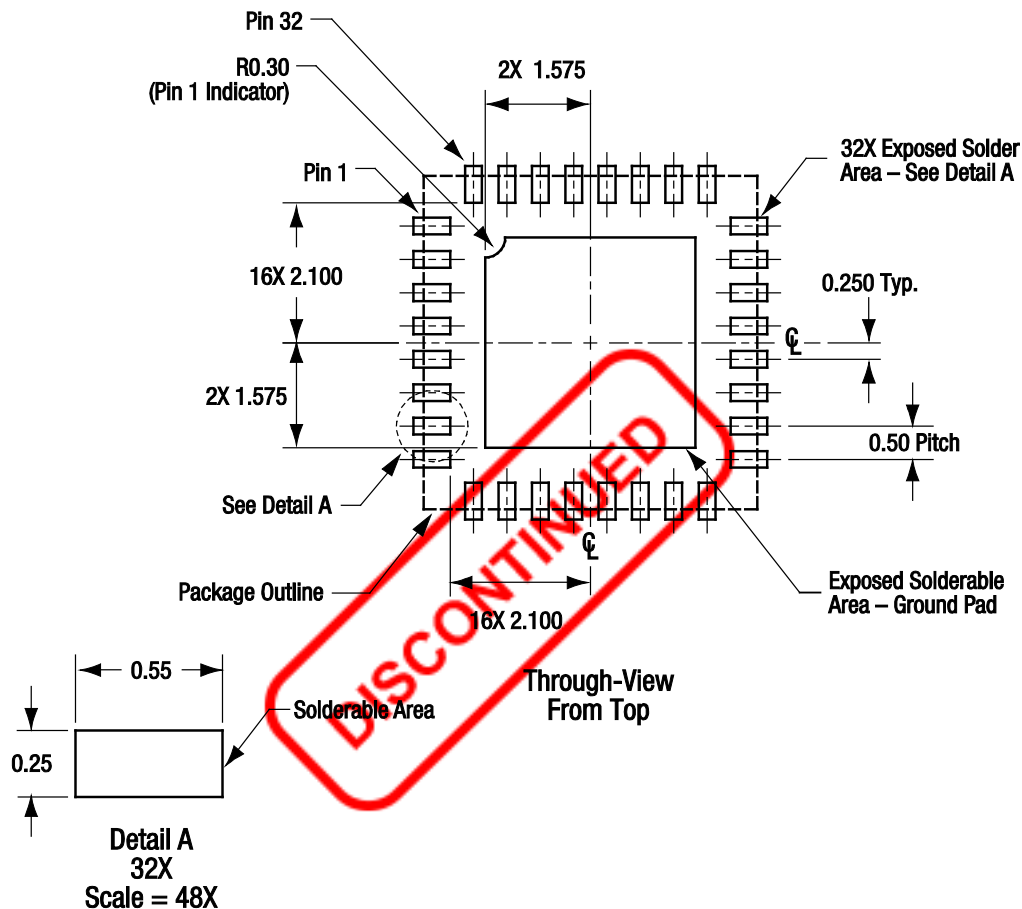
NOTE: Exposed bottom pad must be grounded

S1592

Figure 16. SKY12340-364LF Evaluation Board Schematic Diagram

Table 7. Recommended Evaluation Board Bill of Materials

Component	Value	Size	Manufacturer
C1	0.025 $\mu$ F	0402	Murata
C2	0.01 $\mu$ F	0402	Murata
C3	0.01 $\mu$ F	0402	Murata



All measurements are in millimeters

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Figure 17. SKY12340-364LF PCB Layout Footprint

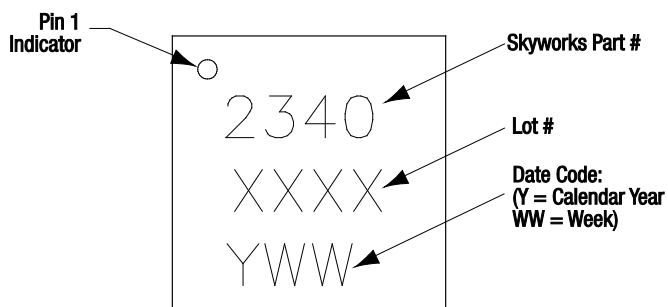
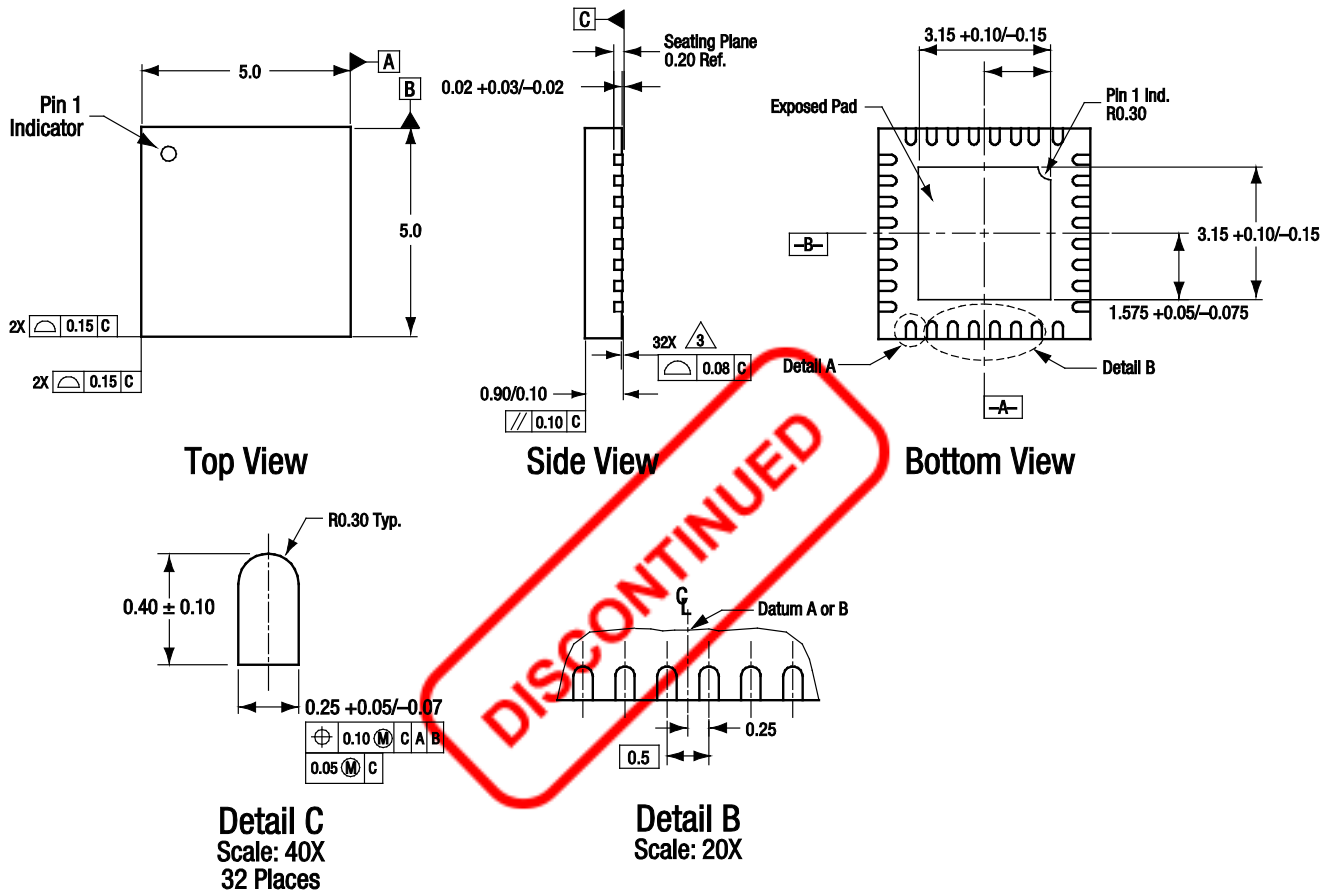


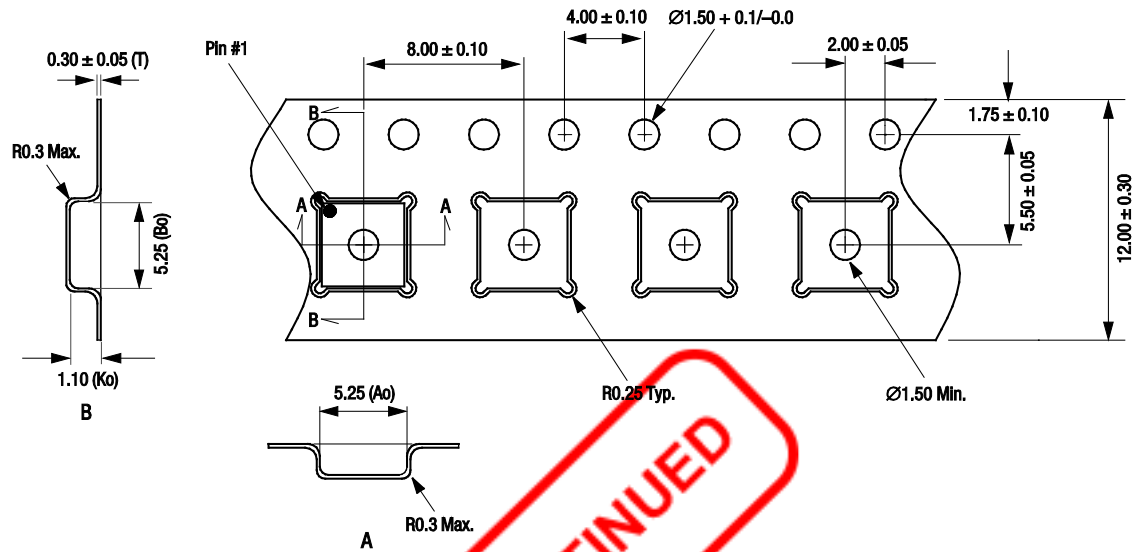
Figure 18. Typical Part Markings



All measurements are in millimeters.  
 Dimensioning and tolerancing according to ASME Y14.5M-1994.  
 Coplanarity applies to the exposed heat sink slug as well as the terminals.  
 Plating requirement per source control drawing (SCD) 2504.

S1583

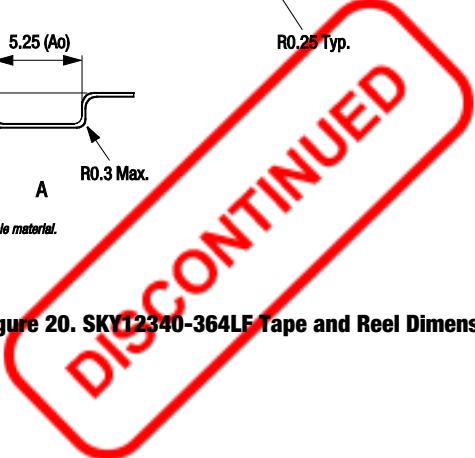
Figure 19. SKY12340-364LF 32-Pin QFN Package Dimensions



- Notes:
1. Carrier tape: black conductive polystyrene, non-bakeable material.
  2. Cover tape material: transparent conductive HSA.
  3. Cover tape size: 9.20 mm width.
  4. All measurements are in millimeters.

S1602

Figure 20. SKY12340-364LF Tape and Reel Dimensions



**Ordering Information**

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY12340-364LF Digital Attenuator	SKY12340-364LF	SKY12340-364LF-EVB



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