

# DATA SHEET

# SE2442L: 902 to 928 MHz High-Power RF Front-End Module

## **Applications**

- Smart meters
- In-home appliances
- Smart thermostats

## **Features**

- Integrated PA with +30 dBm output power
- Receive pass-through
- Integrated antenna switching
- Single-ended 50  $_{\Omega}$  Tx and Rx RF interface
- Fast turn-on / turn-off time < 1  $\mu$ sec
- 2.0 V to 4.8 V supply operation
- Sleep mode current < 1  $\mu$ A
- 4 x 4 x 0.9 mm 24-pin QFN
- Small QFN (24-pin, 4 mm x 4 mm x 0.9 mm) package (MSL1, 260°C per JEDEC J-STD-020)



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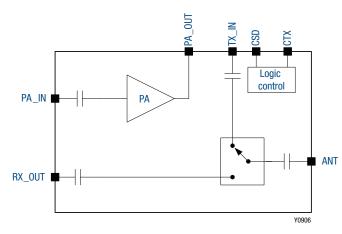


Figure 1. SE2442L Block Diagram

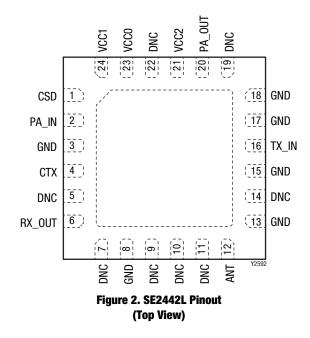
## **Description**

The SE2442L is a high-performance, integrated RF front-end module designed for high-power ISM band applications operating in the 902 to 928 MHz frequency band.

The SE2442L is designed for ease of use and maximum flexibility, with fully matched 50  $\Omega$  input and output, and digital controls compatible with 1.6 to 3.6 V CMOS levels.

The RF blocks operate over a wide supply voltage range from 2.0 to 4.8 V, allowing the SE2442L to be used in battery powered applications over a wide spectrum of the battery discharge curve.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



## Table 1. SE2442L Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	CSD	Shutdown control input	13	GND	Ground
2	PA_IN	PA input	14	DNC	Do not connect
3	GND	Ground	15	GND	Ground
4	СТХ	Transmit enable control input	16	TX_IN	Tx signal to antenna switch (from OMN)
5	DNC	Do not connect	17	GND	Ground
6	RX_OUT	Receive signal to transceiver or SoC	18	GND	Ground
7	DNC	Do not connect	19	DNC	Do not connect
8	GND	Ground	20	PA_OUT	PA output (to OMN)
9	DNC	Do not connect	21	VCC2	Positive power supply, transmit section
10	DNC	Do not connect	22	DNC	Do not connect
11	DNC	Do not connect	23	VCC0	Positive power supply, receive section
12	ANT	Antenna port	24	VCC1	Positive power supply, transmit section
			Paddle	GND	Exposed die paddle; electrical and thermal ground (connect to PCB ground)

# **Electrical and Mechanical Specifications**

The absolute maximum ratings of the SE2442L are provided in Table 2. The recommended operating conditions are specified in Table 3, and electrical specifications are provided in Tables 4 through 6.

The state of the SE2442L is determined by the logic provided in Table 7.

## Table 2. SE2442L Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage receive	VCCO	-0.3	5.5	V
Supply voltage transmit – no RF	VCC1, VCC2	-0.3	5.5	V
Control pin voltages		-0.3	VCC0	V
Operating temperature	Top	-40	+85	°C
Storage temperature	T <sub>stg</sub>	-40	+125	°C
Tx input power at PA_IN port	PIN_Tx_MAX		+10	dBm
Rx input power at ANT port	PIN_Rx_MAX		+10	dBm
Electrostatic discharge:	ESD			
Human Body Model (HBM)			1000	V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

#### **Table 3. Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Ambient temperature	Та	-40	+25	+85	°C
Supply voltage on VCC0, VCC1, and VCC2	Vcc	2.0	3.6	4.8	V

(400 - 5.0  s) is $-725$ 0, as measured on the realization board [be-linbeduce to the bevice], oness otherwise						
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
TX supply current	Ісс_тх30	$\begin{array}{l} \mbox{Tx mode } P_{0UT} = +30 \mbox{ dBm} \\ \mbox{CSD} = \mbox{CTX} = \mbox{high}, \mbox{VCC} = 4.8 \mbox{ V} \end{array}$		420		mA
TX supply current	Icc_tx27	$\label{eq:started} \begin{array}{l} \mbox{Tx mode } P_{\mbox{OUT}} = 27 \mbox{ dBm} \\ \mbox{CSD} = \mbox{CTX} = \mbox{high}, \mbox{VCC} = 3.6 \mbox{ V} \end{array}$		280		mA
Quiescent current	Іса_тх	No RF CSD = CTX = high		50		mA
RX supply current	ICC_RXBYPASS	Rx bypass mode CSD = HIGH, CTX = 0 V			280	μA
Sleep supply current	ICC_OFF	No RF, $CTX = CSD = 0 V$		0.05	1	μA

Table 4. SE2442L Electrical Specifications: DC (Note 1)(VCC = 3.6 V, TA = +25 °C, as Measured on the Evaluation Board [De-Embedded to the Device], Unless Otherwise Noted)

Note 1: Performance is guaranteed only under the conditions listed in the above table.

## Table 5. SE2442L Electrical Specifications: Logic Characteristics (Note 1)

## (TA = +25 °C, as Measured on the Evaluation Board [De-Embedded to the Device], Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Logic input high voltage	Vih		1.6		VCCO	V
Logic input low voltage	VIL		0		0.3	V
Logic input high current	Ін				1	μA
Logic input low current	lı.				1	μA

Note 1: Performance is guaranteed only under the conditions listed in the above table.

Table 6. SE2442L Electrical Specifications: AC Characteristics (Note 1) (VCC = 3.6 V, TA = +25 °C, as Measured on Evaluation Board [De-Embedded to the Device], All Unused Ports Terminated with 50  $\Omega$ , Unless Otherwise Noted)

Transmit (Tx)         Frequency range       FIN         Output power at ANT port       Pout_FE         PA power added efficiency       PAE         Small signal gain       S21         Small signal gain variation       ΔS21         Output return loss       S22ANT         2nd harmonic       HD2         3rd to 10 <sup>th</sup> harmonics       HD3 to F         Turn on time       T <sub>ON</sub> Stability       STAB	M VC VC VC PC 9C 9C	VCC = 4.8 V VCC = 4.0 V VCC = 3.6 V VCC = 3.0 V Pout = +28 dBm at PA_OUT port, 915 MHz V02 to 928 MHz	902	- 31.5 30.0 29.0 27.5 64	928	MHz dBm dBm dBm
Output power at ANT portPout_FEPA power added efficiencyPAESmall signal gainS21Small signal gain variation $\Delta$ S21Output return lossS22ANT2nd harmonicHD23rd to 10th harmonicsHD3 to HTurn on timeTONTurn off timeTOFF	M VC VC VC PC 9C 9C	ICC = 4.0 V ICC = 3.6 V ICC = 3.0 V ICC = 3.0 V Pout = +28 dBm at PA_OUT port, 915 MHz	902	30.0 29.0 27.5	928	dBm dBm dBm
PA power added efficiency     PAE       Small signal gain     S21       Small signal gain variation     ΔS21       Output return loss     S22ANT       2 <sup>nd</sup> harmonic     HD2       3 <sup>rd</sup> to 10 <sup>th</sup> harmonics     HD3 to H       Turn on time     TON       Turn off time     TOFF	M VC VC VC PC 9C 9C	ICC = 4.0 V ICC = 3.6 V ICC = 3.0 V ICC = 3.0 V Pout = +28 dBm at PA_OUT port, 915 MHz		30.0 29.0 27.5		dBm dBm
Small signal gain     S21       Small signal gain variation     ΔS21       Output return loss     S22 <sub>ANT</sub> 2 <sup>nd</sup> harmonic     HD2       3 <sup>rd</sup> to 10 <sup>th</sup> harmonics     HD3 to H       Turn on time     T <sub>ON</sub> Turn off time     T <sub>OFF</sub>	90 Ga			64		dBm
Small signal gain variation $\Delta S_{21}$ Output return loss $S22_{ANT}$ $2^{nd}$ harmonic       HD2 $3^{rd}$ to $10^{th}$ harmonics       HD3 to H         Turn on time $T_{ON}$ Turn off time $T_{OFF}$	Ga	02 to 928 MHz		04		%
Output return loss     S22 <sub>ANT</sub> 2 <sup>nd</sup> harmonic     HD2       3 <sup>rd</sup> to 10 <sup>th</sup> harmonics     HD3 to H       Turn on time     T <sub>ON</sub> Turn off time     T <sub>OFF</sub>			20			dB
2 <sup>nd</sup> harmonic     HD2       3 <sup>rd</sup> to 10 <sup>th</sup> harmonics     HD3 to H       Turn on time     ToN       Turn off time     TOFF	In	ain variation across frequency range			1	dBp-p
3 <sup>rd</sup> to 10 <sup>th</sup> harmonics     HD3 to H       Turn on time     ToN       Turn off time     TOFF		nto 50 $\Omega$ , ANT port		-10	-6	dB
Turn on time     ToN       Turn off time     TOFF	Po	Pout = +27 dBm, CW			-22	dBc
Turn off time T <sub>OFF</sub>	HD10 Po	Pout = +27 dBm, CW			-72	dBc
	Fr	rom 50% of CTX edge to 90% of final RF output power			1	μs
Stability STAB	Fr	rom 50% of CTX edge to 10% of final RF output power			1	μs
	tability STAB $\begin{array}{c} CW, P_{IN} = +6 \text{ dBm} \\ 0.1 \text{ GHz} - 20 \text{ GHz} \\ Load VSWR = 6:1 \end{array}$		ated outputs			
Ruggedness RU	CV	W, Pout = 27 dBm into 50 Ω, Load VSWR = 10:1	No permanent damage			
Receive (Rx) (Note 2)						
Frequency range fin			902		932	MHz
Antenna port return loss S11 <sub>ANT</sub>	Int	nto 50 $\Omega$ , ANT port		-10	-6	dB
Turn on time T <sub>ON</sub>	Fr	rom 50% of CTX edge			1	μs
Turn off time T <sub>OFF</sub>	Fr	rom 50% of CTX edge			1	μs
Gain in bypass mode G_bp	CT	CTX = logic '0' and CSD = logic '1'		-0.7		dB
Input 1-dB compression point in bypass mode IP1dB	CT	TX = logic '0' and CSD = logic '1'	10			dB
Antenna Functions						
Insertion loss from TX_IN to ANT Tx_ANT	90	002 to 928 MHz	-	0.7	-	dB
Insertion loss from ANT to RX_OUT Rx_ANT		002 to 928 MHz				r

 $\label{eq:Note1:Performance} \textbf{Note 1:} Performance is guaranteed only under the conditions listed in this table.$ 

Note 2: Receive section can operate with VCC0 = 2.8 V and VCC1 = VCC2 = 0 V

## Table 7. SE2442L Logic Controls

(TA = +25 °C)

Mode	Description	CSD	СТХ
0	All off (sleep mode) (Notes 1 and 3)	0	0
1	Rx or Tx bypass mode (Notes 1 and 2)	1	0
3	Tx mode (Notes 1 and 2)	1	1

Note 1: Logic '0' level compliant to  $V_{_{\rm IL}}$  as specified in Table 5.

Note 2: Logic '1' level compliant to  $V_{\mu}$  as specified in Table 5.

Note 3: All controls must be at logic '0' in order to achieve the specified sleep current.

## **Evaluation Board Description**

The SE2442L Evaluation Board is used to test the performance of the SE2442L front-end module (FEM). An Evaluation Board schematic diagram is provided in Figure 3. A photograph of the Evaluation Board is shown in Figure 4. A Bill of Materials (BOM) for the Evaluation Board is provided in Table 8.

#### **Evaluation Board Setup Procedure**

## **Connect Supply**

- 1. Connect J9, J10, and J11 to 50  $\Omega$  instruments. Terminate all unused ports (if applicable) with 50  $\Omega$ .
- 2. Connect the supply ground to Pin 1 of the J4 header.
- 3. Connect the DC power supply (2.0 to 4.8 V) to pin 2 of the J4 header.
- Refer to Table 7 for information about selecting the required RF path.

#### Measure TX Performance

Apply an RF signal to connector J10 (PA\_IN) to monitor the 900 to 930 MHz amplifier performance. Monitor the output power on connector J9 (ANT).

#### Measure RX Performance

Apply an RF signal to connector J9 (ANT) to monitor the 900 to 930 MHz RX path performance. Monitor the output signal on connector J11 (RX\_OUT).

*CAUTION:* Care should be taken not to overdrive the amplifier by applying too much RF on the input to the device. A suitable starting input power for the device is -20 dBm.

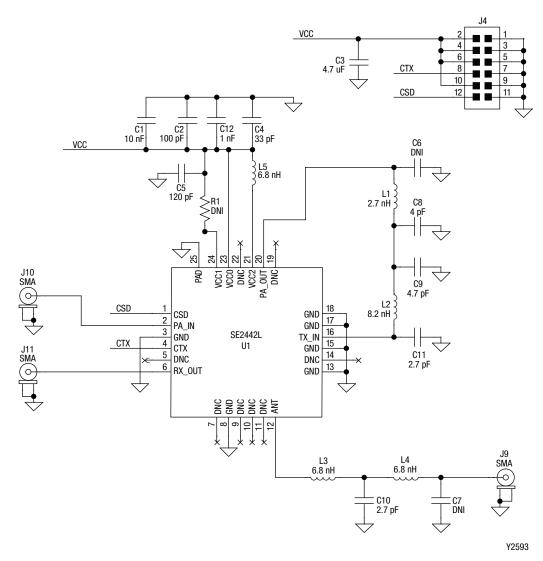


Figure 3. SE2442L Evaluation Board Schematic

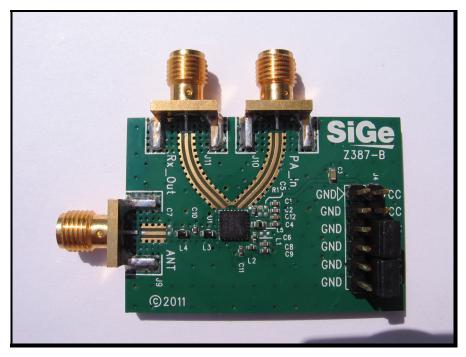


Figure 4. SE2442L Evaluation Board

#### Table 8. SE2442L Bill of Materials (BOM)

Component	Value	Manufacturer	Mfr Part Number	Package Size	Description
C1	10 nF	Murata	GRM155R71E103KA01	0402	Multilayer ceramic
C2	100 pF	Murata	GRM1555C1H101JZ01	0402	Multilayer ceramic
C3	4.7 uF	Murata	GRM188R60J475KE19	0402	Multilayer ceramic
C4	33 pF	Murata	GRM1555C1H330JZ01	0402	Multilayer ceramic
C5	120 pF	Murata	GRM1555C1H121JA01	0402	Multilayer ceramic
C6, C7	DNI			0402	Multilayer ceramic
C8	4 pF	Taiyo-Yuden	UMK105CG040CW	0402	Standard multilayer ceramic capacitor
C9	4.7 pF	Murata	GRM1555C1H4R7CZ01	0402	Multilayer ceramic
C10, C11	2.7 pF	Murata	GRM1555C1H2R7CZ01	0402	Multilayer ceramic
C12	1 nF	Murata	GRM155R71H102KA01	0402	Multilayer ceramic
J1, J2, J3	SMA	Johnson Components	142-0701-851	End launch	SMA end launch straight jack receptacle - tab contact
J4	6x2	Samtex	TSW-106-07-G-D	100 mil	100 mil header
L1	2.7 nH	Murata	LQG15HN2N7S02D	0402	Inductor
L2	8.2 nH	Murata	LQG15HN8N2J02D	0402	High frequency multilayer
L3, L4, L5	6.8 nH	Murata	LQG18HN6N8S00D	0603	High frequency multilayer
PCB1		Skyworks	Z387-B		РСВ
R1	DNI			0402	Do not install
U1		Skyworks	SE2442L	QFN400x400	900-930 MHz High Power RF FEM

# **Package Dimensions**

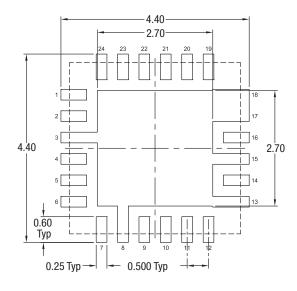
The PCB layout footprint for the SE2442L is provided in Figure 5. A typical part marking diagram is shown in Figure 6. Package dimensions are shown in Figure 7, and tape and reel dimensions are provided in Figure 8.

# **Package and Handling Information**

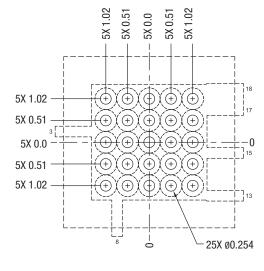
Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperatures during solder assembly.

The SE2442L is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C, and can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



**Board Metal** 



Via Pattern (Note 4)

0.20 Typ

4.40

0.500 Typ

Stencil Pattern (Note 5)

64% Solder Coverage

on Center Pad

\_

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-1.00 Typ

16

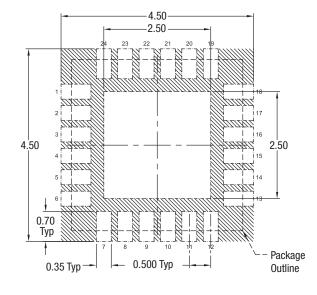
15

14

1]13

1.00 Typ

20 Typ



## Solder Mask Pattern (Note 6)

#### Notes:

- 1. All dimensions are in millimeters.
- 2. Interpret dimensions and tolerances per ASME Y14.5M-1994.
- 3. Unless specified, dimensions are symmetrical about center lines.
- 4. Via hole recommendations:
- 0.025 mm Cu via wall plating (minimum), via hole to be filled with conductive paste and plated over.
- Stencil recommendations: 0.125 mm stencil thickness, laser cut apertures, trapezoidal walls and rounded corners offer the best paste release.
- 6. Solder mask recommendations: Contact board fabricator for recommended solder mask offset and tolerance.

Y2596

#### **Figure 5. PCB Layout Footprint**

4.40

0.60

Тур

0.25 Typ

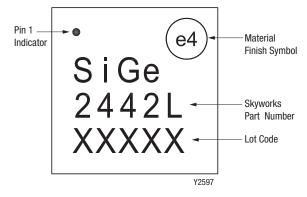
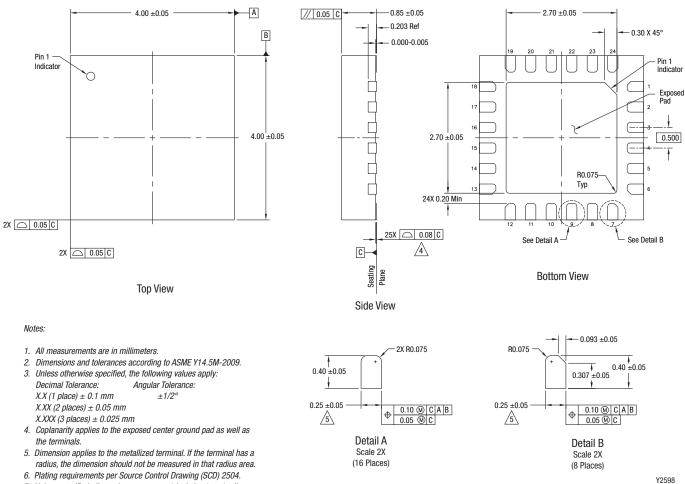
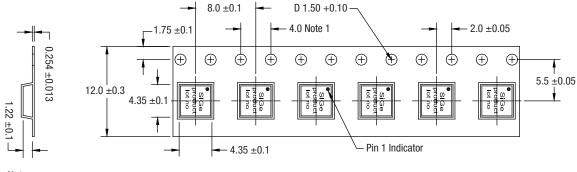


Figure 6. SE2442L Typical Part Marking



7. Unless specified, dimensions are symmetrical about center lines.





Notes:

1. 10-Sprocket hole pitch cumulative tolerance  $\pm 0.2$ .

2. Camber in compliance with EIA-481.

Y0086

#### Figure 8. SE2442L-R Tape and Reel Dimensions

## **Ordering Information**

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SE2442L: 902 to 928 MHz Front-End Module	SE2442L	SE2442L-EK1

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