Will CMOS Amplifiers Ever Kick-GaAs? (Invited)

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***Abstract*- In this paper, we present a discussion and comparison of CMOS and GaAs HBT technologies for handset power amplifiers. Our perspective is unique to other comparisons in that we actually have products in both technologies. To understand the application space where each of these technologies makes sense, we discuss current and near-term PA requirements as well as technology and technology support issues. Finally, we aim to dispel some the common misperceptions surrounding these technologies.**

I. Introduction

While CMOS has made inroads to many power amplifier (PA) applications such as Bluetooth®[1], CMOS PAs for wireless handsets have, seemingly, been the Holy Grail for quite some time. For years, there have been press releases and papers touting the latest and greatest CMOS PA that was going to "Kick GaAs"[2-4]. While there has been good market penetration of CMOS PAs for GSM/GPRS applications, such as Skyworks' line of distributed transformer (DAT)-based CMOS PAs, CMOS still faces challenges in being broadly deployed in the handset space (in particular, for linear applications).

In this presentation, we discuss customer (handset manufacturers) and technology considerations that have led to this current state, and some of the customer-desired features that allow us to reconsider the role of CMOS in some power amplifier modules (PAMs) in the future. We have previously discussed opportunities for BiCMOS[5] – where some of the same challenges remain - but here focus on comparing GaAs HBT or BiFET technologies to CMOS technologies. In addition to the functionality trends, we discuss some of the technology characteristics and components (such as focus on RF modeling, reliability, and design kits), currently enjoyed by GaAs designers, which are generally afterthoughts in a foundry CMOS process. While we restrict this discussion to amplifiers for wireless handset applications, many of the considerations are also applicable to other mobile systems such as wireless LAN. The demonstration of more competitive CMOS PAs will rely heavily on circuit design techniques to overcome technology short-comings and leverage the functionality that can be implemented in these technologies. In the meantime, GaAs technologies are not standing still and we discuss HBT technology trends designed to address upcoming handset needs.

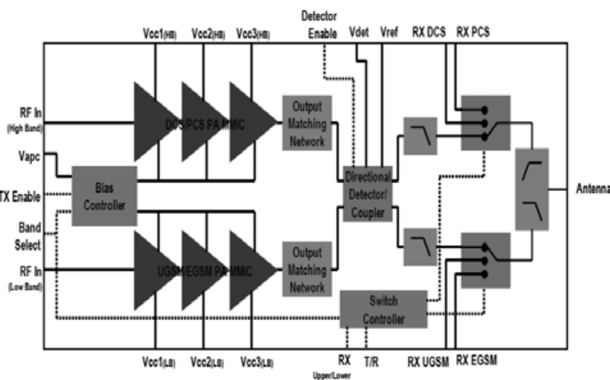

Fig. 1. Block diagram of a multi-mode PA

II. Why Does Anyone Want a CMOS PA Anyway?

Before we compare the technologies, let's consider what the lure is for CMOS PAs. First, in high-volume production, the wafer costs for "base", or vanilla, CMOS are low and continually declining. There is large capacity available from foundries, eliminating the need for owning the wafer fabrication facility and providing flexibility to easily follow up and down market trends. From a design perspective, non-PA components (such as controllers, transceivers, and switches) can readily be integrated with the PA, if desired. The availability of millions of transistors, and different types of transistors, allows the addition of performance enhancing functionality, including complex bias circuitry and well-established ESD design procedures. Finally, CMOS allows integration of on-chip calibration and self-test circuitry that is not possible in III-V technologies[6]. However, there are challenges in designing CMOS PAs: Low breakdown voltage, lower device gain (for devices that are more rugged), linearity issues, design/manufacturing support issues, RF model inaccuracies, lack of high-voltage capacitors, through wafer vias, or semi-insulating substrate are among the technical challenges. At the product level, CMOS can have higher development costs and take longer time[7]. The use of short L_{eff} devices (for gain, integration) drives higher mask costs and compensating the design for a non-PA process increases complexity. The ability to overcome these challenges will largely determine *where* CMOS PAs fit into the PA landscape. At the same time, GaAs technologies have become more feature-rich with the addition FETs to most commercial HBT processes, allowing III-V designers the ability to address some market requirements unattainable with bipolar-only technologies[8]

III. PA Module Trends

A. Multi-mode, Multi-band

Multi-band (specifically quad-band) phones are already in existence (there are many quad-band GSM PAs already on the market). A typical block diagram is shown in Fig. 1. We observe that there are multiple PAs, matching networks, and switches that allow selection between the transmitting PAs and the receive ports. For a PA manufacturer, the dream scenario is multiple PAs and one or more switches. Unfortunately, continuous pressure to reduce module size makes this solution impractical in the long term. It is important to note that CMOS is already part of this solution

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(usually used for the bias controller and perhaps some switching functions) and for multi-mode leveraging this may allow for a simpler, hybrid solution, similar to what has been done with BiCMOS[9]. The downside of this integration, for CMOS, is that CMOS PA designs tend to be large due to the heavy use of inductors or transmission lines (even if they replace passive components). The real hurdle for CMOS is going to be whether or not it can sufficiently address the linear PA requirements, which are currently being implemented in GaAs HBT, which we will discuss later.

Besides the PA technology, to achieve a true multi-mode, multi-band phone in a minimum size, switching or tunable output matching functions become critical needs. For tunability, there are several different technologies for (MEMs, ferroelectric capacitors, and high-Q varactors) that may be viable competitors. MEMs have demonstrated a number of devices (switches, capacitors, etc). While the laboratory demonstrations of these devices are impressive, there are still practical questions related to using them in cellular handsets. Among these are cost, reliability, packaging, and requirement for additional support circuitry. For ferroelectric capacitors, the advantages are: simple packaging and good power handling capability, and fast tuning time. The disadvantages are the trade-offs to get high power and high Q at the same time, relatively narrow tuning range, and high control voltages. Finally, some novel varactor topologies have recently been demonstrated [10] which may also provide a suitable solution for tunable networks.

B. *Mid-power Efficiency*

In contrast to saturated PAs (like GSM) where the power is constantly being adjusted and controlled, in "linear" PAs (e.g. WCDMA), there is a great deal of emphasis placed on techniques that yield the lowest overall current consumption by the PA. In particular, the efficiency at mid-power is a very important specification from handset manufacturers. This requirement is being addressed through both design topologies (quasi-Doherty [12]) and through technologies that allow by-passing of one or more PA stages [13]. For III-V semiconductor technologies, stage by-passing creates some interesting opportunities/challenges. Some of the challenges and trade-offs for various integration strategies have been previously discussed [14] and will be briefly reviewed in the presentation. In CMOS technologies, these power control functions can be implemented in various ways and have been demonstrated in lower power transceivers [15]. Besides the technical challenges, cost and reproducibility are major factors. In the context of a PAM, when a switching function is desired it also requires accompanying logic circuits (switch controller in the figure). Thus, a technology that integrates the logic functions within the switching chip is desirable (and is already obtainable in silicon technologies) [15] and can also lead to lower overall size because of reduced board routing requirements. For III-V technologies, this means that an integrated HBT-FET technology ideally includes E/D mode FETs [16, 17] to be competitive if the circuit yield can be managed. One of the remaining challenges, for GaAs, will be obtaining low enough current draw, for the logic circuits, to rival silicon technologies. As discussed in the previous section, DC-DC converters can be used to obtain similar efficiency improvements and can be directly integrated on CMOS [18] but care must be taken for noise isolation. A final concern is determining what technologies (or technology nodes) will be sufficient to do this switching if the power distribution curves (how often the PA transmits a given power) are modified [19].

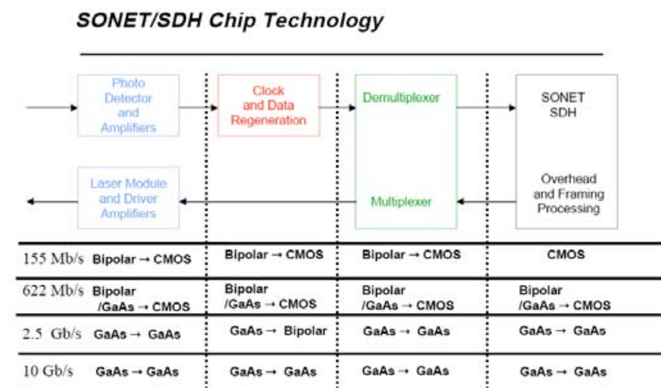

Fig. 2. Example of product evolution for lightwave circuits

Load-insensitivity is another challenging requirement. Phone manufacturers are asking PA vendors to develop modules that are not sensitive to the load that the PA module sees. Previously, the major requirement was that the PA should be robust enough to withstand the voltage standing wave ratio (VSWR) withstood the VSWR when the isolator was removed. The current challenge is to meet performance specifications (e.g., noise, linearity, and PAE) over the same VSWR condition. The responses to this challenge will be varied and place differing demands on the selected technology. The ruggedness challenge presented by this operating mode for linear CMOS PAs will be most likely addressed by circuit design, rather than technology.

C. *Ultra-low Cost Market*

Perhaps the greatest near term opportunity for CMOS PAs lies in the ultra-low cost market that has emerged. This market has several aspects that favor a CMOS PA implementation. The standard is well established (GSM/GPRS), so the specifications will not change (so development time is not an issue) as they often do in other standards, the market is large and well defined, so the risk and cost of development is relatively low, and the premium is on cost, rather than best performance. GaAs technologies have actually come a long way from being an "exotic" technology so the cost of in-house fabricated GaAs HBTs, although not on par with CMOS is still quite competitive overall[1].

IV. TECHNOLOGY IMPROVEMENT OPPORTUNITIES

While there is no doubt that CMOS is the undisputed king of semiconductors, using a process designed for digital applications for PA design is challenging and usually requires something different than "base" CMOS. There are several

basic requirements for fabricating PAs. The ideal CMOS PA process would include: high-breakdown CMOS devices – not just for PA but also because the biasing must see the battery/charger (and the charger is higher voltage than the battery). Keep in mind that this is opposite to the trend of lower supply voltage for the rest of the CMOS used in the system (baseband and transceiver portions). It should have at least two very thick (1-2um) layers of copper for routing source/drain currents that can be extremely high during mismatch operation, high voltage capacitors (for matching), and better controlled/higher quality passives. The details of these considerations will be presented at the conference.

Since most foundry customers are designing digital or analog-mixed signal circuits, the modeling and characterization infrastructure reflects this and the resulting models are not adequate for designing high-power PAs. In particular, the device characterization, if you are lucky, provides s-parameters, with little or no large-signal information provided. In the rare event the foundry does support RF models[20], the compact models have evolved slowly for RF, let alone large-signal use. For example, the popular BSIM model has well known convergence issues at large signals and is discontinuous through zero which makes it difficult to accurately simulate power amplifiers. For the design of PAs – using large FETs- it becomes very critical to simulate the feed structures for the PA [21, 22]. For GaAs HBT technology, since they are mainly used for PA applications, the emphasis is on modeling the devices up to large-signal operation. In addition, EM simulation is routinely used and easily supported because of the semi-insulating substrate. These techniques for simulation are also leveraged at the package level since, for PA products, the package is part of the circuit.

Another very important support issue when dealing with external foundries is RF reliability considerations, or "What are the allowed device operating conditions for RF applications?" Foundries generally specify a safe-operating area (SOA) defined by DC bias conditions only (and applicable to digital and analog applications). What is really needed, for PA designers, is an SOA that is related to RF voltage waveforms for both short-term reliability (ruggedness) and long-term reliability (wear-out). While CMOS DC reliability is very well understood, the failure modes for PA applications are different enough that they require special attention. One major disconnect is that the relationship between DC and RF reliability is not well understood (or at least not published) so designers are at a loss to make device selection decisions based on the limited information from foundries, usually at the cost of performance. Therefore, long-term reliability testing is pushed back to the foundry user and includes extensive circuit level reliability validation, further delaying product introduction. While companies that already have the infrastructure to do both device (to speed up the design process) and circuit level reliability for PAs can absorb this work into existing infrastructure, this is a difficult task for smaller companies that lack these support functions.

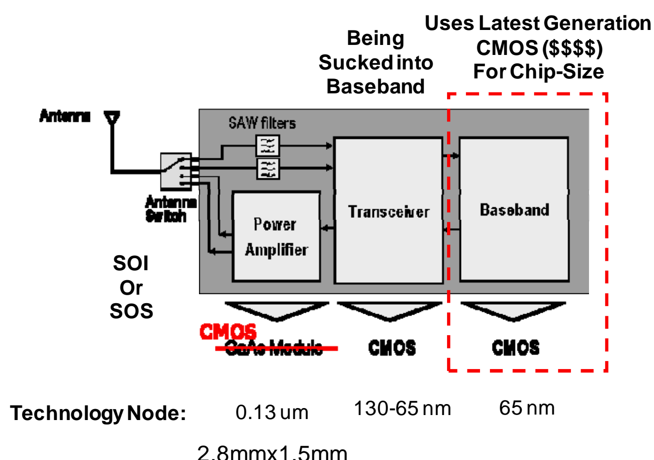

Fig. 3 – Example of technologies used and system partitioning for handset technologies

V. What do CMOS designers do to work around these issues?

Some of the technology limitations we mentioned earlier are things that, if CMOS is to be used, need to be solved by design methodologies since there is little motivation for foundries (unless partnered or captive) to develop PA specific CMOS processes. Some of the proposed ways of dealing with low breakdown voltage devices are: lower the supply voltage with DC-DC convertors[18], cascode or transistor stacking[23], use a complimentary class E topology to divide voltage[24], use distributed transformers (DAT) to decrease Vdd at device[25], or just exceed the safe operating limit (not really an option except for nice publications). The use of DC-DC convertors reduces the overall efficiency because of loss in the convertor. Also, even though the voltage is lowered, a certain amount of output power must be delivered (specified by customer), so the currents will be higher introducing a host of other issues. In general, designers pick higher breakdown voltage transistors with their accompanying low gain, to achieve better ruggedness (or to deal with the reliability rules discussed above). This requires different circuit topologies to achieve higher gain and include using positive feedback[26] or a mode-locked oscillator[14]. However, these solutions are narrow-band and the gain and PAE change with frequency (PA must work over a band, not single point!). Traditional PA topologies require large transistors with a high gate capacitance. This capacitance is absorbed into the input match, requiring high Q inductor and reasonable control of the gate oxide thickness if yields are to be high. The Axiom/Skyworks DAT solves many of these issues by providing a reduced Vdd and reduced array sizes by distributing the transistors[25].

VI. Conclusion

While there is no disputing that you can build CMOS PAs for certain markets, there are still several obstacles that need to be overcome for it to become the technology of choice for general handset PAs. Probably the most critical are the

turn-around time, development cost, and optimum performance compared to III-Vs. This is a familiar, but not identical, situation for CMOS if we recall the development of light wave circuits in the mid to late 1990s (see Fig. 2)[27]. The strategy for these infrastructure products (i.e. you win it, you are in it) was to first gain market entry using a higher performance technology, then eventually migrate it to lower cost technologies as their performance improved. Perhaps we will see a similar evolution in handset PAs. The other long term question is if a fully integrated solution is desirable for customers. Consider Fig. 3 that shows a block diagram from the antenna to baseband. Note that different technology nodes are employed for the different blocks. This creates a fundamental problem in product design since, if you integrate it all, someone is paying too much for their real estate and the development times for the different blocks are very different. Finally, for companies designing CMOS PAs, there are several key support functions – modeling and reliability – that must be done in-house, diminishing some of the advantage of using the foundry anyway. Perhaps this is one of the reasons that all major PA players either own their own fab or have a captive process in a foundry.

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