Effects of Ohmic Metal on Electrochemical Etching of GaAs in pHEMT Manufacturing

Kezia Cheng

Skyworks Solutions Inc., 20 Sylvan Road, Woburn, MA 01801 kezia.cheng@skyworksinc.com (781) 241-2821

Keywords: Ohmic Metal, Contact Resistance, Electrochemical, Galvanic, Erosion

Abstract

Good ohmic metal contact is crucial for optimum device performance for Heterojunction Bipolar Transistors (HBT) and pseudomorphic High Electron Mobility Transistors (pHEMT). Erosion of Gallium Arsenide (GaAs) adjacent to ohmic structure is a common problem and it is generally observed in the compound semiconductor industry. It is believed that electrochemical etching, which has been studied extensively by researchers, is responsible for the phenomenon. Solutions usually focus around the chemistries in the various wet processing steps. In our recent experiments, we have found that galvanic erosion of GaAs can be suppressed or eliminated by optimizing the ohmic metal scheme and alloy condition. This paper will discuss the correlation between ohmic metal composition and electrochemical etching. The improvement in DC and RF parameters as a result of better ohmic contact and lack of erosion will also be presented.

INTRODUCTION

Our standard ohmic metal comprised of E-beam evaporated Ni/Au/Ge/Au. The metal stack is alloyed into the semiconductor at 435ºC for early generation pHEMTs. Contact resistance (R_{cont}) measured immediately after ohmic metal liftoff and alloy is typically very low at around 0.08 Ω-mm. However when R_{cont} is measured again further down stream after several liftoff and clean steps, the value has typically increased by as much as two fold, an indication of some loss of N-doped GaAs during the processes. Scanning Electron Microscopy (SEM) inspection revealed signs of electrochemical etching, which explained the degradation of R_{cont}. See Fig1.

When exposed ohmic metal is present in close proximity to the bare GaAs surface, this electrochemical reaction is known to have caused channel and gate etch uniformity issues and degrade device performance [1]. The pitted surface can trap wet chemistries under passivation nitride and cause reliability issues.

The standard ohmic metal scheme was developed for early generations of pHEMTs with a cap layer doping concentration of 5 E 18 /cm3. This metal scheme has served well in our devices. However, galvanic erosion of GaAs adjacent to ohmic metal is almost always present. The early development work was done with erosion taken into consideration. Since erosion is not a controlled process, the severity varies. Too much erosion will result in a drop in Idss and the opposite will increase gate leakage. Neither extreme is desirable.

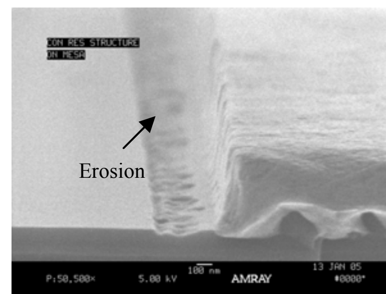

Figure 1 Erosion of N-doped GaAs adjacent to ohmic metal

The advancements in cell phone technologies demand higher degrees of integration and tighter performance specifications. It is clear that we need to minimize or eliminate this undesirable erosion variable in order to achieve good yield on new devices and to reach a higher level of performance.

In the process flow of pHEMT and HBT manufacturing, there are many wet processing steps in which the ohmic metal is exposed to the solutions. DI H_2O in the NMP, dissolved oxygen in the DI water, HCl and NH_4OH pre clean steps can all accelerate the electrochemical etching action. [2][3]. Photo-electrochemical effects further enhance the reactions. Replacing all wet steps and processing in complete darkness as a measure to eliminate erosion is not a practical approach.

To better understand the role the ohmic metal plays in this galvanic erosion, experiments were conducted here at Skyworks to study the relationship between micro phase formation in the ohmic metal and electrochemical reaction. Scanning Electron Microscopy (SEM) was used to inspect surface morphology and perform qualitative analysis of erosion. Wafers with three different ohmic metal grain compositions were analyzed using Focused Ion Beam (FIB) sectioning. Scanning Transmission Electron Microscopy (STEM) and Energy Dispersive X-ray (EDX) were used for

grain composition identification. Finally, DC and RF circuit results of wafers run with the new and the standard ohmic metals were analyzed and presented.

EXPERIMENTAL PROCEDURE

The experimental lot consisted of six wafers with Skyworks PHES6 material, which has a AlGaAs/InGaAs/AlGaAs pHEMT structure with a cap layer doping concentration of 1 E 18 /cm3. The six wafers were split into three groups of two wafers. Group A and B were E-beam evaporated Ni/Ge/Au with an overall thickness of about 1500A. Group C was the control and received the standard ohmic scheme having a final thickness of over 4000A. After lifting off the unwanted metal in NMP, the wafers were alloyed in a Rapid Thermal Annealing (RTA) tool at different conditions. See Table 1. R_{cont} measurements were done on the Transmission Line Model (TLM) structures. With the exception of ohmic metal deposition and alloying steps, the six wafers traveled together from start to circuit test, and therefore were subjected to the same wet chemistries and process conditions.

Group A, New Ohmic	380ºC, 10 sec
Group B, New Ohmic	420ºC, 45 sec
Group C, Control	415ºC, 200 sec

Table 1 Alloy temperature and time of experiment

The wafers were inspected at post-gate test using Scanning Electron Microscopy (SEM) to compare the GaAs surface adjacent to ohmic metal pads. FIB/STEM was used to inspect the different phases that exist in the metal/semiconductor interface. EDX was employed to determine the chemical compositions of each phase.

RESULTS AND DISCUSSION

Contact Resistances

The R_{cont} data for the three wafer groups are given in Table 2

	Pregate R_{cont} (Ω-mm)	Post gate R_{cont} (Ω-mm)	PCM R_{cont} (Ω-mm)
Group A, New Ohmic	0.21	0.47	0.76
Group B, New Ohmic	0.18	0.23	0.25
Group C. Control wafer	0.17	0.27	0.40

Table 2 R_{cont} of ohmic metal to 2DEG

Pregate

Measured at pregate, Group A had an R_{cont} of 0.21 Ω-mm with a wide distribution. The wafers are considered to be slightly under-alloyed. Group B, while having the same metal stack as Group A, had a lower R_{cont} value of 0.18 Ω-mm with a longer alloy time and a higher alloy temperature. The difference in R_{cont} between these two groups can be attributed solely to the alloy condition. Group C had a similar R_{cont} of 0.17 Ω-mm as Group B although Group C had a wider distribution.

SEM inspection of the six wafers at this stage revealed no obvious sign of any erosion but with markedly different surface morphology. Group A had a smooth morphology with speckles sparsely distributed throughout the entire ohmic surface. The gray speckles were determined to be NiGe phase using EDX. Group B had a textured appearance with pronounced grains and slight dendrites. EDX analysis confirmed the presence of NiGeAs phase in the alloyed ohmic metal. Group C had a smooth morphology similar to Group A but without the NiGe speckles. The alloyed ohmic metal retained the as deposited columnar structure.

Post gate

By post gate PCM, the wafers had gone through three additional NMP steps with DI H_2O rinse and one NH_4OH dip. The R_{cont} of Group A wafers had increased sharply to 0.47 Ω-mm and the R_{cont} of the control wafers had risen to 0.27 Ω-mm indicating that some loss of material adjacent to the ohmic metal in the TLM structure had developed. In comparison, Group B had a small increase in Rcont to 0.23 Ω-mm. The contact resistance of Group C had a 59% increase over the pregate value to 0.27 Ω-mm.

SEM inspection of Group A wafers at this stage showed definite trenching of GaAs around ohmic metal. See Fig 2. The degree of trenching was proportional to the ohmic metal size. More aggressive erosion was associated with increasing ohmic metal geometry. No discernable loss of GaAs material was observed in Group B; see Fig 3. Group C, Fig 4, exhibited the same kind of erosion as Group A although the increase in Rcont for this group is less than the former.

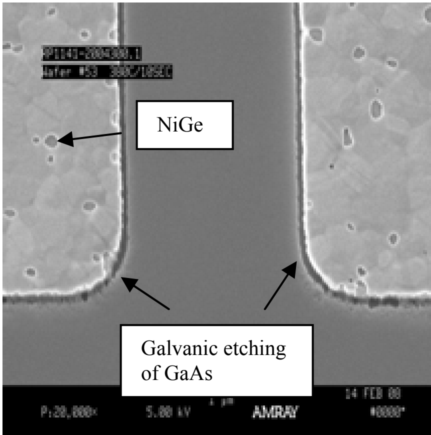

Figure 2 Group A. New ohmic alloyed at 380C, 10sec.

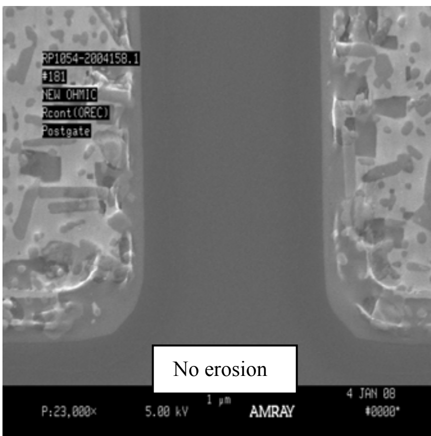

Figure 3 Group B. New Ohmic. 420C alloy, 45sec.

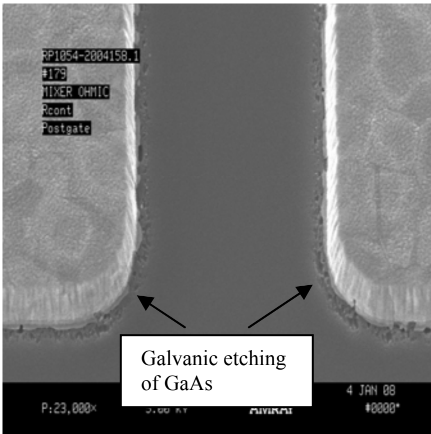

Figure 4 Group C. Standard ohmic. 420C, 200sec alloy.

DC PCM

R_{cont} of the control wafer had gone up further to 0.40 Ω-mm at PCM test, which is 150% increase over the pregate value. Group B had virtually the same R_{cont} as it did at post gate. This suggested that there was little erosion with the additional round of NMP and ammonia dip. Group A had the worst R_{cont} of the three samples at PCM with the R_{cont} increased over 3.5 times over its original value.

Between Post gate and DC PCM tests there were two descum steps and one NH_4OH dip step before the metal was covered under nitride. Once the wafers were passivated, erosion should cease as the GaAs surface was not exposed to wet chemistry anymore. Therefore the degradation of contact resistance seen at DC PCM can be attributed to the descum and NH_4OH clean.

STEM/EDX analysis

Fig 5 depicts a STEM cross sectional image of the standard ohmic metal alloyed at 415ºC taken in ZC mode. The ohmic metal had a semi-homogenous appearance and grains formed at the metal/semiconductor interface. The alloy depth reached the InGaAs channel and there were only Au and Au compounds near the surface of the ohmic metal. EDX was used to identify the composition of the four different grains.

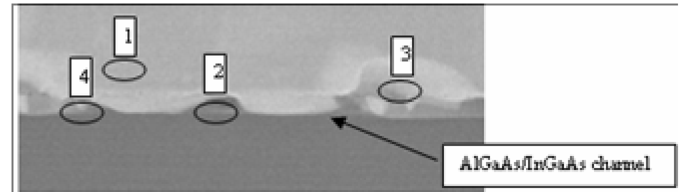

Figure 5 STEM image of standard ohmic

The Noran system used in the EDX analysis employs the Metallurgical and Biological Thin Film Sections (MBTS) Model. This algorithm makes corrections based on derived relative elemental sensitivity factors. The calculation is made without absorption correction as these factors need to be considered more with thicker specimens. Due to the thickness of the FIB membrane (~1500A), it is possible that the EDX data might pick up signals from overlapping grains from within the FIB membrane. As such, only a semi-quantitative data of the chemical composition of the grain is assured.

Site 1 was found to be Au only. Site 2 had a composition of NiGe with inclusion of As. Site 3 atomic make up was Ni, Ge and As with a composition close to Ni_2Ge_2As. Due to the high thickness of Au and a thin layer of Ge, most of the Ni and Ge are trapped close to the surface of GaAs. Above about 2KA from the GaAs surface, the ohmic metal formed a homogeneous film containing only AuAs and Au with Ga and As inclusions.

Figure 6 Group A. New ohmic. 380C, 10sec

A FIB/STEM image of a Group A wafer with the new ohmic metal and 380ºC 10sec alloy is shown in Fig 7. Due to the short alloy time, the metal did not penetrate very deeply into the semiconductor. The ohmic metal contains NiGe and NiAs phases, indicated at site 15 and 17 respectively. Similar to the control sample, the metal has an abundance of Au phases.

A STEM image of Group B with the new ohmic and alloyed at 420ºC for 45 second is shown in Fig 7. It had a markedly different grain structure compared to the standard ohmic wafer with clear phases distributed throughout the entire ohmic metal. The dark regions are NiGeAs in roughly the composition ratio of Ni_2Ge_2As where the brighter regions are Au.

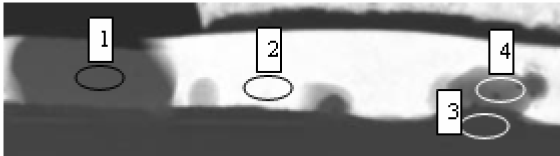

Figure 7 STEM image of new ohmic (Group B)

Previous research had found that the reaction at the Ni/Ge/Au and GaAs interface go through different stages as alloy temperature and time increase [4]. In early stages of alloying, Ni and As diffuse to form NiAs. Some Ni reacts with Ge to form NiGe phase. There is also out diffusion of Ga and As. Some Au diffuses into the substrate. The main phases in the ohmic metal at this stage are NiAs, NiGe and Au containing grains.

As the alloy temperature and time move into the optimal regime, NiAs and NiGe phases transition into NiGeAs phase. The presence of NiGeAs phase is known to be responsible for low ohmic contact resistance. Further alloying will result in the growth of Au containing grains, thereby reducing the ratio of NiGeAs to Au at the interface. Consequently R_{cont} increases with additional alloy time.

Alloyed Ni/Ge/Au ohmic metal does not result in a homogeneous film but rather different phases with different grain compositions [5]. Although having similar contact resistance after ohmic metal alloy, the three groups have very different R_{cont} when measured at DC PCM. SEM inspection of the GaAs surface adjacent to ohmic metal showed that they react differently to electrochemically induced etching. Group C wafers, which is the control, have high ratio of Au phases to NiGeAs phase. This group has definite signs of erosion. Group B wafers have a high proportion of NiGeAs phase and there is no discernable erosion. Test results supported the observation. Group A, although having the same metal stack as Group B, had a very different grain structure. By under-alloying the ohmic metal, an abundance of Au containing phases resulted. These wafers displayed the same kind of erosion pattern as the control wafers.

Erosion Theory

When a metallized GaAs wafer is immersed in an electrolytic solution, such as NMP, electrochemical reaction could take place. The electrochemical reaction comes about if there is a difference in work function between the metal and semiconductor. The potential barrier height is determined by the difference in work functions between metal and GaAs. Noble metals such as Au have a larger barrier height than NiGeAs. The electrochemical reaction at the metal semiconductor junction can be modeled by a series of cells made up of Au, NiGeAs, NiAs and NiGe connected in parallel. The rate of reaction will be dependent on the proportion of the active cell (Au) to cells with lower potential difference. The new ohmic metal with optimized alloy contained a high proportion of NiGeAs grains; consequently, the electrochemical reaction caused by the metal was minimal. On the other hand, both the control and Group A had a high ratio of Au grains in the alloyed metal, considerable erosion therefore resulted.

We can theorize, also, that depending on the property of NiGeAs, a potential difference can exist between Au and NiGeAs phases. The resultant electrochemical reaction between two different adjacent grains will reduce the rate of reaction on the GaAs surface, thereby suppressing the GaAs erosion.

Using the same model, a large ohmic pad is capable of producing more current and a lightly doped GaAs will have a higher potential difference and therefore more aggressive reaction. This is consistent with the observation that erosion is more pronounced off mesa, around a large ohmic structure than on mesa next to a small ohmic feature.

Test Parameters

Engineering splits fabricated with the new ohmic metal showed a difference in DC and RF parameters. Splits were done with alternating serial number to negate any unintentional effects at certain processing steps that require splitting the lot. Odd serial number wafers had the

optimized new ohmic metal stack with 420ºC 45 second alloy time. Even serial number wafers were the control with standard mixer ohmic and alloy.

Table 3 DC and RF test data

	Ron	Leakage (Ig)	3rd Harmonic
Control	4.6 Ohms	0.67 uA	67.53 dBc
New ohmic	4.3 Ohms	0.86 uA	70.29 dBc

Since there was no change to the gate etch or deposition processes in the split experiments, it is unexpected to observe the new ohmic wafers having over 29% higher gate leakage current.

Based on the SEM analysis of the GaAs surface and the R_{cont} values, we can conclude that there is little to no erosion of the GaAs material including the gate ledge. As a result, the leakage current is expected to be higher for the new ohmic wafers. It is difficult to quantify the increase in leakage due to a lack of erosion because the leakage mechanisms in a pHEMT are often complicated and involve several inter-related factors. More work is being done to better understand the exact cause of the higher DC leakage associated with the new ohmic metal.

One of the challenges of the new generation of pHEMT devices is harmonics. Keeping series and parasitic resistance low is critical to improving RF performance of a pHEMT. The new ohmic wafers on average have 4dBc better 3rd harmonic over control. Low series resistance due to better ohmic contact can be attributed to the difference. The better 3rd harmonic opens more process options to improving the Inter-Modulation Distortion (IMD), which, in our device, is often a trade off with harmonics.

CONCLUSIONS

The experiment has established a relationship between electrochemical erosion of GaAs and the type of grain present in the ohmic metal. Results of the investigation work demonstrated that Au and Au compounds are primarily responsible for the galvanic erosion of GaAs. Ohmic metal with an excessive amount of Au and non-optimized Ni to Ge ratio will result in an abundance of Au containing grains. An ohmic scheme with an optimal Ni:Ge:Au ratio can be made to have similar grain structure as the standard ohmic by under alloying.

More work will be done to determine if the lack of erosion seen on the optimized ohmic (Group B) is due to a weaker potential difference between NiGeAs micro-phase and GaAs. A potential difference can also exist between Au phase and NiGeAs phase within the ohmic metal, thereby further reducing the reaction on the GaAs surface.

More aggressive erosion is observed off mesa than on mesa. This is due to the difference in doping concentration with off mesa having a smaller work function. Large ohmic structures have more erosion than smaller features.

New ohmic with optimized alloy condition has lower R_{cont} due to a lack of erosion. Better ohmic contact to the 2DEG results in lower Ron. Reducing series resistance improved harmonics. Wafers processed with the new ohmic metal have significantly higher circuit yield.

ACKNOWLEDGEMENTS

The author is indebt to Larry Hanes for his support and Skyworks Woburn Process Engineering, Product Development and Yield Engineering teams for their inputs and fruitful discussions; Leakhana Meas and Lannie Nguyen for their assistance in wafer test and Aparna Joshi for preparing the test data analyzed.

REFERENCES

[1] Y. Zhao, Y. Tkachenko, D. Bartle, Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1999
[2] M. Tsunotani, T. Ohshima, M. Sato, R. Shigemasa, T. Kimura, GaAs Mantech 1999.
[3] G. M. Metze, S. McPhilmy, P. Laux, IEEE Electron Device Letters, vol. 16, no, 1, January 1995.
[4] T.S. Kuan, P.E. Batson, T.N. Jackson, H. Rupprecht, E.L. Wilkie, J. Appl. Phys. 54 (12), December 1983
[5] T.S. Kuan, P.E. Batson, J.L. Freeouf, T.N. Jackson, E.L. Wilkie, Mat. Res. Soc. Symp. Proc vol. 54, 625 (1986).
[6] M. Shur, Compound Semiconductor Electronics, The Age of Maturity

ACRONYMS

HBT: Heterojunction Bipolar Transistor
pHEMT: pseudomorphic High Electron Mobility Transistor
FIB: Focused Ion Beam
STEM: Scanning Transmission Electron Microscopy