Progress on Distributed Resistance Model for pHEMT

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Abstract—With increasing scale and complexity in pHEMT circuit and dimension shrinking in unit pHEMT devices, distributed effects are becoming more crucial than ever. During the design of amplifiers, precise prediction of the resistances of a device is vital to the simulation result due to the direct impact on impedance. This work reports a set of experiments utilizing different testing structures to reveal how a pHEMT device’s layout affects its gate-to-source/drain resistances due to distribution of resistance along electrodes and the consequent current crowding. As an example, a distributed resistance model of source-side gate bar is quantitatively analyzed. It is shown that the prediction of the model coincides with the measurement data obtained from a variety of testing devices with different numbers of gate fingers.

Keywords: GaAs pHEMT; gate resistance; distributed resistance; current crowding

I. INTRODUCTION

Accompanying the rapid development of wireless communication, design of amplifiers with better performance is becoming more critical and challenging than ever. The simulation accuracy of RF/microwave circuits depends heavily on the lumped model built for each transistor used, especially in prediction on impedances in amplifier designs [1]. With increasing periphery of devices used, the distribution of resistance along electrodes is becoming more and more phenomenal. As a consequence, the modeling method in the traditional lumped model, which treats gate resistance as a constant value, is losing its accuracy in the trend.

In this article, we employ a set of testing GaAs pHEMT devices with the same gate width of 1mm but different numbers of gate fingers, ranging from 10 to 20. A set of experiments are designed to measure the resistances between gate and source/drain terminals. By presenting experimental results, we show that the current crowding effect due to finite resistance of gate and source/drain electrodes significantly affects the total resistance between gate and source/drain terminals. We conclude that the gate configuration in layout can greatly affect these resistances based on a distributed resistance model established to explain the discrepancy observed during our experiment in an analytical form. As an example as well as verification, the model’s predictions on gate-source/drain resistances are compared with measurement data. It is found that the two sets of data match well and thereby validate the model.

II. TESTING STRUCTURES, EXPERIMENTS AND MEASUREMENT RESULTS

Pseudomorphic AlGaAs/InGaAs common-source HEMTs are used in this research. The epi-structure was grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. The pHEMTs are fabricated using a standard fabrication process with the same total gate width of 1mm but different gate finger numbers (10, 13, and 20) and corresponding unit gate widths (100um, 77um and 50um). The electrode metals are standard production alloys to form Schottky and Ohmic contacts. In each group of devices with the same gate number/unit gate width, three types of devices are processed and fabricated with everything identical except the position and orientation of gate electrodes, namely source-edge-gate, center-gate, and drain-edge-gate devices.

Figure 1. Three kinds of devices with different gate orientations and gate electrodes positions are employed in this work. (a) illustrates source-edge-gate device. (b) illustrates center-gate device. (c) illustrates drain-edge-gate device.

The source-edge-gate device has the gate electrode located closer to the source electrode, and a gate bar at the gate side. The gate-source access region is 1.2um in length. The center-gate device has the gate located right at the midpoint from the source electrode to the drain electrode, and a meandered gate going through. The drain-edge-gate device has the gate
electrode located closer to the drain electrode, and a gate bar on the drain side. The gate-drain access region is 1.2um in length. Figure 1 illustrates all three kinds on gate positions and orientations. In summary, there are nine kinds of testing devices in total with different combinations of gate positions and gate numbers.

The characterization process on each device follows the methods of Lee’s, Bennett’s and Cheng’s [2-4], and contains two measurements. In the first measurement, current is injected into gate with source grounded and drain floated. As a result, all current flows into the gate electrode and out of the source terminal. During the sweep of current, gate voltages are recorded. In the second measurement, the gate current sweep is performed with source floated. Values of gate-drain voltage drop are recorded instead.

![Figure 2](image_url)

**Figure 2.** Ig-Vg curves from six measurements on three 10-finger devices. C1000F10D_D and C1000F10D_S are data of the 10-finger drain-edge-gate device with drain and source floated respectively. C1000F10S_D and C1000F10S_S are data of the 10-finger source-edge-gate device with drain and source floated respectively. C1000F10C_D and C1000F10C_S are data of the 10-finger center-gate device with drain and source floated respectively. In all cases, Vg is the voltage drop across the two un-floated terminals.

![Figure 3](image_url)

**Figure 3.** Ig-Vg curves from six measurements on three 10-finger devices. C1000F13D_D and C1000F13D_S are data of the 10-finger drain-edge-gate device with drain and source floated respectively. C1000F13S_D and C1000F13S_S are data of the 10-finger source-edge-gate device with drain and source floated respectively. C1000F13C_D and C1000F13C_S are data of the 10-finger center-gate device with drain and source floated respectively. In all cases, Vg is the voltage drop across the two un-floated terminals.

After the gate-diode is forward biased, we can extract the total resistance between those two terminals between which the current flows from the slope of the linear part of the curve. This total resistance consists of the resistance of the corresponding part of channel, contact resistances, resistances of gate and source/drain terminals, and the resistance of the rest of metal layer in layout. On the same wafer, we fabricated TLM and other testing structures to extract the contact resistance and the sheet resistances of the channel, Schottky metal layer and Ohmic metal layer. Meanwhile, an analytical form of the total resistance is derived in consideration of distributed electrode resistances and current crowding. The measurement data from different kinds of testing structures are employed to validate the model. Measurement data is shown in Figure 2, 3 and 4.

![Figure 4](image_url)

**Figure 4.** Ig-Vg curves from six measurements on three 10-finger devices. C1000F20D_D and C1000F20D_S are data of the 10-finger drain-edge-gate device with drain and source floated respectively. C1000F20S_D and C1000F20S_S are data of the 10-finger source-edge-gate device with drain and source floated respectively. C1000F20C_D and C1000F20C_S are data of the 10-finger center-gate device with drain and source floated respectively. In all cases, Vg is the voltage drop across the two un-floated terminals.

**III. MODELLING APPROACH AND DISCUSSION**

From the measurement data presented in Figure 2, 3 and 4, we found an agreed trend in all three kinds of devices with different gate numbers. After an accordant turn-on voltage around 0.7V confirms that the gate diode is forward biased, the source-edge-gate device always has the lowest total resistances. Because the resistance in the gate-drain access region is larger than that in the gate-source access region, it is expected that the resistance measured with drain floated is a little bit less than that with source floated. However, if all devices employed the same gate orientation, the drain-edge-gate device would have the same values in resistances reading as the source-edge-gate device has, for the simple reason that the measurement settings of source-edge-gate device with drain floated are symmetric to that of drain-edge-gate device with source floated. The same symmetry applies in the measurement of the source-edge-gate device with source floated and the drain-edge-gate device with drain floated. Therefore, the gate orientation and the resultant change in resistance distribution are responsible for the discrepancy in resistances. As shown, this effect may even double the resistance under certain situations. When we take gate orientation into consideration, we can easily explain all our observations. The source-edge-gate device has the lowest resistance because all gate fingers are paralleled to each other. The drain-edge-gate device has higher resistances since all current has to travel through the first finger before it can reach the rest paralleled fingers. The meandered gate has the largest resistances as all current crowds in the only path. In other words, current has to go through the whole gate before it
reaches the furthest finger as there are no fingers in parallel at all. Please note that, although previous research [2] reveals a non-constant current factor in gate current because the current distribution in the part of channel beneath the gate changes, this factor should remain constant in this work as measurement data of source-edge-gate device forms very straight lines which indicate a constant resistance between the two un-floated terminals during these measurements.

Figure 5 shows schematic diagrams of two pairs of electrodes in a multi-finger source-edge-gate device and depicts the current paths in the floated source and the floated drain measurements respectively. Figure 5(a) shows a pair of gate and source electrodes, together with the source access region in between. Figure 5(b) demonstrates the gate-drain side of the same FET. In both cases, input gate current flows into the gate electrode from the left side. After traversing the source/drain access regions, gate current leaves the source electrode from the left side in the floated drain measurement and leaves the drain electrode from the right side in the floated source measurement. In both figures, \( R_c \) is the resistance per unit width of the corresponding part of the channel, including various contact resistances and channel resistances. \( R_g \) and \( R_s \) are the resistances per unit length of the gate electrode and the source/drain electrode. \( W \) is the unit length of a single gate finger. Please note the boundary conditions of these two cases are different due to their different gate orientations.

![Figure 5. Illustration of current paths in a source-edge-gate device. (a) demonstrates the floated source measurement and (b) demonstrates the floated drain measurement.](image)

According to Figure 5(a), we can establish the equation set as follows:

\[
\begin{align*}
V(x) &= \frac{dIe(x)}{dx} \\
\frac{dV(x)}{dx} &= -(R_g + R_s)Ie(x)
\end{align*}
\]  

(1)

After applying the boundary conditions

\[
\begin{align*}
Ie(0) &= I \\
Ie(W) &= 0
\end{align*}
\]  

(2)

We have

\[
V(x) = I \left[ \frac{R_g + R_s}{R_c} \frac{e^{\gamma(W-x)} - e^{-\gamma(W-x)}}{e^{\gamma W} - e^{-\gamma W}} \right]
\]  

(3)

And

\[
Ie(x) = I \frac{e^{\gamma(W-x)} - e^{-\gamma(W-x)}}{e^{\gamma W} - e^{-\gamma W}}
\]  

(4)

Where

\[
\gamma = \frac{R_s + R_g}{R_c}
\]  

This leads to an analytical form of total resistance as

\[
R = \frac{V(0)}{I} = \sqrt{\frac{R_s + R_g}{R_c}} \frac{e^{\gamma W} + e^{-\gamma W}}{e^{\gamma W} - e^{-\gamma W}}
\]  

(5)

Parameters such as \( R_s \), \( R_g \) and \( R_c \) can be extracted from TLM and other test structures. After we plug in these parameters and add in resistances of external components, such as that of the gate bar, we can acquire the total resistances between gate and source/drain by solving a finite resistance network. The modeling process is repeated for the cases of both measurements on all test devices with various gate numbers. The comparison between our model prediction and the measurement data are shown in Figure 6. The two sets of data match well with each other.

![Figure 6. Modelled total resistances in floated drain measurement on source-edge-gate devices of 10, 13 and 20 fingers.](image)

We can repeat this modeling approach on the drain side of the FET. This time, the equation set describing the current and voltage distribution is as follows:

\[
\begin{align*}
V(x) &= \frac{dIe(x)}{dx} \\
\frac{dV(x)}{dx} &= -(R_g + R_s)Ie(x) + R_sI
\end{align*}
\]  

(6)

Please note that although the boundary conditions on the drain electrode changes to the following,
From another perspective, it is interesting that (10) can be validated by a previous research on the impact of current crowding on insertion loss [5]. Although different terminals are focused in both models, the equation derived from the modeling procedure in [5] is a special case of (10) in which $R_g = R_d$ holds.

By establishing similar differential equation sets and corresponding boundary conditions and following this procedure, the total resistances in other cases can be derived as well [6]. At the same time, this procedure can be utilized in other applications when distributed impedance causes current crowding. In other words, layout of a device should be taken in consideration during its resistance modeling under certain circumstances. A carefully chosen layout topology may greatly change resistances between terminals.

IV. CONCLUSION

A distributed resistance model is proposed to calculate the total resistances between gate and source/drain terminals. In this article, analytical forms of resistances under two characterization exams on source-edge-gate FET are derived as examples. The model-predicted Ig-Vg curves coincide with our measurement data. Based on our observation and model, we conclude that layout plays a vital role in deciding resistance between terminals when distributed resistance changes current distribution and hence should be considered during circuit designs.

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REFERENCES