Distributed Switch FET Model that predicts Better Insertion Loss and Harmonics

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***Abstract*— With increasing scale and complexity in phemt switch circuits and dimension shrinking in unit phemt switch devices, distributed effects are becoming crucial on insertion loss and harmonics, especially the second harmonic. Distributed effects of metal resistances and inductances are taken into account in this paper. It is shown distributed effects either along the drain/source fingers or distributed effects along the lateral direction when the signal feeds are on the line ends have impact on frequency roll-off in insertion loss. The parasitic distributed effects especially those of gate fingers beyond the active region, on the other hand, have crucial impact on second harmonics. The new model is analytic and do not need any EM simulator, and therefore is easy to incorporate into large-signal model. The model was validated against various layout and structures in terms of frequency roll-off in insertion loss and the harmonic simulation for various sizes of phemt devices. Through simulation using the new model it is shown that more design guide as regarding to how to reduce insertion loss and 2nd harmonics have to be considered in switch circuit design.**

I. Introduction

For modern communications, design of PHEMT switch with very low insertion loss and high linearity performance is critical and challenging. [1,2] It is highly desired to have a comprehensive and accurate large-signal model to predict both small-signal and linearity for various gate-widths and gate-numbers and even layout of devices. With the requirement of low insertion loss at high power and lower harmonics, it is common to use large-periphery PHEMT devices, such as up to 3-4 mm periphery. For such high gate periphery, simple lumped device model can not account for distributed effects. Further more, to reduce the chip size, unit cells of phemt devices are keeping shrinking. For our recent phemt technology, the drain/source metal strips have been reduced to as small as 2.5um, so that the metal loss along the finger is no longer a small portion of on-resistance and its distributed effects must taken into account. Unfortunately, it is difficult to account for distributed effects. None of existing compact models, whatsoever, have taken into account any distributed effects. We have reported to use EM simulation to account for small-signal response of phemt switches, so called EMFET [3], it is fancy but time-consuming and can not use for large-signal simulation.

In this paper, we developed a distributed model to account for parasitic effects, including metal strip loss along drain/source fingers as well as the loss along the metal lines combing drain/source fingers. Also it has been a puzzle why lumped switch models can hardly useful to account second harmonics. Ideally, symmetric devices can not generate 2nd harmonics at all with high resistances on the gates. However, slightly external gate impedance provides favourite route to generate 2nd harmonics. One of the parasitics is the gate parasitic outside the mesa area. We also take into account gate parasitic effects.

While this work is dedicated to phemt switch device modelling, the model can be equally useful for any large devices that has distributed feature such as silicon SOI switch device.

II. Distributed Model of Metal Strips

For smaller device, the extrinsic parasitics can be considered as lumped elements. A typical on-state equivalent circuit is shown in figure 1, where Rs is the drain and source resistance including the contributions of extrinsic channel resistance contact resistance and metal resistance, Ls is metal inductance, Cs is metal to ground capacitance and Cds is the drain-source coupling capacitances. Normally the Ls and Cds can be calculated from EM simulation and we have generated those values as function of gate width W and finger number for SG-FET, DG-FET and TG-FET for a particular technology.

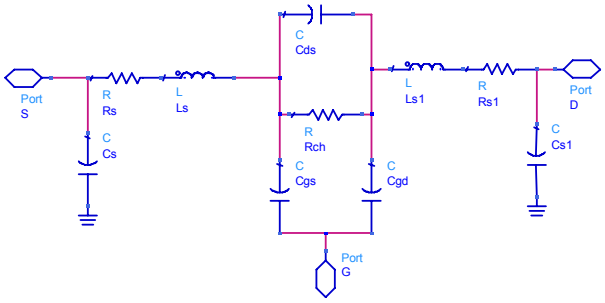


Figure 1. Conventional small-signal equivalent circuit, where Rch and Cgs/Cgd are functions of biases. For on state, Rch is small depending on Vg, for off state, Rch is very high and Cgs/Cgd is comparable to parasitic Cds.

For a lumped parasitic model, normally Cs and Ls values shown in the figure 1 are very small and Cds, Rch dominate the frequency response at on-state. Due to increasing shunting effect of Cds with frequency, the modelled small-signal S21 always shows a increasing insertion loss in contrary to the roll-off in real world. This discrepancy can only be solved by accounting for distributed effects. Figure 2 shows the diagram how we account for the distributed effects. In the diagram, the

metal line along the finger has an equivalent circuit with distributed line inductance Lo (nH/mm), line-to-ground capacitance Cso (pF/mm) and metal loss Ro (Ohm/mm). Between the drain line and source line there is distributed channel resistance Rs (Ohm/mm) connected to the virtual drain and source of device respectively.

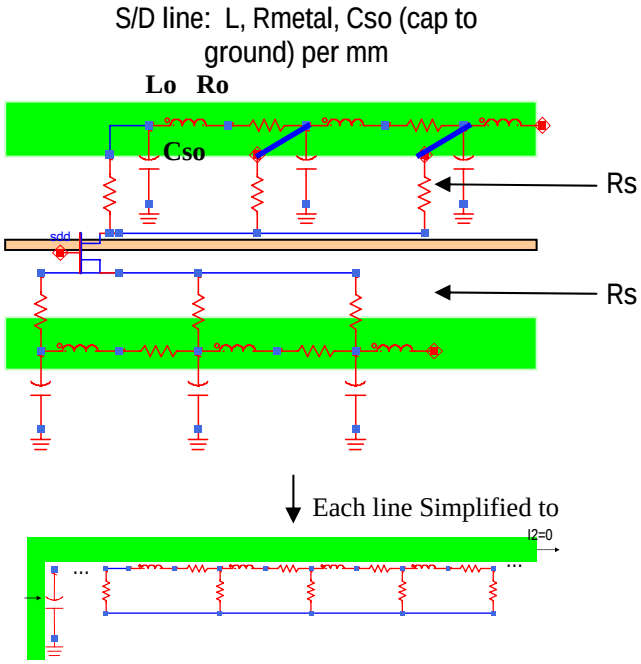


Figure 2. Distributed equivalent circuit of switch devices. The intrinsic Phemt is still regarded as lumped element. The distributed line-to-ground capacitances are then lumped into a capacitance per line.

The distributed impedance can be derived as follows. In the derivation, we set boundary condition of one side of the source line is excitation and the other end of the line is open, I_2=0. The same also applies to drain line, but the configuration is the reverse of the source line.

$$V_2 = V_1 \cosh(\beta * UW) - I_1 Zo \sinh(\beta * UW) \quad (1)$$
$$I_2 = -V_1 \cosh(\beta * UW) + I_1 Zo \sinh(\beta * UW) \quad (2)$$

Where UW is the length of finger

$$\beta = sqrt((\omega L + R_{metal})/R_s) \quad (3)$$
$$Zo = sqrt((\omega L + R_{metal}) * R_s) \quad (4)$$

For open finger at the other side, I_2=0. The impedance of one finger is:

$$Z_{\_1finger} = Zo / \tanh(\beta * UW) \quad (5)$$

where Rs and Rmetal are the source/drain channel resistance and metal resistance per unit length. For multi-finger devices, if the signal combines without phase difference at feed and output, we called as Cascade connection, the total impedance is Z= $Z_{\_1finger}/N_f$ where N_f is the total drain or source finger number. As regarding to calculation of L, Cso, it is simply from look-up table generated from EM simulation, with scaling factor of finger number. Rmetal is calculated from:

$$R_{metal} = \frac{\rho \cdot 1mm}{T0.5W_s} \quad (3)$$

where ρ is metal- gold resistivity and Ws, T is metal strip width and thickness. Here only a half of metal strip is considered, since the other half of strip is for the next drain/source multi-metal pair.

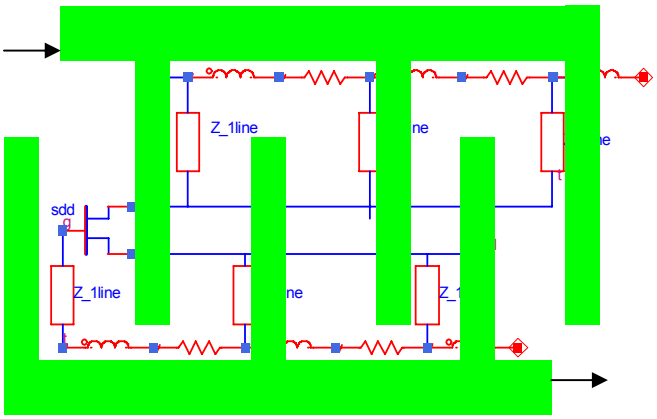


Figure 3. Equivalent circuit to account for the lateral distributed effect of combined fingers.

Similarly, we can derive the composite impedance for multi finger when the signal is fed along the combined line, as shown in figure 3, designated as tandem connection.

$$V_2 = V_1 \cosh(\beta_t * N_f) - I_1 Zot \sinh(\beta_t * N_f)$$
$$I_2 = -V_1 \cosh(\beta_t * N_f) + I_1 Zot \sinh(\beta_t * N_f)$$

where Nf is number of gate finger

$$\beta_t = sqrt((\omega L_{side} + R_{side})/Z_{\_1line})$$
$$Z_{ot} = sqrt((\omega L_{side} + R_{side}) * Z_{\_1line})$$

For open finger at the other side, I2=0. The impedance of one finger is:

$$Z_{tandem} = Z_{ot} / \tanh(\beta_t * N_f)$$

where Rside and Lside are the source/drain channel resistance and inductance per unit cell (one pair of drain/source finger).

The frequency-dependent element for distributed parasitics is implemented with linear SDD z2p model in ADS simulator and put it as a part of device model in netlist.

III. MODELING GATE PARASITICS OUTSIDE MESA

The second harmonics is highly dependent on layout. Normally it is hard to predict the 2nd harmonic without going to complicated

EM based large-signal simulation. However, one of the main sources of layout parasitic that impacts on 2nd harmonics is the gate parasitics outside the mesa area, as shown in figure 4. Basically, the parasitic gate capacitance to the ground contributed by the gate lines at turn-around outside the mesa area.

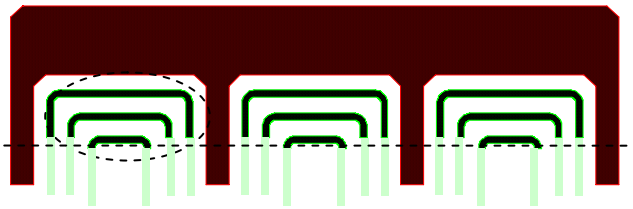


Fig.4 Parasitic gate outside mesa (dotted line) as show in circle

The parasitic capacitance caused by those turn-around gate area can be expressed as:

$$Cgp = Nf * Csub(L=0.7um,\ W=Ws+S)$$

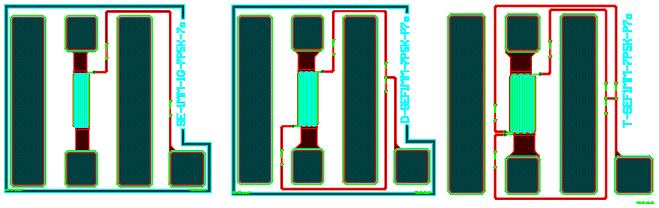
Where Cgp is the parasitic capacitance for each finger, L is the external gate length, 0.7 um, W is the average extended gate width, which is equal to spacing S plus the drain/source metal width Ws. Csub can be expressed as:

$$Csub = \varepsilon_{\_eff} * sqrt(W*L) * \pi / atan(T_{sub}/(W+L))$$

Where $\varepsilon_{\_eff}$ is the effective dielectric constant, normally is approximately $(\varepsilon_{GaAs} + 1)/2$. T_{sub} is the substrate thickness.

IV. Results on Insertion Loss- Layout Effects

The distributed effects on insertion loss are first validated with phemt 7 technology, where the drain/source metal width is 3um. Figure 5 shows the layout of 1mm SG-FET, DG-FET and TG-FET in series connection, all finger number is 8.



SG_FET in series 1mm DG_FET in series 1mm TG_FET in series 1mm

Figure 5. layout of 1mm series SG-FET, DG-FET and TG-FET. Gate resistors are all 7.5 kOhm.

Figure 6 shows the simulated (line) versus measured (symbol) in insertion loss for those series devices. It is seen that the simulated predicts very well the frequency roll-off.

The insertion loss is dependent on finger number. It is imaginable that more finger shorter unit width should have lower insertion loss. As seen in figure 7, a single Gate FET with 20 fingers with 50um for each finger has much lower insertion loss that less fingers to say 5, but longer width 200 um. This has been validated in measurements.

Next, we study the effects of connection type on insertion loss. There are three types of connections. One is called Cascade, in that the signal input and output are from the whole line combining all drain/source fingers without phase difference. The second is that signal feeds and going out from the end of the combining lines. The third one has accesses at the center with the width varying. The calculation for the third case can be done given the finger number partition between the cent and its either side by combining the cascade and tandem cases. The third and second one are shown in fig.8.

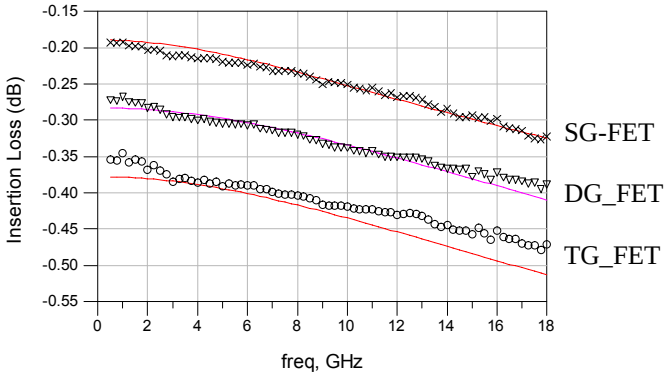


Figure 6. Simulated (line) versus measured (symbol) insertion loss for series 1mm SG-FET, DG-FET and TG-FET. The gate fingers numbers are all 8 and gate resistors are all 7.5 kOhm.

Figure 9 shows the simulated (line) versus measured (symbol) insertion loss for center (left) and tandem (right) structures. Both structures have gate periphery of 2mm and finger number are 40. It is shown that the center structure has less roll-off in insertion loss. At f=18GHz, the center structure has 0.2 dB lower insertion loss than tandem structure. The figure also shows good agreement of simulation with measured data, and thus, verified our distributed model.

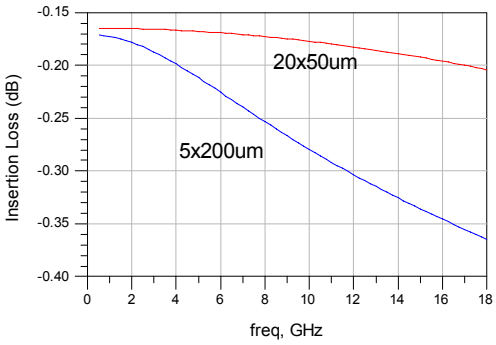


Figure 7. Simulated insertion loss of SG-FET with 1mm gate periphery. The upper curve is for 20x50um and lower curve for 5x200um.

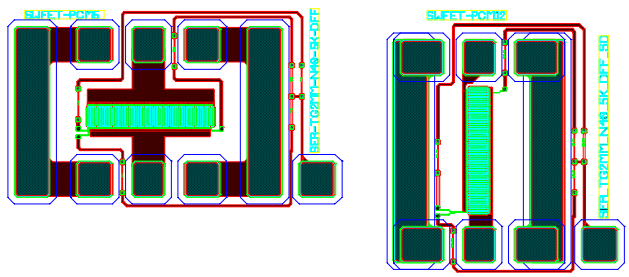


Figure 8. Patterns of 2mm series TG-FET in different connection. The left one the signal feeds and output from the center of the feeding lines. The second, tandem connection, the feeding and output are from the side of the lines.

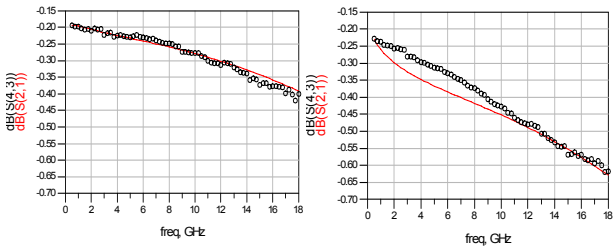


Figure 9. Simulated (line) versus measured (symbol) insertion loss for center (left) and tandem (right) structures. Both structures have gate periphery of 2mm and finger number are 40.

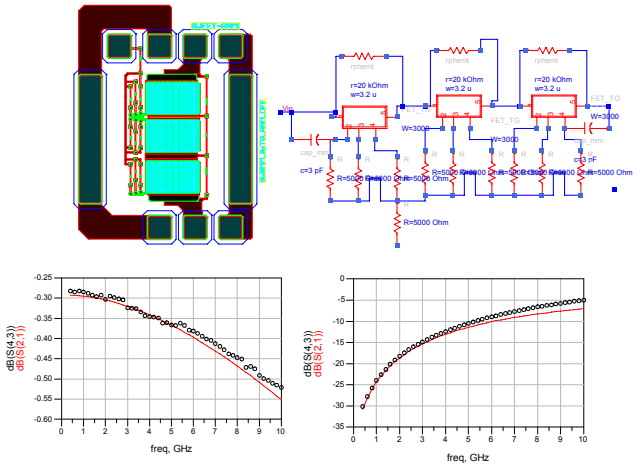


Figure 10. Simulated (line) versus measured (symbol) insertion loss (left) and isolation (right) for 3 stages of cascade 3mm TGFET with feedforward capacitance 2pF. All FET have gate finger number 25.

As last example for validation of distributed model, we used three stages of TGFET in stack connection, each FET has 3mm gate periphery and 25 fingers. The connection of the FETs is cascade. For the most side gate we used feedforward capacitances 2 pF. The layout is shown in upper-left part of figure 10 and its schematic is shown in upper-right part. The lower figures show the simulated (line) versus measure (symbol) insertion loss (left) and isolation (right) against frequency. The distributed modelling does show good agreement in small-signal response. Since it is compact model, the simulation time is only seconds in comparison to EM simulation of hours.

Finally we show the impact of parasitics on 2nd harmonics of switch. The circuit used for validation is GSM switch for nominal, low-Idss and high-Idss corners. Here just give the results for Low band –GSM band. Table 1 shows the measured harmonics data in dBm with 35 dBm drive – listed in the first column, simulated with lumped parasitics – the second column and distributed parasitic model – the third column. It is seen that the distributed model gives improved fitting in harmonics, especially for the 2nd harmonics for nominal, low_Idss corner and high-Idss corner wafers.

Table I

LB harmonics	measured	Modeled-lumped	Modelled-this work
Nominal H2	-43 +/- 1.49	-45.7	-42.8
Nominal H3	-43.6 +/- 1.26	-41.84	-41.2
Low-Idss H2	-37.9 +/-0.7	-41.2	-37.9
Low_Idss H3	-47 +/-1.13	-43.7	-44.9
High_Idss H2	-45.1 +/- 2.14	-52.7	-48
High_Idss H3	-39.4 +/-3.33	-42	-40.4

VII. Conclusions

Distributed model of parasitics for PHEMT devices are developed. The distributed model is especially useful for switch circuit applications where large periphery of device and narrower metal strips for unit device size are utilized. The model takes into account the distributed metal loss and distributed metal inductances and gate parasitics outside the gate mesa area. The distributed model predicts very well the insertion loss in terms of various gate periphery, gate numbers, and signal feeding types.

The gate parasitics outside the mesa area has great impact on 2nd harmonics. It is shown that by utilizing the distributed model, the harmonics especially 2nd harmonics can be predicted much closer to what measured at high power drive.

The distributed model allows switch designers to make trade-off in switch design between the insertion loss and harmonics. For example, given a total gate periphery, a device with more gate finger number but shorter unit gate width would give better insertion loss but worse second harmonics in high power operation.

References

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