Modeling Mutual Coupling Capacitance Effects of Package RDL to Chip on Radio Frequency ICs

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Abstract

As technology continues to scale, radio frequency (RF) applications are moving towards higher frequencies and increased levels of integration. This leads to interconnect wiring effects which impact circuit performance significantly. Chip package coupling is one of the major factors in successfully predicting final product performance. This chip-package interaction is difficult to incorporate into post-layout simulation flow; therefore, it is typically ignored. The most common solution is to use an Electromagnetic (EM) simulator to model package effects for the coupling to chip die. Challenges in EM simulations are time consuming to solve, and difficult to seamlessly integrate into parasitic extraction (PEX) simulation flows. Therefore, PEX accuracy and design automation enablement becomes more critical with the increase in performance, density, complexity and integration in analog mixed signal and radio frequency (RF) designs. A PEX solution is preferred over complicated EM tools for handling highly integrated parasitic networks. A truly comprehensive extraction solution allows design houses to have reliable parasitic analysis to reduce silicon spins and facilitate time-to-market. This paper will describe a methodology of modeling mutual coupling effects between on-chip circuits and the chip package, which enables a post-layout simulation flow with incorporating chip and package interactions simultaneously.

PEX technology files provided by foundries do not account for package layer effects on a chip, especially with re-distribution layers (RDL). In this paper, we will describe the methodology used for enabling a PEX deck to account for the mutual coupling effects with both test structures and a circuit in practical applications.

1. Introduction

As process technologies continue scale down, RF applications move to higher frequency and increased level integrations. As a result, interconnect wiring effects will significantly impact circuit performance. Chip-package coupling becomes one of the key factors in successfully predicting final product performance. With current PEX decks provided by foundries, interaction between chip and package is not incorporated into post-layout simulation flows. The current PEX methodology only captures chip die level couplings and by default also assumes a design is wire bond packaged.

The most common solution is to use an EM simulator to model package effects and to evaluate the coupling to chip die. However, there are some disadvantages with EM simulations. EM simulation capability is limited by complexity of interconnect wiring structure. Package metal routings are usually modeled by 3D EM tools [1,2]; while chip level parasitics are modeled by EDA PEX tools. This creates a challenge to integrate EM simulation results into an on-chip parasitic netlist derived from EDA PEX tools, due to different formats and interface restrictions, etc.

We have developed a solution to capture the coupling effects between the IC package and an on-chip circuit using EDA tools. We will describe the methodology and discuss how to implement it in a typical RF technology in Section II. Section III shows test results, and section IV describes summary details.

2. Extraction Methodology

PEX accuracy and design automation enablement become more critical with increasing complexity and levels of integration in analog mixed signal and RF designs. In general, a PEX solution is preferred over complicated EM tools for handling highly integrated parasitic networks, since it is faster and easier to use than EM tools. A truly comprehensive extraction solution should provide design houses with accurate post-layout simulations to reduce silicon spins and accelerate time-to-market.

Mentor Calibre xRC is a common parasitic extraction tool, and we focus on enabling the feature to account for packaging effects with xRC PEX flow. Based on the foundry provided Mentor Interconnect Process Technology (MIPT) file, we can enable our customized MIPT with the addition of a package layer RDL, and set up connectivity between on-chip designs with RDL,

which basically extends the last metal layer to the RDL. Figure 1 shows the typical RDL process cross section in the technology. By adding the package parameters for related dielectric constants and other electrical parameters, we create a complete MIPT techfile. Then we use the Mentor Calibre xcalibrate engine to generate the customized tech rule file. Figure 2 shows the MIPT cross section in Mentor xcalibrate view engine. The more detailed descriptions can be found in reference paper [3].

After MIPT and tech rule file are generated, we need to define RDL related layers in Calibre LVS (layout versus schematic) to establish the complete connectivity from the bottom substrate-RDL layers. Therefore, corresponding layers can be recognized by both LVS and PEX. As a result, PEX can extract coupling effects between RDL and DIE correctly, which are commonly ignored by PEX decks provided by foundries.

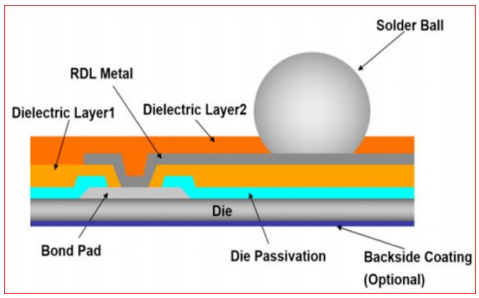

Figure 1: The cross section of RDL Process

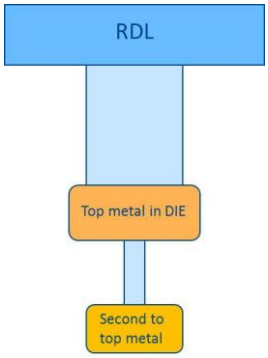

Figure 2: MIPT cross section

3. Test Structure and Validation

To validate the rule file against a standard reference EM tool, we have used a common test structure –nested metal lines as shown in Figure 3.

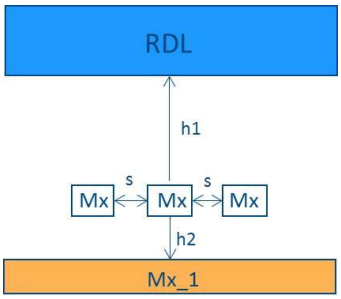

Figure 3: Nested metal line test structure

The purpose of this test is to correlate the accuracy of the newly created PEX with our standard reference EM flow. Table 1 shows simulation results for both the new PEX deck and EMX, which ensures that the PEX deck can be used for RDL layer extraction precisely. In Table 1, w1 means one time minimum width and s1 and s2 mean one or two times of minimum spacing for the metal layer in the nested structure.

Table 1: xRC vs EMX results

EMX	LEFT	CENTER	RIGHT	TOP	BOTTOM
RDL_cap_test_w1_s1.gds	1.91E-14	2.18E-14	1.91E-14	2.90E-14	8.80E-14
RDL_cap_test_w1_s2.gds	1.69E-14	1.73E-14	1.69E-14	3.01E-14	9.06E-14
xRC	LEFT	CENTER	RIGHT	TOP	BOTTOM
RDL_cap_test_w1_s1.gds	1.94E-14	2.37E-14	1.94E-14	4.40E-14	5.22E-14
RDL_cap_test_w1_s2.gds	1.69E-14	1.85E-14	1.69E-14	4.29E-14	5.48E-14
Deviations	LEFT	CENTER	RIGHT	TOP	BOTTOM
RDL_cap_test_w1_s1.gds	1.58%	8.69%	1.58%	51.90%	-40.69%
RDL_cap_test_w1_s2.gds	0.18%	6.64%	0.18%	42.62%	-39.49%

In Table 1, the capacitance unit is farad (F) and the capacitance values are the total capacitance. The capacitance value of column center is the sum of center to left, to right, to top and to bottom. With respect to accuracy, the total center value is the most important. In reality most of the interconnect lines are surrounded by different routing lines from all of the directions. Therefore, per the Table 1 results, there is high confidence to use the customized PEX deck to predict the RDL effects of a real design.

We also verified the accuracy of the new PEX deck with an LNA design as shown in Figure 4.

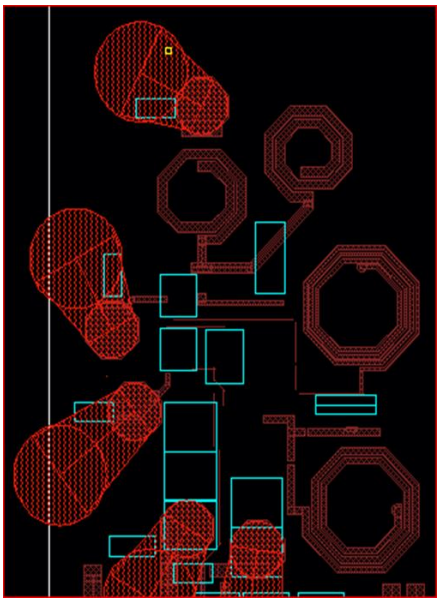

Figure 4: LNA layout with RDL

In this design, there are some RDL layers overlapping with DIE, which will impact the LNA performance. We will run post layout simulations using Mentor Calibre xRC[4] PEX with/without RDL layer to see whether there are any differences on some critical LNA parameters, due to RDL layer effects. In the case of LNA designs, designers are usually concerned with the following design performance parameters: NF, NFmin, Gain, ReZin, etc. Simulation results shows: with RDL layers, the minimum noise figure (NFmin) became degraded by 19%, gain (s21) degraded by 3.3% and ReZin degraded by 24% compared to that layer RDL is not being considered.

The simulation results indicate that ReZin, input impedance, is more capacitive with the effect of RDL layer. This makes sense as the coupling capacitances increase when RDL layer is over the top of the last metal layer. In addition, as the loss increases, the gain of LNA is degraded. NF and NFmin also becomes worse as RDL layer covers more metal layers, which is consistent with our expectation in theory and matches with our measured data.

4. Summary

In this paper we described the methodology we used to expand the capability of PEX deck to consider coupling effects from DIE to package RDL layer, which are widely ignored by the PEX deck provided by foundries. Simulation results show that our customized PEX deck with RDL effect being considered can very well predict the coupling capacitance effects between RDL to a DIE.

It can also be concluded that this methodology enables modeling of mutual coupling between on-chip circuits and the chip package, which allows post-layout simulations to incorporate chip and package interactions seamlessly and simultaneously.

Acknowledgments

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