# Large-signal Modeling of SiGe HBT for PA Applications

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***Abstract* — Accurate modeling of large-signal behavior of power amplifiers (PAs) is key in minimizing the number of design spins and design cycle time. This paper presents the 1- and 2-tone large-signal behavior of SiGe HBT with respect to power, frequency, bias, and transistor geometry. While the transistor's weak non-linearity is largely determined by the trans-conductance (Gm) and the quasi-static (QS) charge-storage of the transistor, its high-power large-signal behavior heavily depends on the high-current gain roll-off characteristics and supply clamping. It is discussed from a PA-design standpoint how the SiGe bandgap engineering impacts the large-signal behavior through a steeper gain compression at high currents and high power levels. It is also shown that the 2-tone inter-modulation products of a transistor are closely related to its 1-tone distortion characteristics. Finally an accurate prediction of critical parameters of a practical WCDMA PA was demonstrated with careful accounting of the high-current effects in the SiGe HBT transistor.**

**Index Terms — SiGe HBT modeling, large-signal modeling, PA design, RF circuit design.**

## I. INTRODUCTION

The rapid commoditization of cellular applications has stimulated the development of Si PAs leveraging their low cost and natural capability to enable sophisticated bias schemes and integrated controllers on the same die. However, because of the lower breakdown voltage (BV) at applicable speed, PAs manufactured with Si bipolar junction transistors (BJT) have only very limited success in the commodity handset marketplace. SiGe BiCMOS technologies with improved performance and additional technology features make them attractive to address new system level requirements. While having low cost in volume production, Si-based technologies tend to have higher non-recurring engineering (NRE) costs and longer development times. To offset this disadvantage, accurate models and simulation methodologies are required to reduce the number of mask spins, achieving acceptable NRE and time-to-market. Also, because an IC at higher integration is more difficult to debug at the hardware level, a predictive model is always desirable as a powerful and cost-effective diagnostic tool.

Design of handset PA mostly focuses on meeting sufficient power output (Pout) and linearity, while maximizing the power added efficiency (PAE). Recent emphasis for extended battery life in a metropolitan area requires a PA having high PAE, not just at the maximum Pout, but also at the low and medium power level. To optimize the PA for this wide range of Pout, the large-signal behavior of the transistor has to be accurately predicted over a wide range of bias as well as input power.

As the application of SiGe HBT has grown beyond its original purpose for the making of super computers and extended into the RF and microwave range, many research papers have been published in the area of RF modeling. However, most of them focused on small-signal behavior and noise modeling of the transistor [1][2]. Only a few discussed the non-linear behavior of the transistor with little emphasis for high-power PA application [3][4] or based on the analysis of Volterra series [5].

While providing insight on the impact of each non-linear component within a transistor to the overall system distortion [5][6], the Volterra series is practical only for analysis of weak non-linearities. Its application relies heavily on an accurate compact model to provide good estimates of the transistor parameters, such as $G_m$, $C_{BE}$, and $C_{BC}$, at the bias point where the non-linearity is calculated. Therefore, it is only useful for the analysis at a given quiescent point such as in an LNA.

To reveal the non-linear behavior of a transistor with respect to bias and power for PA applications, our approach is to evaluate compact transistor models at various levels of complexity and understand the most important effects for high power and, more importantly, at a wide range of bias conditions. As suggested in [7] and also shown in the later 2-tone large-signal measurement, the 3rd order inter-modulation (IM3) can be greatly reduced as the transistor is biased at a certain current level.

Understanding the scaling of the transistor performance with respect to the emitter width ($W_E$) is also critical, as the optimization of a big transistor array, capable of delivering sufficient output power, depends on the trade-offs between various parameters as a function of $W_E$ and $L_E$. The selection of a particular transistor geometry must take into account several important factors such as layout footprint, thermal

properties, and RF properties (largely the reduction of base-collector capacitance per emitter area) [8]. The width to reduce the footprint, as an example, must be evaluated against the trade-offs with the RF gain, emitter utilization, linearity, ruggedness, and stability. For instance, the narrowest finger, while generally having higher maximum oscillation frequency (fmax) -- the figure of merit often quoted for the technology -- does not always provide the maximum stable gain at all frequencies. Contrarily, widening the finger can make it more susceptible to pinch-in. As a result, it is very desirable for designers to optimize the transistor geometry for different stages, applications, or bias conditions.

The paper is organized as follows: the next section presents the large-signal characterization result of the transistor, followed by a discussion of its application to high-power PA design. For the purpose of illustrating the most important effects of a SiGe HBT for high-power PA application, two models are investigated: 1. the SPICE Gummel-Poon Model (SGPM) and 2. the High Current Model (HICUM) for bipolar transistors. Finally, a system-level validation of the full-blown HICUM model is demonstrated on a WCDMA Band V PA.

## II. Measurement and Modeling

The process used here is a custom 0.35μm SiGe BiCMOS process with a tailored collector implant for high-power PA application. The process has an option of adding GaAs-like through-wafer vias (TWVs), enabling a single-ended amplifier architecture, which is commonly used in the commercial cellular PAs. The devices under test (DUTs) are the proposed PA unit cells with different emitter widths (WEs). The DUTs were laid out in GSG pads for testing. The layout of the transistor was custom-made as in the large PA cell array.

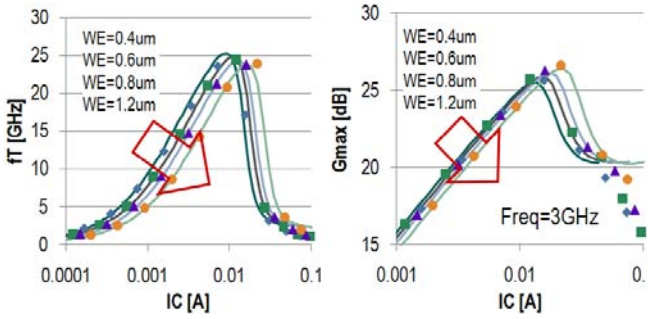


Fig. 1. RF performance, fT on the right and Gmax on the left, of transistors of different WE of 0.4, 0.6, 0.8, and 1.2um and constant $L_E$=20um. Symbols represent the measured data and lines model prediction.

A wider emitter is always desirable for making the final stage of a PA, as it enables a more compact layout for the same amount of output power capability and has less parasitic. For the technology used here, the transistor with wider emitter also has a higher $G_p$, thereby enabling higher PAE or providing room for trade-off with other critical performance parameters. Depending on the application, the manufacturability, the thermal characteristic, and how the $R_b$ and $C_{cb}$ trade off with each other with respect to $W_E$, the transistor with increased $W_E$ does not always have benefit for PA design. Therefore a continuously scalable model is required for the PA array optimization.

Since the foundry-provided model supports only two discrete $W_E$s of 0.44 and 0.8μm, the model used here was enhanced with the methodology outlined in [9] to be continuously scalable from WE=0.4um up to 1.2um. To scale the high current effects with respect to $W_E$, a trapezoidal shape of collector spreading as described in [10] is assumed to scale the high-current charge parameters. Fig. 1 shows the model can predict the basic RF performance such as $f_T$ and $G_{max}$ for more than 3 decades of $I_C$ and $W_E$=0.4~1.2μm.

While it is known that SGPM is insufficient for high-power applications, it highlights in the exercise here how the high-current effects influence the large-signal behavior of a transistor. The high-current effects, which are also known as base push-out or Kirk effect, cause a surge in the quasi-neutral charges in the base, which in turn causes the gain compression and distortion of the transistor. Fig. 2 shows the SGPM prediction on the 1- and 2-tone characteristics of a transistor. The SGPM model used here was extracted from a simple DC and small-signal AC capacitance measurement. Therefore the model, while predicting accurate DC currents and AC capacitances at low currents, does not account sufficiently for any of the high-current effects. As shown in the figure, the model does not predict gain compression properly due to the insufficient accounting of such excess charges. Therefore the model is too optimistic at high-power levels. However, the model can still predict the non-linear behavior reasonably well up to the P1dB point, demonstrating the weak non-linearity of a transistor largely depends on just its DC $G_m$ and drift/diffusion capacitance.

The excess charge accumulation in a SiGe HBT increases at a much faster rate than that in a Si transistor, when $I_C$ surpasses a certain value. This is due to the retarding field induced by the bandgap difference at the base-collector junction. When the current is low, a retarding field is countered by the strong electric field in the base-collector depletion region. As the base push-out happens at high currents, this counter field disappears and the retarding field becomes suddenly present, causing an enhanced charge accumulation in the extended base. This effect is also manifested in the

especially steeper $f_T$ roll-off at high currents, when compared with that of a Si bipolar transistor.

While HICUM does not explicitly account for such a retarding field caused by the bandgap difference at the base-collector junction, its transit equation was formulated suitably to model such a sharp rise of the quasi-neutral charges in the base [10]. Fig. 3 shows the prediction of HICUM on the large-signal behavior of a transistor. Accurate accounting of the sharp high-current charge storage increase for a SiGe HBT extends the predictability of 1-tone harmonic distortion and 2-tone 3rd and 5th order inter-modulation IM3 and IM5 by ~20dB above the P1dB point, thereby making HICUM suitable for high-power application.

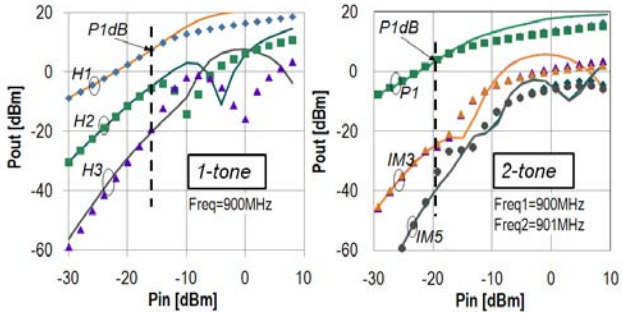


Fig. 2. Prediction of a simple SGPM model versus 1- and 2-tone large-signal characterization data of a 4x1.2umx20um transistor VBE=0.8V, VCE=3.0V. Symbols represent the characterization data; lines the model prediction.

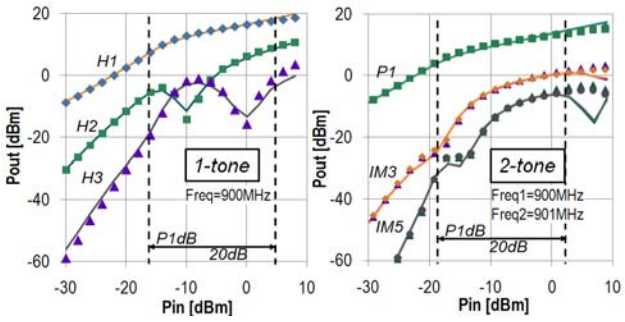


Fig. 3. Large-signal prediction of the full-blown HICUM model versus 1- and 2-tone large-signal characterization data of a 4x1.2umx20um transistor at VBE=0.8V, VCE=3.0V. Symbols represent the characterization data; lines the model prediction.

Fig. 4 shows the excellent predictability of the model on the large-signal behavior of the PA unit cell versus the quiescent $V_{BE}$ bias, which corresponds to more than two orders of magnitude of change in $I_C$. As shown in the figure, the 2-tone IM3 tracks well with the 1-tone H2, while IM5 correlates well with the H3. This can be intuitively understood with the fact that IM3 is the mixing product of the 2nd harmonic with the fundamental of the other tone. Similarly IM5 is the product of the 3rd harmonic with the 2nd harmonic of the other tone.

Based on the correlation, the optimal IM3 bias point can be estimated with the H2 of a simple 1-tone measurement. It is also interesting to note that H2 dips when the fundamental tone of the transistor reaches its peak. It can be understood as the magnitude of H2 of a transistor is proportional to the absolute value of the derivative of its fundamental tone with respect to the input voltage, i.e. $V_{BE}$ in this case. Therefore the dip of H2 appears when the fundamental tone peaks and a severe gain compression occurs.

It is important to note that the large-signal characterization presented here was made with a typical broadband 50ohm system. As the PA unit cell, i.e. the DUT here, is around 2 orders of magnitude smaller than the final stage PA array, the gain compression of the PA unit cell under such a system is mainly driven by the high $P_{in}$. The gain compression of an actual PA, as designed for high PAE, is usually dictated by both supply clamping and input gain compression. Even with a different gain compression mechanism, it is common to observe a similar dip in IM3 or H2 for a PA that correlates with the severe gain compression at high power levels.

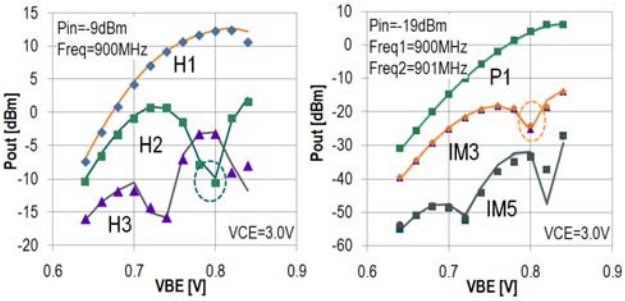


Fig. 4. Large-signal prediction of the full-blown HCUM model versus VBE for a 4x1.2umx20um transistor at constant Pin=-9 and -19dBm for 1- and 2-tone characterization; Symbols represent the characterization data; lines the model prediction.

## III. System-Level Validation

The vehicle used here for the system-level validation is a WCDMA band V PA. The design has complete bias, power control, and ESD protection circuits on chip. The input matching is on-chip and the output matching is realized with printed inductors and SMT components at the module level.

Modeling of a finished PA requires not just a good transistor model, but also an accurate accounting of the bond wires, printed components, surface mount components (SMTs), and ground network of the printed circuit board (PCB). The module-level model was obtained with Ansoft HFSS 3D electromagnetic (EM) simulation and the ground network was simulated with Q3D. It is discovered that the PA small-signal response is extremely sensitive to the modeling of the module-level components, while the large-signal behavior

heavily relies on the transistor, especially at the high-power level, when the amplifier operation is close to gain compression.

Fig. 5 shows the full-blown HICUM, when combined with a thorough modeling for the module-level components, can predict well the power gain ($G_p$), power added efficiency (PAE), and 3rd order inter-modulation distortion (IMD3) performance of the finished WCDMA PA at the test board level from low all the way to the high Pin that drives the PA into hard saturation. As expected from the earlier discussion, a pronounced IM3 dip appears just as the severe gain compression occurs. IM3 is the most important design parameter for the modern linear-type PA, as it directly impacts the Adjacent Channel Power (ACP) performance.

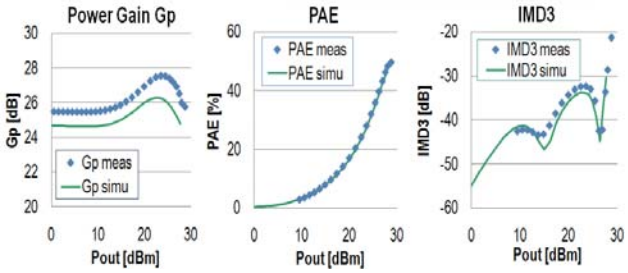


Fig. 5. Power, PAE, and IMD3 of the WCDMA PA measurement data versus model.

It is interesting to note that the key performance parameters of the WCDMA PA, such as those shown here, do not have a significant sensitivity to a reasonable amount of perturbation to the self-heating or impact ionization parameters in the model. It is because the self-heating is not quite severe. A thermal scan on the die reveals that the maximum temperature rise is only a few degrees and the gradient is not very pronounced as compared to its GaAs counterpart. In additions, per WCDMA linearity requirements, the PA is usually designed with some margin from the hard VCC clamping, i.e. back-off from the saturated power. Therefore, the impact ionization current is not very significant and does not influence the performance either.

## IV. Summary

First the modeling of the weak non-linearity of a transistor was investigated. It was demonstrated that the transistor distortion and inter-modulation behavior at small to medium power levels can be captured sufficiently with the conventional SGPM model based on DC IV and small-signal AC capacitance at low currents. However, the modeling of a transistor non-linearity at high power, i.e. beyond P1dB, needs careful treatment of the transistor behavior at high currents. It was shown that the transistor's IM3, as closely correlated with H2, is a strong function of $I_C$. The fact highlights the importance of the modeling of the steeper gain roll-off for a SiGe HBT for PA application. Finally the predictability of the model on large-signal gain (Gp), output power (Pout), and inter-mod modulation (IMD) was demonstrated on a practical WCDMA PA manufactured with the SiGe HBT process.

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