Recent Study on On-state Breakdown Modeling of pHEMTs

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Abstract—**Traditionally, the on-state breakdown of pHEMTs is attributed to impact ionization and thermal breakdown under high Vd stress. Nonetheless, neither of these hypotheses perfectly explains all observations, including but not limited to when on-state breakdown happens and how it happens in devices with various structures. A systematic study on the on-state breakdown of pHEMTS carried out by our group recently reveals strong correlation between the adjusted input power and the burnout locus of devices. We further conclude that on-state breakdown happens mainly because the temperature of a certain spot in the channel exceeds a critical value, and that this hot pot, usually emerging beneath the drain-side end of the gate electrode, is the result of the unevenly distributed electric field in the channel of the pHEMT. We thereby developed a simple model which sheds some light on the physics mechanism behind on-state breakdown of pHEMTs and is capable of accurately predicting the corresponding burnout voltage for different devices under operating various operation conditions.**

Keywords – Pseudomorphic HEMT (pHEMT), breakdown voltage, power burnout, on-state breakdown.

I. INTRODUCTION

As one of the most important devices for microwave and millimeter-wave applications, pHEMTs draw tremendous attention on the issue of its reliability, especially under high bias stress. As a consequence, there have been great amounts of study devoted to understanding the physics mechanisms behind breakdown of pHEMTs. Considerable progress has been made in the past decade on the research of off-state breakdown [1] and the strategy to improve the off-state breakdown voltage of pHEMTs, such as the introduction of field plates and the engineering of gate recess region. On the other hand, relatively less advancement has been accomplished in the area of on-state breakdown, including both explanation to the underlying physics mechanisms and corresponding modeling approach to precise prediction of the locus of on-state breakdown. Two mainstream theories on on-state breakdown of pHEMTs are impact ionization theory [2] and power burnout theory. Nevertheless, recent study of our group suggests that there exists another theory because some pivot factors are not taken into consideration during previous research.

The main difficulty that the power burnout theory experiences is the prediction of the locus of on-state breakdown. Apparently, the on-state breakdown happens under much higher drain biases than the theory foretells, especially when the gate bias is high. On the other hand, the impact ionization model considered off-state breakdown a thermionic-field emission (TFE)-dominated process and on-state breakdown a multiplication-dominated one. While the experimental result shows that impact ionization does happen in the channel of a pHEMT at the time when on-state breakdown happens, the coincidence does not necessarily lead to the consequence. It is commonly observed in experiments that a device may still survive even after the impact ionization has started for a while.

II. MODELING PROCESS

Previous research [3] studying the distribution of voltage and lateral electric field indicates that the current path in an operating pHEMT mainly follows the hetero-junction interface, and, under certain bias conditions, deviates from the interface beneath the drain-side end of gate electrode. The place where the lateral electric field peaks is thereby where the most voltage drop occurs. In fact, after a pHEMT reaches saturation, the drain bias in excess of the onset saturation voltage will mostly drop in this region. Fig. 1 shows the uneven distribution of lateral electric field and electron concentration. The voltage dropped in this region, defined by the integral of lateral electric field, clearly accounts for most of the total drain bias.

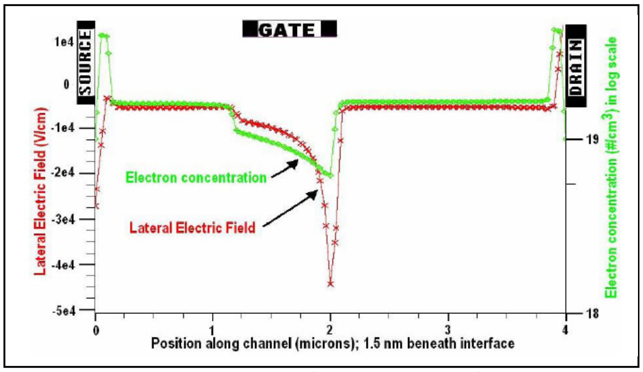

Figure 1: The distribution of lateral electric field and electron concentration along the channel of a pHEMT.

As a result, the unevenly distributed voltage drop leads to an unevenly distributed channel resistance throughout the current path. Due to the continuity of drain current, the channel resistivity peaks where the lateral electric field reaches its maximum value, as shown in

$$\rho(x) = \frac{dV(x)}{Idx} = \frac{E_x(x)}{I} \tag{1}$$

Consequently, the power dissipated at a certain location P(x) is proportional to the value of the resistivity function at that spot. In other words, the power dissipation beneath the drain-side edge of gate electrode is much higher than at other spots in the channel.

As for the thermal model, the thermal network is depicted in Fig. 2, based on the widely accepted theory of thermal modeling of transistors [4][5].

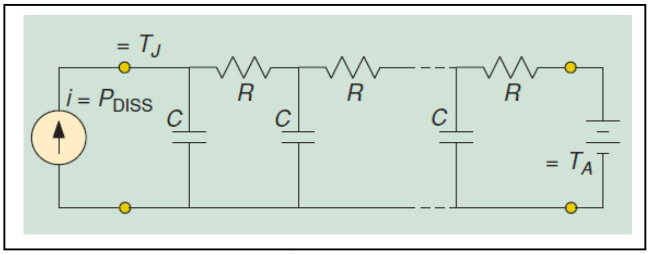

Figure 2: 1D themal network of a spot in a pHEMT

Keeping the back of the device at a constant temperature equal to the ambient value, we consider the rise of the temperature at a specific spot determined by the power dissipation $P_{diss}(x)$ and the R-C thermal network. A simplified model extensively used is

$$T_J = T_A + P_{diss} R_{TH} \tag{2}$$

Combining (1) and (2), we can readily get the temperature distribution as

$$T_J(x) = T_A + I R_{TH} E_x(x) \tag{3}$$

Because of the much higher lateral electric field at drain-end gate edge in comparison to that in other spots, source access region for example, the temperature at this hot spot is much higher than at other places, if we neglect thermal coupling for the sake of simplification.

To determine the locus of on-state breakdown on I-V plane, we need to calculate the maximum lateral electric field at a certain corresponding operating point. An accurate modeling approach can be achieved by the modeling of lateral electric field reported before [6], together with a temperature-dependent thermal and transporting parameter set. Meanwhile, we can always make a rough estimate to determine the locus of on-state breakdown on I-V plane, we need to calculate the maximum lateral electric field at each corresponding operating points. An accurate modeling approach can be achieved by the modeling of electric field described before, together with a temperature-dependent parameter set. Meanwhile, by employing a first-order thermal network and some simplification measures, such as temperature-independent parameter set and an approximated analytical solution of lateral electric field, we can make a rough estimate which predicts the trace of on-state breakdown spots in the I-V plane as follows:

$$I^2 \times (I_0 - I) \times (V - V_0) = A \tag{4}$$

where A is a constant decided by thermal resistance and critical temperature; I_0 is the upper threshold of drain current transported in a pHEMT, and V_0 is the lower threshold of drain-bias inducing an on-state breakdown determined by thermal and fabrication parameters, and associated with the distribution of lateral electric field throughout the channel.

III. DISCUSSIONS AND CONCLUSIONS

The curve depicted in (4) satisfactorily explained the commonly seen steep end of the trace of on-state breakdown locus in an I-V plane, which happened in the region of low drain-bias and high current. Furthermore, the inclusion of V_0 explains previous experimental observations that on-state breakdown never happens when drain bias is lower than a certain value. This feature overcomes the difficulty which power burnout theory meets while using contour lines with same level of power to model locus of on-state breakdown. At the other end of the trace, when the current drops to a certain level, the phenomenon of TFE from drain-side gate edge emerges and dominates, incurring the off-state breakdown. In a complete breakdown model, the trace of breakdown locus will be a combination of these two curves.

Meanwhile, the development of this model and the understanding of the physics behind on-state breakdown also provide some insight into prevention measures. As the model explains, a multi-gate device experiences almost the same level of risk of on-state breakdown as single-gate devices because the difference in configuration does not change the fact that most of the drain bias drops at the gate edge closest to the drain. Nonetheless, those measures leading to more balanced distribution of lateral electric field, such as field plates, will help protect the device from on-state breakdown.

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