Transmission-Line Broadband GaN FET Class-E Power Amplifier

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Abstract — A transmission-line loading network for class-E amplifiers is presented. In this work, a GaN FET device with a parasitic drain capacitance of 4-pF is used at 1-GHz design frequency for 20-W output power at 20-V DC supply voltage. A finite inductive reactance DC-feed class-E amplifier output network is designed based upon wire-lines and then modified using transmission-line transforms. The final network topology is managed so that it contains specific transmission-line impedances suitable for breadboarding employing air-suspended brass-bars so that no dielectric is used. The network presents the proper impedance at the device intrinsic drain and at the same time serves as broadband matching to 50-Ohms. The resultant measured performance of 80% efficiency or higher and flat output power over wide bandwidth (760-1060 MHz) is presented.

Index Terms — Amplifier, broadband, class-E, efficiency.

I. Introduction

Several different methods for transmission-line (TL) loading networks for high-efficiency power amplifiers (PA) can be found in the literature designed to meet the required impedances at the device reference plane at the fundamental-frequency (f_0) and a limited number of harmonics [1].

In this paper, a simple TL loading network synthesis method is applied by using TL as reactors at f_0. Nonetheless the resultant network has no practical implementation in planar form and transforms are used to manage the TL impedances, network topology realizability and broadband matching. The PA input and output networks are then realized in microstrip form using air-suspended brass-bar TLs over a ground plane so that no substrate is used and it makes it convenient for breadboarding and tuning obtaining high efficiency in a broad frequency range performing as a parallel-tuned class-E PA.

II. Basic Transmission-Line Class-E PA Design

In [2] the optimal loading network component values are computed for a broadband class-E PA using reactance compensation and it is realized using lumped elements. We can take the reactances of these components to define dual loading network based on wire-line TLs.

Alternatively, this technique can be understood as a direct substitution of lumped-elements to TL by applying Kuroda identities [3].

As a proof of concept a design example with target output power of *20*-W with a supply voltage of *20*-V and load resistance $R_0=27.36$-Ω is presented. The computed optimal

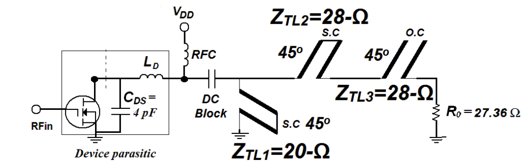

Fig.1. Wire-line transmission-line class-E PA.

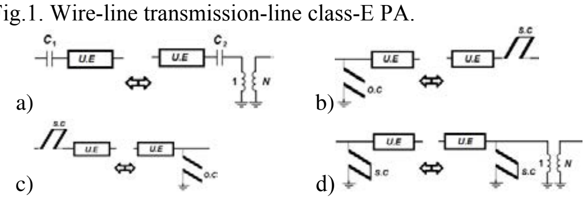

Fig. 2. Richard's transforms. All wire-lines and UE are 45° in length.

output capacitance [1], [2] is 4 pF at f_0 of 1-GHz; hence, a PolyFET device GP2001 with C_{OSS}=4 pF is a suitable GaN FET to serve the purpose. Next, the output network is designed using wire-line TL. The first wire-line from drain to load will have a characteristic impedance defined as $Z_{TL1}=0.732 \cdot R_L$ = 20-Ω, Fig 1. The RF-Choke and DC-block are considered ideal components.

For this particular design, the series connected short-circuited (SC) wire-line and open-circuited (OC) wire-line act as a series resonator for pseudo-reactance compensation. Their respective impedances are: $Z_{TL2}=1.026 \cdot R_L$ = *28.1*-Ω for the series connected SC wire-line. The series connected OC wire-line impedance has to be exactly the same as that of Z_{TL2}, thus $Z_{TL3}=Z_{TL2}$=*28.1*-Ω, Fig. 1. The electrical length of all wire-lines is 45° (1/8-λ) at the design f_0 of 1-GHz.

The basic wire-line class-E amplifier schematic shown in Fig. 1 represents the dual of a lumped-element loading network. However, the series-connected SC and OC wire-lines cannot be realized in planar form; moreover, broadband matching to a 50-Ω load must be included.

III. Transmission-Line Transforms

In order to implement a suitable TL loading network in planar form for a broadband class-E amplifier around f_0 TL transforms are introduced.

All transforms are performed at 1 GHz and most of them have been used extensively in TL microwave filter design. First, TL transforms are applied to the original schematic for broadband matching to 50-Ohms similar to [2]. Then, the well-known Richard's transforms are applied for network topology practical implementation introducing unit-elements (U.E). A summary of TL transforms used in this paper is shown in Fig. 2 and they can be found in [3]. The

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transformation process is tedious but the final network is compact and suitable for a broadband PA without any extra matching to 50- Ω required.

A. Transforms for broadband matching

The schematic shown in Fig 1 is now transformed in order to provide impedance matching to 50-Ω and the transformation sequence begins with the addition of a series SC (Z_{TL4}) and shunt OC (Z_{TL5}) wire-line as shown in Fig. 3a. This steps-up the load impedance to 30- Ω. Next, the two SC wire-lines are merged into Z_{TL6}=36.62-Ω and broadband impedance matching to 50- Ω is performed by the addition of a transformer with turns ratio N1=1.291, Fig. 3b. The next transform is the L-left to L-right applied to the OC wire-lines Z_{TL3} and Z_{TL5} resulting in the schematic in Fig. 3c alternating series and shunt connected wire-lines. This includes a transformer with N_2=0.773 which is the inverse of N_1, thus the two transformers cancel as shown in the equivalent network in Fig. 3d with 50-Ω load.

B. Transforms for network topology

After applying the previous transforms for broadband matching to 50-Ω and shunt wire-lines to ground at all nodes the schematic in Fig. 3d still imposes several practical difficulties. The large impedance ratio between the shunt SC and shunt OC wire-lines, the inability to implement the network in planar form and the lack of physical separation between wire-lines are practical issues that have to be overcome in the following transformation sequence. Also, TL impedances near to 50-Ω are desirable.

For convenience, the OC wire-line Z_{TL8} is replaced by its equivalent series capacitor C_1=4.38pF, Fig 4a, so that we have only three wire-lines to deal with and C_1 will assist in following steps using Richard's transforms [3]. Besides, a 50-Ω unit element, UE1, in planar form TL, is inserted between C_1 and the 50-Ω load, Fig 4a. Its electrical length is 45^o (1/8λ) and has no influence in the network characteristics at the design frequency. Now we can apply the Richard's transform from Fig. 2a to C_1 and UE1 in Fig 4a. The resultant schematic is shown in Fig. 4b. Design equations for this and other transforms are available in [3].

The next step is to shift the UE2 towards the left side of the circuit. Such that, the transform from Fig. 2b is applied to Z_{TL7} and UE2 creating UE3 and Z_{TL9} in Fig. 4c.

Again, the UE3 is pushed to the left of the ciruit using transforms from Fig. 2c, creating UE4 and the shunt OC wire-line Z_{TL10} in Fig. 4d. Now there is a TL between two shunt wire-lines. The same procedure is repeated introducing the UE5 at the 50-Ω load. C_2 is shifted to the right side of the transformer creating C_3, in Fig. 4e, and applying the transform in Fig. 2a the schematic in Fig. 4f is created.

Next, Z_{TL9} is shifted to the right of transformer N_3 so that it is adjacent to UE6 and the transforms in Fig. 2c is applied creating Fig. 4g in which all wire-lines are shunt connected

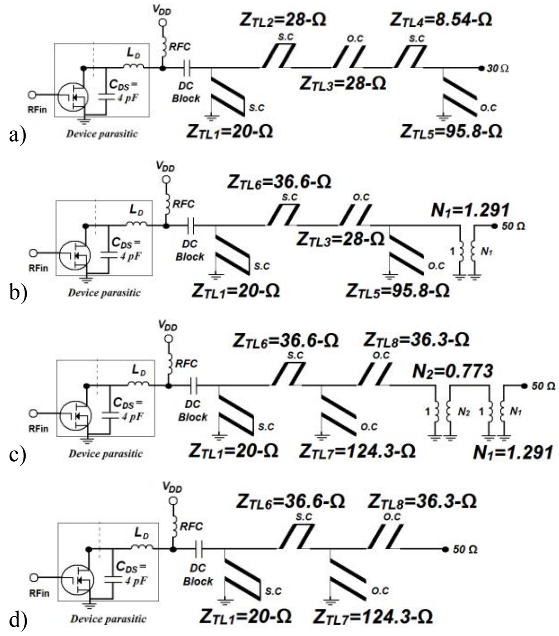

Fig.3. Wire-line transforms. All line lengths are 45^o (1/8λ).

and the network is getting ready to be implemented in planar from. The two ideal transformers remain to be eliminated.

In order to eliminate the two transformers in Fig 4g, Z_{TL1} is split into two SC wire-lines of specific impendences (Z_{TL13} and Z_{TL12}). We can use the SC wire-line Z_{TL12} of 58- Ω which is adjacent to UE4, Fig 5a, and apply an L-right to L-left transform introducing a transformer with turns ratio N_5 with inverse value of the product of the two transformers N_3 and N_4 such that the three transformers can be eliminated in subsequence steps, Fig 5b. Also, because of its high impedance, the OC wire-line Z_{TL11} which is right next to UE6 can be eliminated, Fig 5b.

The network simplification is straigthforward. Transformer N_5 is shifted to the right to be next to transformer N_3 and this produces an equivalent transformer N_6 with turns ratio of $N5 \cdot N3 = N_6 = 1.42$, Fig 5c. When a transformer is moved to the right all component values it passes change according to the move transformer right transform shown in [2]. Then the right most transformer is moved to the left in order to meet transformer N_6. Again a transformer moved to the left changes the values of all components it passes [2] in this case, C_5 and UE8 change accordingly, Fig 5d. The final schematic is shown in Fig 5e and it has no transformers, all shunt wire-lines, it is matched to 50-Ω and ready to be implemented in planar form such as microstrip lines.

C. Final network in planar form

It is convenient to manage the characteristic impedance of the wire-lines in the schematic in Fig. 5e. Since a 45^o wire-line with a characteristic impedance Z present a given reactance at the design frequency, this wire-line can be replaced by a planar form TL with characteristic impedance of 50-Ω and electrical length other than 45° [3], e.g, Z_{TL13}= 30.5-Ω with 45° of length is equivalent to a TL Z_{TL13}=50-Ω and 31.7° of length at 1-GHz, Fig 6a. Similarly, the wire-lines Z_{TL14} and Z_{TL15} have their duals with 50-Ω characteristic impedance and Z_{TL3} is now used as the DC feed. The unit elements UE7 and UE8 have no duals in this form.

Finally, the physical TL widths and lengths are synthesized as shown in Fig. 6b for a microstrip implementation with no substrate (air) so that a dielectric constant of ε_r=1 is used with a height of 30 mils as described in the next section.

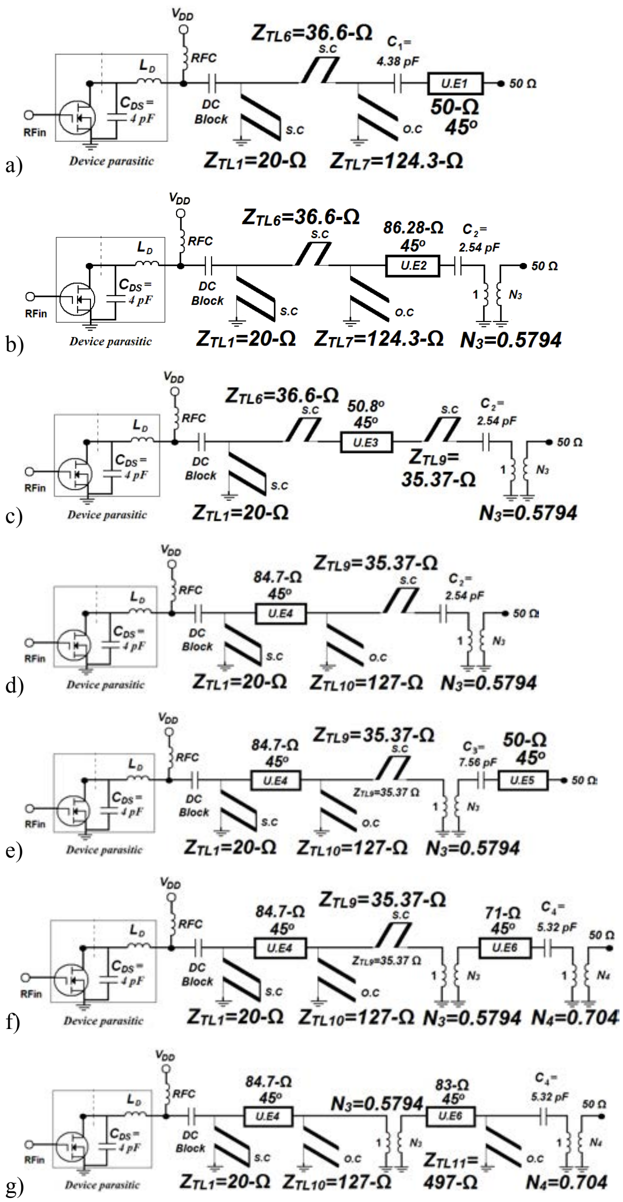

Fig.4. Transformation sequence to obtain shunt-connected wire-lines.

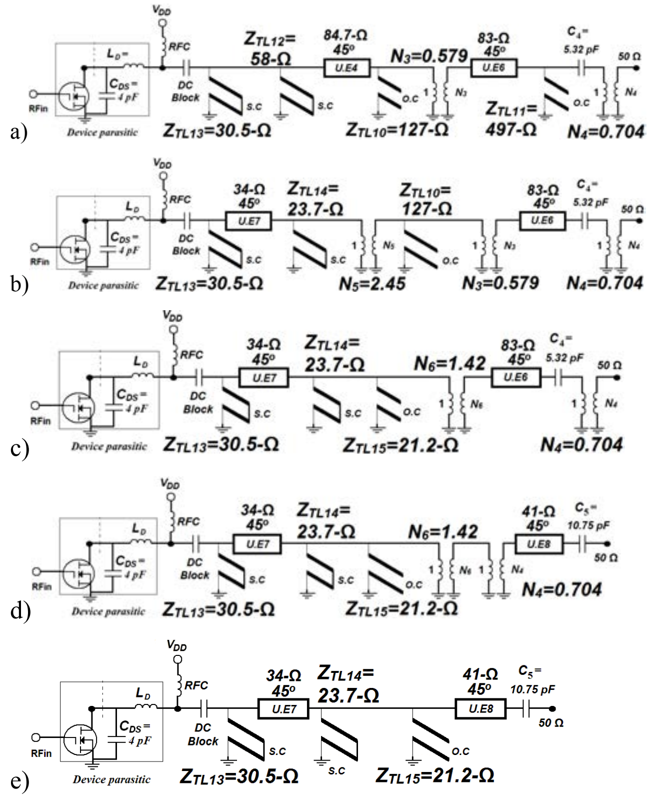

Fig.5. Transformers elimination sequence.

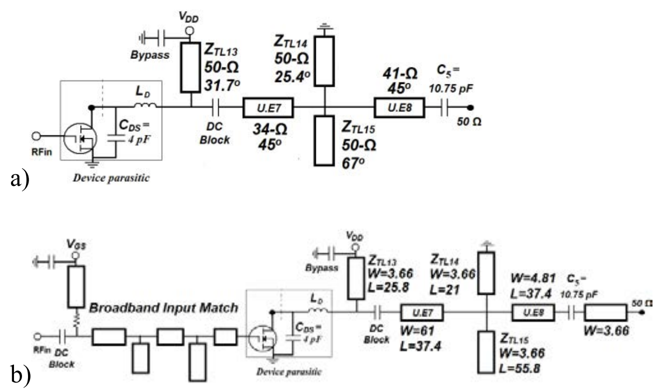

Fig.6. Final schematics for microstrip, widths and lengths in mm.

IV. Breadboarding and PA Performance

The amplifier schematic in Fig. 6b (units in mm), including the broadband input matching network are implemented using air-suspended brass-bars as shown in Fig 7. With no dielectric material the effect of dielectric loss and dielectric constant variation is eliminated. The shunt connected brass-bars can be moved along the straight line from drain to load for tuning purposes and then fixed with solder. Since the thicknesses of the TLs are comparable to their widths, Fig. 7, electromagnetic simulations are used to correct for their proper impedances.

The amplifier performance is shown in Fig. 8 and the measured 80% efficiency bandwidth is 33% (300-MHz) with an output power variation of 1.7 dB with 43 dBm at 1-GHz.

The breadboarding technique allows interchanging the bar-brass stubs with different lengths and widths for performance optimization. The gap between ground and the stubs can be easily controlled with small pieces of plastic boards. It is worth mentioning that no printed-circuit board processing is required and multiple transmission-line lengths and impedances can be made available to assist the tuning process.

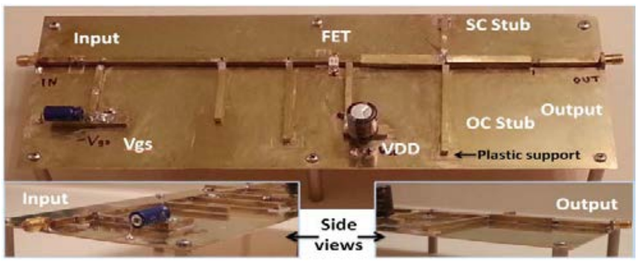

Fig.7. Transmission-line class-E amplifier prototype.

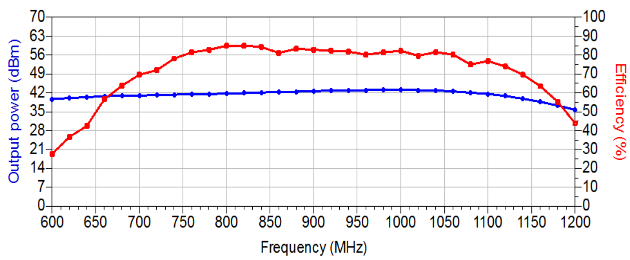

Fig.8. Measured output power and efficiency.

V. Conclusions

A transmission-line class-E amplifier can achieve wide bandwidths by judicious selection of its output network topology. A simple loading network topology can be modified using transmission-line transforms in order to provide virtual drain loading with the required impedance to produce the target output power with high efficiency in a wide frequency range. The breadboarding technique presented in this paper can be used as an alternative construction method of the circuit board that does not need printed transmission-line processing.

Acknowledgement

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