

ESD Considerations for SOI Switch Design

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This paper proposes a solution that employs transistor self-conduction and circuit design techniques to improve ESD performance for SOI RF switch applications. The primary limitations and challenges in the ESD design for SOI technology are discussed. The solution enables the switch to pass 8kV IEC as well as typical HBM standards.

THE MOTIVATION AND CHALLENGES

A common perception about Si technology is that the ESD performance should be better than that of the compound semiconductor. This is generally true for digital IO and typical rail-to-rail analog applications, as the methodology is pretty standard. However, as a switch or front end module is concerned, the SOI device faces the same challenges as pHEMT. In some applications, SOI is facing even bigger challenges than pHEMT. The main challenge is the thin oxide breakdown of the SOI technology. According to TLP characterization results, the gate of a pHEMT device can easily sustain 50V+ ESD transient voltage. The oxide of the 2.5V MOSFET in the SOI technology can only sustain 10V transient voltage at most. The gate-oxide breakdown voltage has become the primary ESD performance hurdle.

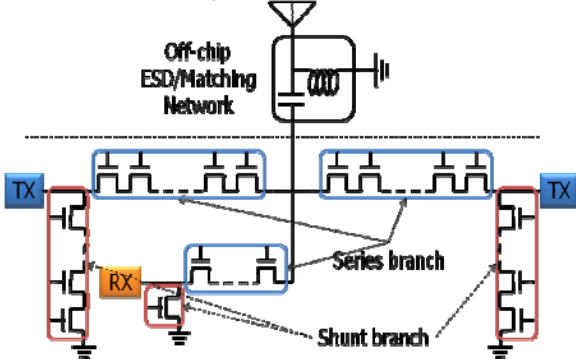


Figure 1: A typical RF switch schematic

Figure 1 shows a typical RF switch schematic for cellular handset applications. As far as a designer of an RF switch for the cellular handset application is concerned, the main objective is to pass IEC of 8kV or more. IEC requirements stand out from other ESD standards due to the very high peak current of ~4A/kV, the long lasting period in hundreds of nanoseconds, and thereby a very high total integrated energy. It is usually not feasible to design an integrated circuit on a modern semiconductor technology which was designed to enable high-

speed and high integration, and to pass such high rating. Therefore, external protection is needed to lower the electric shock to a more tolerable level that a modern semiconductor could take. However, even with a properly designed ESD network in the front, the energy passing through can still be very significant. Testing data show that some of the unprotected arms can pass only 1~2kV IEC even with the ESD network in the front.

Figure 2 shows the self-protection capability of the unprotected transistors from three different foundries. As observed in the figure, the normalized ESD tolerance of the 5V FET on a thick film SOI is about 2x that of 2.5V FET on a thin film. The thin film also limits the usefulness of the on-chip high-voltage (HV) silicon controlled rectifier (SCR) devices, which are often used as ESD protection devices when the system requires high trigger voltage and low holding voltage. Even with a proper snapback behavior, the SCR device on thin film silicon can only sustain a very small amount current of ~10mA/um before it is damaged or destroyed.

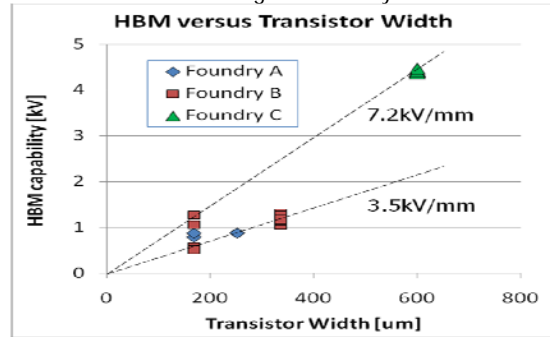


Figure 2: Self-protection capability of unprotected transistor of three different SOI technologies; foundry A & B manufacture 2.5V FET on thin film SOI, while foundry C manufactures 5V on thick film SOI.

Besides the intrinsic technology limitation, the system requirement also imposes constraints for ESD design of an RF switch. The most stringent one is its linearity requirement. A typical RF switch for a cellular handset application requires the inter-modulation level to be below -105dBm at a maximum output power of 35dBm. Given that an isolation of 30+V is required from either transmit or antenna port to ground, which is dictated by the RF signal amplitude appearing at the port at the output power level of 34dBm under a high voltage standing wave ratio (VSWR), any ESD protection device used there will need to behave completely linear or it can't be used at all.

ESD DESIGN CONSIDERATIONS

As mentioned earlier, it is not practical to expect the on-chip semiconductor device to survive very high system-level ESD testing like IEC without any external ESD alleviation. For most of the digital applications, such high energy is absorbed by external transient voltage suppressors (TVS). However, because of the nonlinearity introduced by the TVS at high power, this solution can't be used for very linear applications such as the RF switch used in handsets. Instead, an LC passive high-pass filter as shown in Figure 1 is employed to limit the bandwidth of the long lasting energy of an IEC event up to hundreds of nS to just a few nS. Such a network also improves the HBM robustness between RF to digital I/Os as it establishes ground connection between these two domains.

Even with such a passive network in the front, the energy passing through still has very high amplitude, e.g. a peak current of a few amps or a peak voltage of a couple hundred volts, although the period of the transient voltage spike is much shorter. Any weak arm needs to be protected. It is not a very difficult task for the RX ports as the potential RF signal swing is not high. It can be done with a pair of anti-parallel diodes shunting to the ground. The anti-parallel diode protection also helps suppress the residual voltage passing through to the next stage. However, as an RF signal swing of 30V is expected on the TX and antenna ports under a high VSWR condition, it is no longer feasible to use the stacked diode network for ESD protection. Given that the HV SCR device on a thin film technology is not strong enough for ESD protection, the protection can only be relied on the transistor's self-conduction, which is triggered by a fast transient such as that in an ESD event. However, the self-conduction of transistors is degraded and eventually limited by the number of the transistors in series due to voltage imbalance.

Figure 3 shows the maximum transient voltage of a long transistor chain as a function of the number of the transistors in series. As seen in the figure, the transient voltage tolerance is not linearly proportional to the number of transistors in the stack.

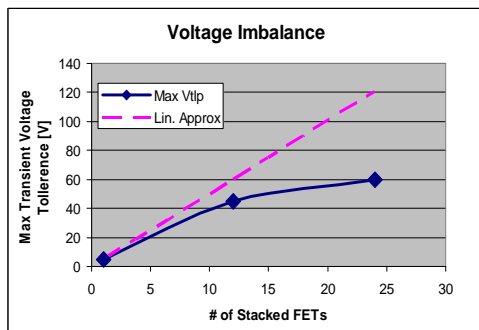


Figure 3: Measured maximum transient voltage tolerance of a long transistor chain as a function of the number of the transistors in series.

This reaches a saturated value very quickly because the transient voltage rise of an ESD event does not get evenly

distributed along the long chain. The first transistor suffers a much higher voltage stress than the one at the end, as it takes a certain amount of time to charge up every transistor in the chain and establish self-conduction from the beginning to the end to alleviate the ESD stress. The longer the chain, the longer the charging time is needed for all of the transistors to be turned on. Whenever the terminal voltage of the very first transistor in the chain reaches the oxide breakdown, the whole chain gets blown away.

ESD ENHANCEMENT METHODOLOGY

To mitigate the problem, we propose a methodology that add a capacitor ladder to balance the transient voltage distributed along the chain, as shown in Figure 4. The capacitor ladder helps the bottom transistor in the chain turn on quickly, therefore enabling the self-conduction of the whole transistor chain evenly to alleviate an ESD strike.

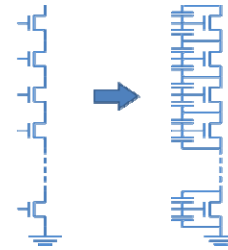


Figure 4: Add capacitor ladder to improve the robustness of a long transistor chain.

Figure 5a shows the measured maximum tolerable TLP voltage as a function of the value of ladder capacitance. As shown in the figure, without capacitor ladder, both 8- and 12-transistor arms fail at similar voltage as a result that the first transistor blows off before the whole chain gets into self-conduction. As the capacitor ladder facilitates the self-conduction of the bottom part of the chain, the transient voltage becomes more evenly distributed so that the sustainable voltage increases. The sustainable voltage eventually saturates as the chain reaches its full strength as dictated by the number of the transistors in the chain as shown in the 8-transistor chain. Figure 5b shows the ESD protection capability of a long series transistor chain can be improved by more than 10x with the capacitor ladder; however, it is at the cost of a significant amount of chip area increase.

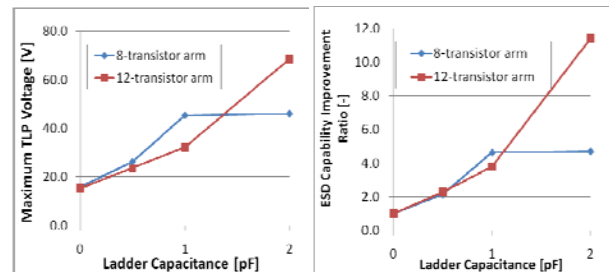


Figure 5a: Maximum tolerable TLP voltage as a function of the value of C_{ladder} . 5b: ESD capability improvement ratio as a function of the value of C_{ladder} .