

# A Comprehensive PHEMT Core Model For Switch Applications

Ce-Jun Wei, Yu Zhu, Hong Yin, Olesky Klimashov, and Dylan Bartle

Skyworks Solutions Inc. 20 Sylvan Road Woburn, MA 01801 USA  
20 Sylvan Road, Woburn, MA 01801, USA

**Abstract** — A comprehensive non-linear PHEMT core model for switch applications is described. The model combines an accurate description of CV below pinch-off and a 2D CV function above pinch-off for better charge and capacitance modeling. At the same time, more accurate is the model's IV prediction on the current in the near pinch-off region. The model has detailed leakage equations and dispersion function covering a wide range of operation, and taking gate lag into consideration. The model was verified by a variety of measured data, including IV/transfer curves, leakages, floating voltages and S-parameters/CV curves. In a switch application, comparison between modeled and measured data on harmonics, insertion loss and isolation regarding various driving power shows excellent and consistent agreement in both on-state and off-state.

## I. INTRODUCTION

Although many compact models for PHEMT's have been published and have been incorporated into most popular automated design software applications, few of these models could be used for switch design in wireless communications. For example, PHEMT multi-mode multi-throw switches operating at off state with bias far below pinch-off have very low harmonics down to -50>-60dBm for drive power of 35dBm. The only nonlinearity comes from the gate capacitance as a function of gate bias. Therefore, accurate modeling of CV relation below pinch-off is critical. Unfortunately most popular models assume that the capacitance is either, when below pinch-off, a constant that makes the model inaccurate or, when near/below pinch-off, a 2-D function that exaggerates the harmonics owing to troublesome associated trans-capacitances. Simulation of switch circuits using these models can often predict much higher harmonics than measured by up to 20dB! Proper modeling of leakages and their partition are also crucial in multi-gate switch modeling. Again most of the existing models lack accurate description of leakages. Another issue for switch applications is that the device normally is operated at Vds=0 and at this point the model is symmetric and can be swapped between drain and source. Gummel Symmetry Test (GST) must be satisfied by the model so that the derivative at Vds=0 could be ensured to be continuous up to 3<sup>rd</sup> order or higher.

Dispersion description is required not only at active and on-state region but also at pinch-off region. Gate-lag effects have an impact on the transition from off-state to on-state. Therefore comprehensive PHEMT modeling is indispensable for switch application. The requirement for core model is summarized as follows:

- Accurate modeling of C(V) below pinch-off
- Smooth transition from 2D CV function above pinch-off to 1D function below pinch-off. 2D CV functions are used since the RF Vds swing could be very high and there is

non-zero internal DC Vds of stacked FET for a multi-gate FET.

- Accurate modeling of IV around sub-pinch-off region
- Accurate modeling of gate leakages and drain-source leakages
- Bias-dependent dispersion, including gate-lag

We have developed a new PHEMT model for switch applications [2,4] as well as for LNA applications[3]. The model has many features including comprehensive and distributed extrinsic model. The core model meets all above challenges and the model has been incorporate into company's design kits in ADS and GoldenGate/Cadence. It is proven to be robust. In this paper we'll address the issues and solutions related to the *intrinsic* part of the PHEMT model. The extrinsic part and multi-gate device modeling were and will be continuously presented elsewhere[5].

## II. CAPACITANCE/CHARGE MODEL

A typical Cgs(Vgs) or Cgd(Vgd) at Vds=0 is shown in figure 1. The pinchoff voltage Vp is around -1 V. The Cgs increases quickly with Vgs when Vgs is crossing Vp. The Cgs continues to rise with Vgs after Vp but more slowly depending on Vgs. A proper description of Qg(V) has two parts, Qg1(x) and Qg2(x), dedicating to Vgs<Vp and Vgs>=Vp correspondingly, where x stands for Vgs or Vgd.

The first part is always a one-dimensional function, to cover different technologies we introduced more parameters. The expression is as follows.

$$Qg1(x) = C_{-o} + \frac{C1 \times (v(x) - Vp)^2}{2} + \frac{C1a \times (v1(x) - Vt1)^2}{2} + \frac{C2a \times (v1(x) - Vt1)^3}{3} + Cea \times d_{ve} \times e^{-\frac{v(x)-Vp}{dve}} \quad (1)$$

where

$$v(x) = \frac{x + Vp - \sqrt{(x + Vp)^2 + del^2}}{2} \quad (2)$$

and

$$v1(x) = \frac{x + Vt1 - \sqrt{(x + Vt1)^2 + dela^2}}{2} \quad (3)$$

C1 is the coefficient of capacitance linearly decreasing with negative Vg starting from Vp with transit voltage del. Cea is the coefficient of exponentially decreasing capacitance with decreasing distance d<sub>ve</sub>. C1a is the linear coefficient and C2a is the second order factor in capacitance-voltage curve starting at Vg=Vt1 with smoothing voltage, dela.

The derivative of Qg1(x) leads to below-pinchoff gate capacitance Cg1(x). The second part of charge can be represented as follows:

$$Qg2(x) = C10 \times d1 \times \ln(1 + e^{-\frac{x-Vp}{d1}}) + C0 \times Vbi \times \frac{(1 + \frac{u(x)}{Vbi})^{1-m0}}{m0 - 1} \quad (4)$$

where

$$u(x) = \frac{x + V_p + \sqrt{(x + V_p)^2 + del^2}}{2} \quad (5)$$

Similar to that of  $Qg1(x)$ , the first-order derivative of  $Qg2(x)$  defines the above-pinchoff gate capacitance  $Cg2(x)$ . The fitting curve (line) compared to measured curve (symbol) for a PHEMT device is shown in Figure 1.

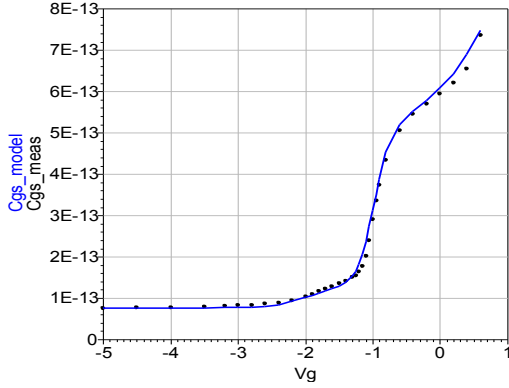


Figure 1. Gate Capacitance- $Cgs$  as function of  $Vgs$  for  $Vds=0$  for a PHEMT Device. Line: modeled, symbol: measured

The charge-capacitance model above fits the  $Cgs(Vgs)$  and  $Cgd(Vgd)$  very well at  $Vds=0$ . For other than  $Vds=0$ , the capacitance and charge above pinch-off become a two-dimensional voltage function. That is to say,  $Cgs$  is not only a function of  $Vgs$  but also a function of  $Vds$ . For capacitance based model, we use the following equations to replace  $Cg2$  in the Cold-FET case mentioned above.

$$Cgd2 = Cgd1 \times f1 + Cgs1 \times f2 + \frac{Cp2(Vgs) \times e^{-cvd \times Vds}}{1 + e^{-\frac{(Vgd - v_t)}{del2}}} \quad (6)$$

$$Cgs2 = Cgd1 \times f2 + Cgs1 \times f1 + \frac{Cp2(Vgd) \times e^{cvd \times Vds}}{1 + e^{-\frac{(Vgs - v_t)}{del2}}} \quad (7)$$

Where

$$Cp2(x) = \frac{Co}{\left(1 + \frac{x}{Vbio}\right)^{mo}} \quad (8)$$

$$Cgs1 = C11 + C12 \quad (9)$$

$$Cgd1 = -C12 \quad (10)$$

Here  $C11$ ,  $C12$  are defined identically to what those in EEHEMT charge model are defined.

The model in active region ( $Vgs > Vp$ ) differs from EEHEMT model is additional charge term  $Cp2 \times exp$  term that depends on  $Vds$  as well.

The fitting can be reasonably good over a wide bias range as shown in figure 2. The fitting range covers  $Vds$  from 0V to 2 V step 0.2 V and  $Vgs$  from -1.4V to 0.6V step 0.05V or 0.1V.

Since there are no unified equations to cover both the active region and the cutoff region (below  $Vp$ ), the combination of two charge/capacitance models are important and poor transition can affect the switch modeling results. For capacitance based model it is simpler and straightforward. The Capacitances can be combined as follows:

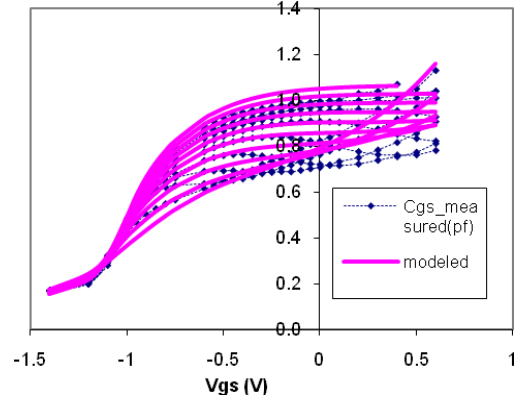


Figure 2. Gate Capacitance- $Cgs$  as function of  $Vgs$  at  $Vds=0$  to 2 V step 0.2V for a PHEMT Device. Line: Modeled, symbol: Extracted from S-parameters:

$$Cgs = \frac{Cg1(Vgs)}{1 + e^{\frac{Vgs - Vp}{d2}}} + \frac{Cgs2}{1 + e^{-\frac{Vgs - Vp}{d2}}} \quad (11)$$

$$Cgd = \frac{Cg1(Vgd)}{1 + e^{\frac{Vgd - Vp}{d2}}} + \frac{Cgd2}{1 + e^{-\frac{Vgd - Vp}{d2}}} \quad (12)$$

Owing to surface trapping effects, the large-signal RF swing may see different CV dependence. To address this issue, we introduced another parameter  $_Cc$ . In varying parts of CV characteristics,  $Vgs$  are replaced by an effective gate-source voltage  $Vgse$  which is defined as follows:

$$Vgse = _Cc \times Vgso + (1 - _Cc) \times Vgs \quad (13)$$

In a similar method, we also define an effective gate-drain voltage  $Vgde$  to replace  $Vgd$  in the CV characteristics. In this way, the small-signal CV remains the same, but large signal  $Cgs$  will be reduced by  $1 - _Cc$  factor.

In the charge model, we can use similar transition functions for  $Qg1$  and  $Qg2$  as (11) and (12). Caution must be taken over capacitances in the vicinity of  $Vp$ . (11) and (12) have denominators involving voltage differences,  $Vgs - Vp$  and  $Vgs - Vp$ , and their derivatives may become huge in the transition region near  $Vp$ . To diminish this effect, we modified the gate charge definition  $Qg$  into the following form:

$$Qg = Qg1(Vgs) + [Qg2(Vgs) - Qg2(Vp)] \times f(Vgs) \quad (14)$$

Where  $f(vgs)$  is a transition function  $-1/(1 + \exp(-(Vg - Vp)/d2))$ . As a result, the capacitance is derived as the derivative of charge term:

$$Cgs = \frac{\partial Qg}{\partial Vgs} = Cg1(Vgs) + Cgs2 \times f(Vgs) + [Qg2(Vgs) - Qg2(Vp)] \times f'(Vgs) \quad (15)$$

The smoothing action results in the last term in (15). This term is an extra contribution to the previously defined  $Cgs$ . But it stays very small at all  $Vgs$  since the factor  $[Qg(vgs, Vds) - Qg(Vp, Vds)]$  is close to 0 when  $Vgs$  is close to  $Vp$ , and  $f'(Vgs) \approx 0$  at elsewhere.

### III. IV modeling

Most advanced models can generate good fitting in IV curves. Considering the best convergence, we borrowed Symmetric Angelov IV model [4] as starting model that has good description of self-heating effects on  $I_{max}$ ,  $Vp$  and other parameters. However, Angelov model is implicit in terms of pinchoff. It is not

directly accessible to the pinchoff parameter and performance near sub-threshold region.

The IV equations are a modified Angelov symmetric model [1] and they can be expressed as:

$$I_{ds} = I_{dsp} - I_{dsn} \quad (16)$$

where

$$I_{dsp} = \frac{I_{max}}{2} \times (1 + \tanh(\phi p)) \times fp(V_{gs}) \times (1 + \kappa \times V_{ds}) \tanh(\alpha(V_{gs}) \times V_{ds}) \quad (17)$$

The equation contain similar terms,  $\phi p$ ,  $\phi n$  as in Angelov model, but we add additional terms to account for cutoff near pinchoff.

$$fp(x) = 1 / (1 + e^{\frac{V_p - x}{dV_p}})^{-n} \quad (18)$$

$I_{dsn}$  is the same as  $I_{dsp}$  but it replaces  $V_{gs}$  with  $V_{gd}$  and  $V_{ds}$  with  $-V_{ds}$ .

Another modification is slope function, the equation  $\alpha(x)$  describes the vgs dependence of slope parameter at linear region. It is written as follows:

$$\alpha(x) = \alpha_0 + \theta \times (0.9 - x) + \phi p \times 0.5x [1 - \tanh(\frac{x - V_p}{dv_2})] \quad (19)$$

The  $\alpha_0$  is the slope at the linear region of the DCIV curve at  $v_{gs}=0.9$ , and  $\phi p$  is the slope at below and near  $V_p$ . This parameter not only fits the slope at low vgs region but also fits the real part of S-parameters in the range near and cross  $V_p$ .

The model apparently satisfies the GST condition since both  $I_{dsp}$ , and  $I_{dsn}$  are continuous and best conditioned functions. We should point out that the self-heating effects are incorporated with a sub-thermal circuit that defines the junction temperature rise. In the model,  $I_{max}$ ,  $V_t$ ,  $V_p$  and  $C10$  are all functions of junction temperature  $T_j$ . The dependence of  $I_{max}$  on  $T_j$  results in a drop of  $I_{ds}$  at saturation and high power region. Combined with device thermal conductance model, the model can give good fitting for various size and configuration of devices

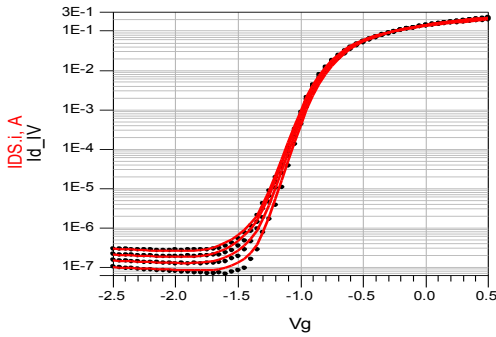


Figure 3. Comparison of modeled and measured transfer curves for a PHEMT Device.  $V_d=1,2,3$  and  $4V$ . Line: modeled, symbol: measured

In the above equations the parameter definitions were not given and the authors assume they are self-explanatory.

Figure 3 show the fitting of transfer curves in log scale,  $V_d=1$  to  $4 V$  step  $1V$ . It is shown that the model fitting around  $V_p$  is excellent. Figure 4 shows modeled and measured  $S_{21}$  for a series connected PHEMT, the gate is connected with  $7.5 K\Omega$  resistor and biased from  $-3V$  all the way to  $0.2V$  across  $V_p$  region.  $S_{21}$  is the transmission from source to drain. The parameter of  $\phi p$  fits the real part of  $S_{21}$  when  $V_{gs}$  cross  $V_p$ .

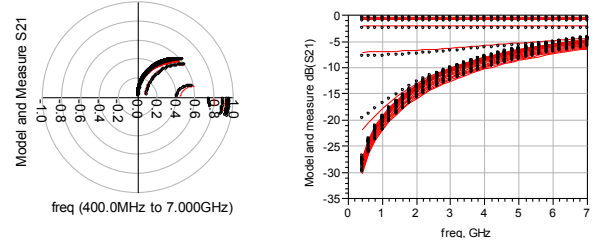


Figure 4. Modeled (line) versus measured S-parameters (symbol) for a series connected PCM SG-PHEMT as a function of  $V_g$  (from  $-3V$  to  $0.2V$ ) at  $V_{ds}=0$

#### IV Leakage model

Leakage fitting is important especially for multigate FETs where the internal channel is floating. The internal gate-channel voltage is dependent on the partition of leakages between gate-channel and drain/source to internal channel.

The GD or GS leakage are expressed as three components that dominated at lower, medium and high negative  $V_g$  area.

$$\frac{1}{i_{gs\_lk}} = \frac{1}{i_{gs\_lkl}} + \frac{1}{i_{gs\_lkm}} + \frac{1}{i_{gs\_lkh}} \quad (20)$$

where  $i_{gs\_lkl}$ ,  $i_{gs\_lkm}$ ,  $i_{gs\_lkh}$  are diode-like gate currents at lower, medium and high negative vgs regions.

In this model, DS leakage near pinch-off is a 2-D function of  $V_{ds}$  and  $V_{gs}/V_{gd}$ :

$$I_{ds\_lk} = I\alpha \times e^{N\alpha \times v(vg1)} \times [e^{(N\alpha 2 - M\alpha \times v(vg1)) \times V_{ds}} - 1] + \frac{I\beta \times \tanh(K\beta \times V_{ds})}{1 + e^{\frac{V_{go} - V_{g1}}{dV_g}}} \quad (21)$$

With  $vg1$  as  $V_{gs}$  at non-negative  $V_{ds}$  and as  $V_{gd}$  at negative  $V_{ds}$  and with  $v(x)$  defined in (2).

DS leakage in the high  $V_{ds}$  region follows a diode-like relation:

$$I_{d\_high} = I_{ho} \times (e^{N_{dh} \times V_{d}} \lim - 1) \quad (22)$$

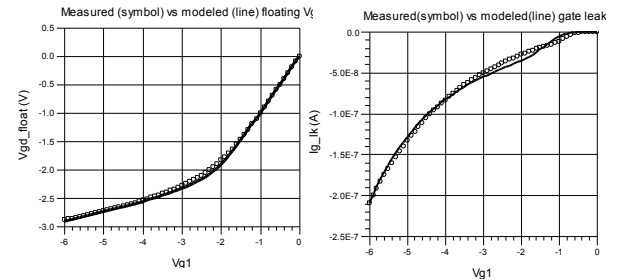


Figure 5: Modeled (line) versus measured (symbol) gate leakage and floating voltage for a PCM PHEMT Device.

Where

$$V_{dlim} = \frac{V_d - V_b + \sqrt{(V_d - V_b)^2 + del^2}}{2} \quad (23)$$

Here  $V_b$  is the starting point of DS breakdown. The fitted gate leakage and floating gate-to-drain voltage at drain open condition is shown in figure 5. Since the internal channel nodes of a multi-gate switch FET at off state are floating, precise models of leakages are critical to accurate prediction for the whole device.

### III. DISPERSION MODEL

We define a bias dependent feed-forward factor,  $cfw$  and feedback factor  $cbk$  to address the difference in RF  $G_m$  and RFGds from DCGm and DCGds respectively. There are three slow RC time constant circuits at gate-source/gate-drain branches and drain-source branch. The currents flowing through GS and GD RC branches generate feed-forward voltages on the gate and hence alter the  $G_m$  at  $v_{ds} > 0$  as the GS branch feed-forward excitation and  $v_{ds} < 0$  as the GD feed-forward excitation. On the other hand, the DS RC branch has feedback voltage added to the gate and thus alters the RF- $G_{ds}$  curves. The corrected input to the gate would be as follows:

$$v_{gt} = v_g + cfw(V_{gso}, V_{dso}) \times v_{gs\_rf} + cfw(V_{gdo}, V_{dso}) \times v_{gd\_rf} + cbk(V_{gso}, V_{dso}) \times v_{ds\_rf} \quad (24)$$

Here,  $V_{gso}$ ,  $V_{gdo}$  and  $V_{dso}$  are the DC components of  $v_{gs}$ ,  $v_{gd}$  and  $v_{ds}$ .  $v_{gs\_rf}$ ,  $v_{gd\_rf}$  and  $v_{ds\_rf}$  are their corresponding rf or ac components. When  $V_{gso}$  or  $V_{gdo}$  is below pinch-off, the  $cfw$  describes the gate lag.

### VI. MODELED HARMONICS AT SWITCH CONDITION

The model was validated for a SG-PHEMT in a switch configuration. The PHEMT is in a series connection configuration. Namely the RF feeds on source side and output at drain side. The gate is a meander line connected with a 7kOhm bulk resistance. When the gate bias is at  $V_g = 0$ , it is at switch on-state, whereas it is at switch off-state when the  $V_g = -3V$ . Swept power from 15dBm to 30dBm at  $f = 0.9GHz$  was applied the device. The configuration is shown in figure 6.

Figure 7 shows the output power, 2nd and 3rd harmonics against input power when switch is on, i.e.  $V_g = 0$ . Excellent coincidence between measured (symbol) and modeled (line) is achieved. Insertion loss as function of  $P_{in}$  can be also seen from  $P_{out}$  curves. Figure 8 shows the output power, 2nd harmonics and third harmonics against input power when switch is off, i.e.  $V_g = 0$ . Agreement between measured (symbol) and modeled (line) is also achieved. Isolation as function of  $P_{in}$  can be also seen from  $P_{out}$  curves.

### IV. CONCLUSION

A comprehensive PHEMT core model has been developed for switch applications. The model was validated by a variety of characteristics, including IV curves, S-parameter in linear region, CV curves below and above pinch-off, floating voltages, and leakages. At the same time, predictions of this model exhibit excellent agreement with measured data including insertion loss, isolation and harmonics at power drive condition.

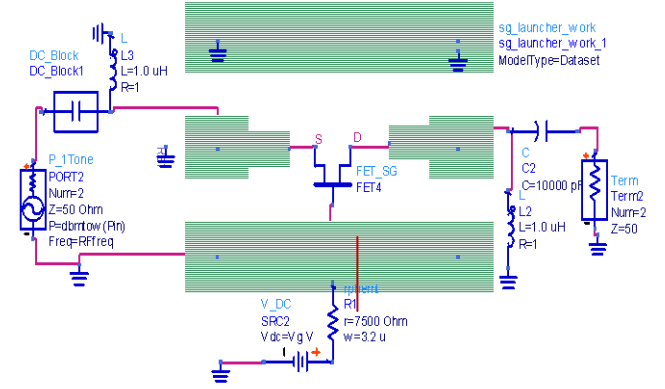


Figure 6. Simulation bench of power drive for a series connected PCM PHEMT used in a switch configuration.

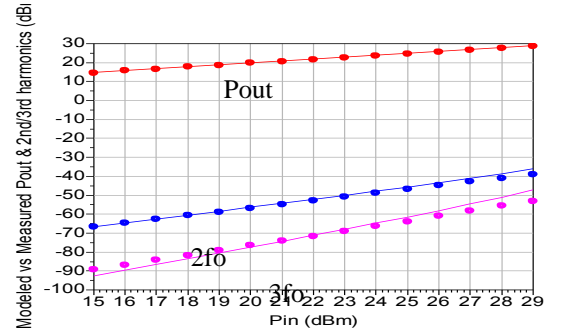


Figure 7. Models (line) versus measured (symbol)  $P_{out}$ , 2<sup>nd</sup> and 3<sup>rd</sup> harmonics versus input power at  $V_g = 0$  or on state.  $f = 0.9 GHz$ .

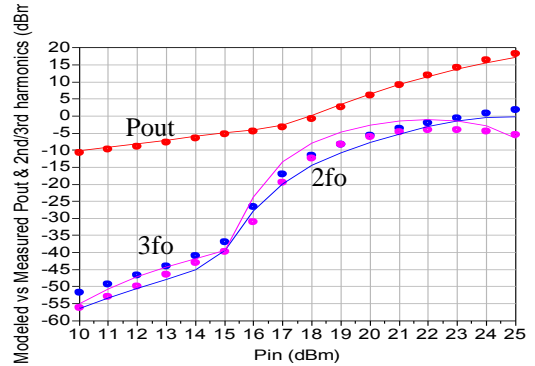


Figure 8. Models (line) versus measured (symbol)  $P_{out}$ , 2<sup>nd</sup> and 3<sup>rd</sup> harmonics versus input power at  $V_g = -3 V$  or off state.  $f = 0.9 GHz$ .

### Reference

1. I. Angelov, L. Bengtsson, M. Garcia, "Extensions of the Chalmers Nonlinear HEMT and MESFET Model," *IEEE MTT* Vol. 44, No. 10, October 1996.
2. C.-J. Wei et al, "Analysis and modeling on linearity of multi-thru TX/RX switches," Proc. 3<sup>rd</sup> MAPE 2009, pp.5-8, Oct. 27-28, 2009, Beijing.
3. C.-J. Wei, Yu Zhu et al, "Scaleable Two-Current Low-Noise PHEMT Model that Predicts IP3," 2008 APMC at Hong Kong, Dec. 2008
4. C.J. Wei et al, "Large-Signal PHEMT Switch Model Accurately Predicts Harmonics and Two-Tone Intermodulations," MTT-Symposium, Long Beach, June 12-17, 2005
5. C.-J. Wei et al, "Distributed Switch FET Model that predicts Better Insertion Loss and Harmonics", 2010 EUMW, Paris