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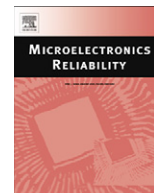

Measuring seam/crack formation in interconnect metallization

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ABSTRACT

Low cost processes, in both GaAs and Silicon, often use non-planar interconnect metals. While very efficient in simplifying processes, seam (more commonly called "crack") formation due to inter-level dielectric topologies can (1) cause significant thinning in the metallization, impacting the reliability and (2) act as process defects that reduces circuit yield. To better understand and monitor crack formation, we used a series of test structures to develop an electrical test allowing crack formation to be characterized. We confirmed our results with cross sections. The methodology presented here is also used to characterize new process steps or processes to verify the new process make cracking worse. In the first application of this method, it highlighted a potential cracking issue, preventing it from propagating into production.

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1. Introduction

The formation of metal seams (so-called "cracks") that result from non-planar back-end of line (BEOL) metallization can create reliability and yield risk for integrated circuits. In particular, the seams/cracks result in a significant thinning of the interconnect metal that increases the resistance of the line. Since the resistance and current carrying capability are dependent on the cross-sectional area, this is potentially dangerous for metals lines containing these seams (or devices like inductors and capacitors that also contain them). In the extreme case, these seams can cause open circuits, impacting the circuit yield. While "after the fact" cross sectional analysis can identify these problems, it is not capable of giving statistical information on the extent of cracking or how it impacts things electrically. Process engineers typically attempt to use via chains to assess these cracks, but those structures generally only find gross opens and do a poor job of isolating the seams because they are more dependent on the actual interconnecting metals. To allow collection of electrical data related to seam formation, we designed, tested, and experimented with a number of structures to (1) characterize the degree of cracking in current processes, (2) guide the development of new processes to minimize the seams, and (3) highlight required design rules in newly developing processes. The application and analysis of these structures is presented here and leads to identification of a more compact subset of structures useful for statistical data collection. The results were also confirmed by cross-sectional analysis and led to relevant design rules for inductors in a new process we were developing.

2. Test structure development

2.1. Test structure design

There were several considerations for developing structures to measure the metal seam formation. First, we need to find the sheet resistance and the effective electrical width of the drawn lines. These can be quite different from blanket process control wafer results and the narrow lines vary from "as-drawn", especially for evaporated metals. For this purpose, long metal lines with different widths were used (all test structures used in this experiment were carefully layed out in Kelvin probe patterns), similar to those used in the cross-bridge structures in [1]. Kelvin probing eliminates any error due to contact resistance and the "T" in the structure is placed so that the vias and pads connecting to the lines do not enter into the measurement (the reference plane for the measurement is at the beginning of the metal line itself). The pads and connecting vias used layouts (since they are not space constrained) to minimize the impact of seams and the pad and top and bottom of the measurement lines. These structures are referred to as R_{METAL}. Second, we wanted to have structures that would isolate the resistance of the "crack" region inside the vias. Noticing our MIM capacitors and vias are very similar (the only difference is that the MIM does not have an opening in the thin lower dielectric), patterns based on M2 running into and out of such vias are used. The MIM patterns are labeled MIM and via patterns are labeled VIA. The important factors we started with were metal line width, number of vias, and length via length, as defined in Fig. 1. The metal width is included for the MIM, VIA, and NO_M1 structures because of the supposition that the seam formation is width dependent (this is later shown to be false). Similarly, the via length was investigated because it could have an impact on the topology (this also turned out to be unimportant). While it would appear

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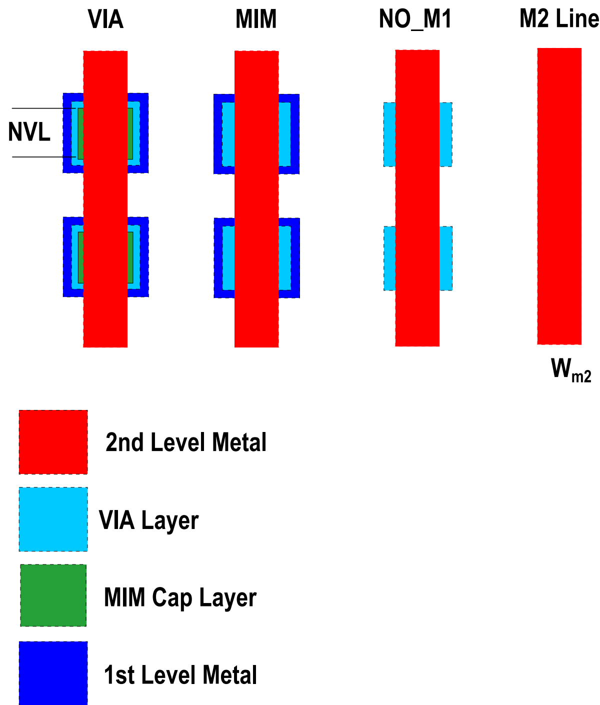

Fig. 1. Top view of the various structures. VIA includes vias along the metal line, MIM structures are the same as VIA except there is MIM cap layer separating M1 and M2, NO_M1 has via opening only, the M2 line is an M2 line of with W_{m2}.

obvious we would only need to use the MIM style structure, we wanted to verify that the profiles obtained by these structures were similar so both were tested and analyzed. Because of how the interlevel dielectric planarizes in this process, the worst case structure would be a via with no metal underneath it (this allows the dielectric to be at its full thickness rather than thinned because of topology). These are labeled as NO_M1. The NO_M1 type via had been previously recommended for tacking down long metal lines that occasionally had lift-off issues and could occur in inductor layouts unless there are rules to prevent it. Fig. 2 is a representative cross section of the VIA style structure that shows the definition of the terms used for modeling the cracks. Eq. (3) is based on the

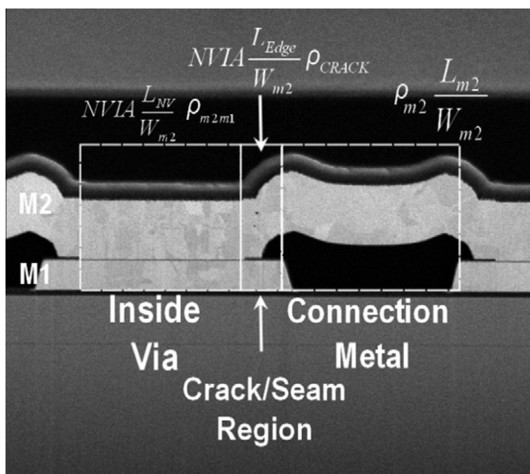

Fig. 2. Cross section showing the physical regions corresponding to the terms in Eq. (3). The region on the left is the 3rd term and is the region inside the via. The region on the right is the metal interconnect (M2) in between the vias. The region in the middle is defined as the "crack" region (from the end of the via to the edge of the M1).

Table 1
Wafer averaged measured data for all structures.

Style	W2_width	NVIA	NVL	Resistance
MIM_2 25_4_2	2	25	4.2	5.645125831
MIM_2_25_2.2	2	25	2.2	5.657401989
MIM_2_50_2.2	2	50	2.2	6.027292133
MIM_2_75_2.2	2	75	2.2	6.348355881
No via_2	2	0	0	5.258199125
No via_2.5	2.5	0	0	3.975322294
No via_3	3	0	0	3.196526938
NO_M1_2_75_2.2	2	75	2.2	7.704282521
NO_M1_2_25_4.2	2	25	4.2	5.962362818
NO_M1_2_50_2.2	2	50	2.2	6.924714929
NO_M1_2_25_2.2	2	25	2.2	6.020084049
VIA_2_25_4.2	2	25	4.2	5.321300117
VIA_2_25_2.2	2	25	2.2	5.540176072
VIA_2_50_4.2	2	50	4.2	5.230586105
VIA_2_50_2.2	2	50	2.2	5.718100476
VIA_2_50_2.2	2	50	2.2	5.681946614
VIA_2_100_2.2	2	100	2.2	5.952642616
VIA_2.5_50_4.2	2.5	50	4.2	4.022458962
VIA_2.5_50_2.2	2.5	50	2.2	4.384952225
VIA_2.5_100_2.2	2.5	100	2.2	4.602225723
VIA_3_50_4.2	3	50	4.2	3.168691937
VIA_3_50_2.2	3	50	2.2	3.484859553
VIA_3_100_2.2	3	100	2.2	3.7029189

definitions in Fig. 2. Only the standard via type structure was laid out at different widths for comparison to metal lines. These structures were all Kelvin probed and the resulting resistance measurement is shown in Table 1. The table also shows the three metal widths used (W_{m2}), the number of vias of the different styles (NVIA), and length of the vias (NVL). The length of the M2 used for all structures was 633.5 µm. Analysis and discussion of this data is presented in the next section.

2.2. Structure measurement and analysis

All structures were tested and the wafer average is used for analysis. The measured values are shown in Table 1. The data values are consistent. The metal lines have the lowest resistance and the resistance decreases with larger widths. The NO_M1 lines show the highest resistance followed by the MIM structures. The VIA structure has the next lowest. Increasing the number of vias increased the resistance for all of the structures. For the structures where M1 is not connected underneath (NO_M1 and MIM), the via length did not have a significant effect on the resistance. Since the data set is consistent, we can now proceed with data analysis.

To start our analysis, we first need to determine the width correction (for M2) as well as the sheet resistance. The metal lines with different drawn widths allow the actual on-wafer metal width and the sheet resistance to be extracted from:

$$R_{\mathrm{METAL}} = 2R_{\mathrm{contact}} + \rho_{\mathrm{m2}} \frac{L_{\mathrm{m2}}}{W_{\mathrm{m2}} + dW} \quad (1)$$

where R_{METAL} is the measured resistance, R_{contact} is the contact resistance, ρ_{m2} is the metal two sheet resistance, L_{m2} is the length of the measured metal line, W_{m2} is the drawn $M2$ width and dW is the correction. In this case, we used metals of width 2, 2.5, and 3 µm. The L was fixed at 633.5 µm for all structures. Assuming the R_{contact} is negligible and taking the reciprocal we get:

$$\frac{1}{R} = \frac{1}{L_{\mathrm{m2}}\rho_{\mathrm{M2}}} W_{\mathrm{m2}} + \frac{1}{L_{\mathrm{m2}}\rho_{\mathrm{M2}}} dW \quad (2)$$

Plotting $1/R$ vs. W_{m2} we find the intercept and the slope. Dividing the intercept by the slope a dW of −0.45 µm is found. Part of this offset is because the lift-off metal has the shape of a trapezoid as shown in Fig. 3 and the bottom width is targeted as the "as-drawn"

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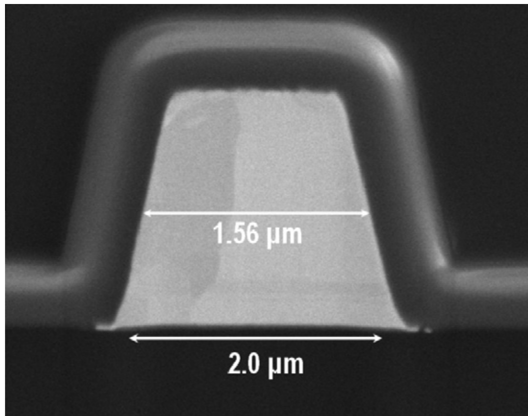

Fig. 3. Cross section of metal 2 line structure showing the trapezoidal shape of the metal.

width. The electrical measurement and the physical cross-section, which shows $dW = -0.44$ µm, are in excellent agreement, supporting the extraction method. The reciprocal of the slope divided by the length is just the sheet resistance, ρ_{m2}, and is 12.9 mOhms, close to the expected value. We will use this width correction, dW, and sheet resistance in subsequent calculations. After cross section, we determined we did not need to make any thickness corrections since the thickness was very close to nominal (2 µm).

With these values, we now turn to analyzing the structures with "cracking." Eq. (3) shows the terms in the resistance based on analysis of Fig. 2 (a VIA type structure). The first term is the total contact resistance. The second term is the resistance from metal 2 outside of the via or crack region. The third term is the total resistance from the metal inside the via region (in this case it is M2 in parallel with M1 written as M2||M1, for the MIM structure it is just M2) and the final term is the total resistance due to seam formation.

$$R_{total} = 2R_{contact} + \rho_{m2}\frac{L_{m2}}{W_{m2}} + NVIA\frac{L_{NV}}{W_{m2}}\rho_{m2m1} + NVIA\frac{L_{Edge}}{W_{m2}}\rho_{CRACK} \quad (3)$$

Resistance = Resistance_Between+Resistance_In+Edge

R_{total} is the resistance for the most general case where we have an M2 metal line that includes M1M2 vias underneath it (that connect to first level metal), where $R_{contact}$ is the contact resistance (should be small since this is Kelvin probed), ρ_{m2} and ρ_{m2m1} are the sheet resistances of M2 and M2||M1 respectively, L_{m2} and W_{m2} are the length and widths of M2, NVIA is the number of vias, L_{NV} is the length of the nitride opening between M1 and M2 of the via. Finally, ρ_{crack} is the resistance of the crack (two per via). Examining Eq. (3), we note that it reduces to:

$$R_{MIM} = 2R_{contact} + \rho_{m2}\left[\frac{L_{m2}}{W_{m2}} + \text{NVIA}\frac{L_{NV}}{W_{m2}}\right] + 2\text{NVIA}\frac{L_{Edge}}{W_{m2}}\rho_{CRACK} \quad (4)$$

for the MIM cap structure since only M2 is inside the via region. We also note that the M2 line resistance of Eq. (1), R_{METAL}, can be rewritten in this same form as Eq. (4):

$$R_{METAL} = 2R_{contact} + \rho_{m2}\left[\frac{L_{m2}}{W_{m2}} + \text{NVIA}\frac{L_{NV}}{W_{m2}}\right] + 2\text{NVIA}\frac{L_{Edge}}{W_{m2}} \quad (5)$$

From the earlier observation that the length of the via has no impact, the only remaining difference between the MIM and the metal line of the same width should just be the "crack" region. This can also be noted by comparing Eqs. (4) and (5).

Subtracting R_{METAL} (Eq. (5)) from R_{MIM} (Eq. (4)) and rearranging we get:

$$\rho_{CRACK} = \frac{(R_{MIM} - R_{METAL}) \cdot W_{m2}}{2\text{NVIA} \cdot L_{Edge}} + \rho_{m2} \quad (6)$$

Substituting the values for W_{m2} ($W - dW$) and ρ_{m2} we found before, gives a crack sheet resistance of 22 mOhm/sq where we have used the ledge (1.29 µm) from cross sectional data – compared to the 1.4 µm as drawn (the difference by using the drawn is small). Here we have averaged over all the 2 µm width MIM structures. This indicates that there is almost double the resistance for the seam region compared to the planar M2! This is important since most current carrying rule development uses planar lines. This can also be important for devices that are connected by vias such as MIM capacitors and inductors.

Using the same method, the NO_M1 structures were analyzed and a crack sheet resistance of 31 mOhms/sq was calculated. This is roughly 30% higher than the via structures and represents a potential worst case. To understand the relative differences in resistances, cross sectional analysis was performed in the via locations and the NO_M1 locations. From this, we observed that there was severe cracking in the NO_M1 structures (which is why the resistances were highest) as shown in Fig. 4. This is because the inter level dielectric planarizes differently on narrow structures (like the M1) – i.e. it thins - compared to large structures. This was also evident in cross-sections that looked at the via to via spacing. Based on this work, further scrutiny of some inductor test structures showed that this severe cracking could happen on certain inductor layouts. This led to a parameterized cell (p-cell) change to prevent this from occurring in a production circuit [2].

Following the same calculation we just did for the MIM, we can find the sheet resistance of M2 in parallel with M1 using the MIM and the VIA structures to determine the resistance of the metal inside the via region:

$$\rho_{m2m1} = \rho_{m2} - \frac{(R_{MIM} - R_{VIA}) \cdot W_{m2}}{2\text{NVIA} \cdot L_{Edge}} \quad (7)$$

This returns a value of 8.73 Ohms/sq (the expected value from ρ_{m2m1} and the M1 specification is 8.72 Ohm/sq). The values seem to be fairly reasonable and consistent.

As a final check of consistency, all of the data from the via structures, was fit using Eq. (3). Before fitting, the factors mentioned earlier were converted into forms that are compatible with the equation. M2 width was converted to squares using the corrected M2 length in the structure ($M_{2drawn} - dW$), the crack sheet resistance was converted using the number of edges (two times the number of vias), divided by the corrected width, multiplied by the length of the "edge", and the resistance within the via was

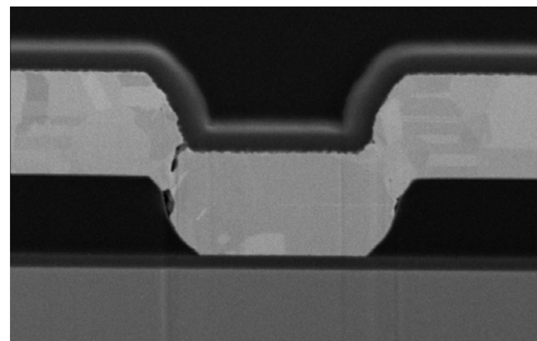

Fig. 4. Cross section of NO_M1 via structure showing crack formation that results in high resistance for the NO_M1 test structures.

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converted by multiplying the number of vias times the M2||M1 connection length in the via (where M2 stacked in parallel with M1), divided by the corrected M2 width.

These results were then fitted in JMP® to determine the different resistance components in Eq. (3). Fig. 5a shows the comparison between the measured data (*y*-coordinates) and the model generated data (*x*-coordinates). The value of Rsquare close to unity for the fit indicates the model accurately depicts the data. It estimates the proportion of variation in the response that can be attributed to the model rather than to random error. Rsquare adj is an adjusted version of Rsquare [3], Root Mean Square Error is the sigma, and Mean of the Response if the mean of the data. The number of points is represented by Observations. All of the points being near the 45° line indicate low residual error. Fig. 5b–d shows the leverage plots for the individual factors. The *x-axis* is a scaled version of the factor being compared. The further a point is from the center of the *x-axis*, the more leverage it exerts on the fit. The dashed lines (above and below) the solid line indicate the confidence curves. Since they pass through the horizontal dashed line, this indicates they are significant factors. The slopes of the lines are the estimates for the

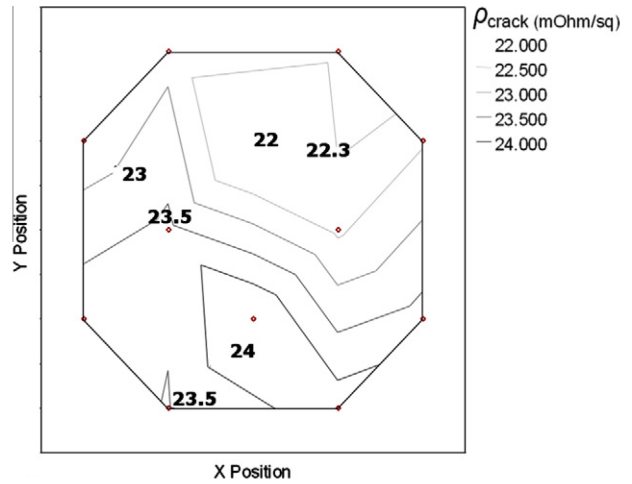

Fig. 6. Example of contour map for the crack sheet resistance, ρ_{crack} for an entire wafer using the three metal lines and a single via string of a via structure.

(a) Response Nom (4")

Whole Model

Actual by Predicted Plot

Nom (4") Actual

Nom (4") Predicted P<.0001

RSq=1.00 RMSE=0.0406

Summary of Fit

RSquare	0.998766
RSquare Adj	0.998236
Root Mean Square Error	0.040569
Mean of Response	4.648083
Observations (or Sum Wgts)	11

(b) Square 4"

Leverage Plot

Nom (4") Leverage Residuals

Square 4" Leverage, P<.0001

(c) Nedge/W2*LC 4"

Leverage Plot

Nom (4") Leverage Residuals

Nedge/W2*LC 4" Leverage, P<.0001

(d) NV*VL/W 4"

Leverage Plot

Nom (4") Leverage Residuals

NV*VL/W 4" Leverage, P<.0001

Fig. 5. Results of fitting to Eq. (3) and the leverage of the factors used for modeling. The most important factors were the M2 length and the crack sheet resistance. This was after correcting for the on-wafer M2 width.

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model parameters for each term. After geometry adjustment, M2 sheet resistance is 12.9 mOhm/sq (E-spec is 13.3 mOhm/sq), ρ_{m2m1} should be about 8.9 – now measured 5.6 mOhm/sq and ρ_{crack} is 23.89 mOhm/sq, a two times increase over the metal line itself. The model compares quite well with the simpler calculation above.

To demonstrate the advantage of these structures over relying on cross-sectional data, we applied the simple calculation method for extracting the crack resistance to another test wafer that included the MIM and metal line structures. The result is shown in Fig. 6 (the resistivity in this plot is in Ohms). The resistivity of the crack region does not vary much across the wafer but this shows that a simple set of structures (four lines in total) can be used to get statistical quantities of data for comparison of different processes.

3. Conclusion

We developed a set of electrical test structures to allow seam/crack formation in a non-planar process to be evaluated and characterized. This test structure set provides a way for gathering statistically relevant sets of data compared to simple cross sectional analysis. From the analysis shown here, as few as four lines (three metal lines of different width to determine dW and sheet resistance and one MIM style line) could be used to collect high volume data on seam formation in vias. It is also useful for process development to ensure that new processes do not exacerbate crack formation. Analysis by fitting the data with a model gave similar results as the simplified expressions. The exploration of these structures led to identification of a potential yield risk due to the layout on an inductor cell and this was corrected at the p-cell level.

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