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Tackling Multi-Bit Attenuator Designs

Designing an accurate digital step attenuator (DSA) with outstanding RF/microwave performance requires careful attention to detail and knowledge of semiconductor process variables.

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Digital step attenuators (DSAs) are versatile components that allow precise control of amplitude levels in a variety of RF/microwave systems. Of course, the requirements for different applications, from wireless and cellular communications equipment (portable and infrastructure) to wired cable-television (CATV) systems, can vary greatly. Designers of DSAs must remain aware of the different demands of the many potential applications while aiming for low insertion loss, high linearity, high attenuation accuracy, and fast switching speed.

Control of signal amplitudes is vital to the effective operation of many systems, where signals within the system can vary by orders of magnitude in power levels. Traditionally, voltage variable attenuators (VVAs) and variable gain amplifiers (VGAs) have been used for such level control. But in modern communications systems that rely on digital modulation formats, it is important to maintain the highest possible linearity. VVAs and VGAs can sacrifice performance in terms of linearity as a function of attenuation compared to a DSA. In addition, the return loss of VVAs can vary drastically with attenuation, complicating the VVA implementation into the system and adversely affecting system performance.

Commercial DSAs from Skyworks Solutions employ gallium arsenide (GaAs) RF pseudomorphic high electron mobility transistors (pHEMTs) coupled with silicon CMOs controllers for enhanced flexibility of system integration. By combining the advantages of gaas and silicon CMOs technologies, these attenuators offer outstanding performance at affordable prices with a maximum level of system integration flexibility. The DSAs incorporate two types of attenuation control: parallel interface and serial-to-parallel interface (SPI) control for addressing and power-up options.

The RF sections of these DSAs are comprised of gaas depletion-mode pHEMT field-effect transistors (FETs) and thin-film resistors (TFRs) arranged in cascaded “pi,” “T,” or “bridged-T” attenuator network configurations. Depletion-mode GaAs pHEMt circuits require negative DC bias voltage or external bias components such as RF chokes and/or DC blocking capacitors for proper operation, which can complicate their implementation in a given circuit. The silicon controllers designed for these 6- and 7-b attenuators incorporate negative-voltage generators (NVGs). These mitigate the issue and properly bias the gaas attenuator bits without a separate, external negative-voltage bias supply or the addition of any external bias components. Therefore, external RF chokes or DC blocking capacitors are not required for proper operation of these attenuators. This reduces the overall footprint, component count, and cost for the attenuation function on the RF system circuit board.

The pHEMT FEts operate much like switches that are either “on” or “off” in each attenuator bit, appropriately switching the various thin film resistors in a given bit into the main signal path or by-passing bits altogether. This method of FET operation ensures that the FET is biased discretely in either its ohmic or cutoff region. This results in higher attenuator linearity for all attenuation levels, as compared to VVAs or VGAs which continuously bias the transistor(s) between saturation and cutoff, significantly degrading linearity, depending on the attenuation or gain setting. Another advantage to operating pHEMT FETs in the ohmic or cutoff regions is reduced bias current draw or static bias power compared to VVAs and VGAs.

DSAs are usually specified in terms of the number of attenuation bits and the attenuation of the LSB. The bits are then typically binary weighted off of the LSB attenuation value in order to maintain a linear-in-dB step attenuation over all attenuation states. For example, model SKY12347-362LF is a 6-b DSA with least-significant bit (LSB) of 0.5 dB. For the SKY12347-362LF, bit number 1 has the LSB value of 0.5 dB while the DSA’s most-significant bit (MSB), bit

number 6, has an attenuation value of 16 dB. In between, bits 2, 3, 4, and 5 have attenuation values of 1, 2, 4, and 8 dB, respectively.

For example, in the bypass setting, the attenuation is 0 dB and when all bits are engaged, the attenuation is 0.5 + 1 + 2 + 4 +8 +16 dB or 31.5 dB, with values that can be selected in 0.5-dB increments between these two extremes.

Similarly, model SKY12343-364LF is a 7-b DSA with an LSB of 0.25 dB and an MSB of 16 dB resulting in an attenuation range of 0 to 31.75 dB in 0.25 dB steps.

These attenuators can switch between attenuation settings within 650 ns. Attenuation values are minimally affected by temperature, and the DSAs can be biased for +3.3 or +5.0 VDC operation. Linearity is maintained regardless of attenuation state and temperature within the specified bias voltage range. Numerous attenuators can be cascaded together and separately addressed when more than the maximum attenuation values of 31.50 or 31.75 dB are needed for a particular system application.

The multi-bit SKY12347-362LF and SKY12343-364LF DSAs are comprised of cascaded individual single bit attenuator networks. These single bit attenuator networks consist of pHEMT FET switched resistor circuits in “pi” or “T” topologies, as shown in **Fig. 1**. The design equations for the respective attenuator bit topologies are shown below. These DSAs are designed for operation in systems with a characteristic impedance, Z0, of 50 Ω with input and output impedances, also matched to 50 Ω: ZIN = ZOUT = 50 Ω. In these equations, the desired bit attenuation or loss is represented by L_{dB}.

For a “T” type attenuation bit device, the design equations for finding the appropriate resistor values for the circuit in the schematic diagram on the left-hand side of **Fig. 1** are:

$R_3 = 2\{[Z_{IN} \times Z_{OUT} \times 10^{(LdB/10)}]^{0.5}/(10^{(LdB/10)} - 1)\}$ (1)
$R_1 = Z_{IN}[(10^{(LdB/10)} + 1]/(10^{(LdB/10)} - 1)] - R_3$ (2)
$R_2 = Z_{OUT}[(10^{(LdB/10)} + 1]/(10^{(LdB/10)} - 1)] - R_3$ (3)
For the case where $Z_{IN} = Z_{OUT} = 50\ \Omega$, and substituting 50 Ω, the three equations above become: $R_3 = 100[(10^{(LdB/10)})^{0.5}/(10^{(LdB/10)} - 1)]$ (4)
$R_1 = 50[(10^{(LdB/10)} + 1]/(10^{(LdB/10)} - 1)] - R_3$ (5)
$R_2 = 50[(10^{(LdB/10)} + 1]/(10^{(LdB/10)} - 1)] - R_3$ (6)

For a “pi” type attenuation bit device, the design equations for finding the appropriate resistor values for the circuit in the schematic diagram on the right-hand side of **Fig. 1** are:

$R_3 = 0.5(10^{(LdB/10)} - 1)[(Z_{IN} \times Z_{OUT})/(10^{(LdB/10)}]^{0.5}$ (7)
$R_1 = 1/\{[(10^{(LdB/10)}) + 1]/[Z_{IN}(10^{(LdB/10)}) - 1] - (1/R_3)\}$ (8)
$R_2 = 1/\{[(10^{(LdB/10)}) + 1]/[Z_{OUT}(10^{(LdB/10)}) - 1] - (1/R_3)\}$ (9)

For the case where ZIN = ZOUT = 50 Ω, and substituting 50 Ω, the three “pi” bit attenuation equations become:
$R_3 = 25[(10^{(LdB/10} - 1)/(10^{(LdB/10)})^{0.5}]$ (10)
$R_1 = 1/\{[(10^{(LdB/10)}) + 1]/[50(10^{(LdB/10)}) - 1] - (1/R_3)\}$ (11)
$R_2 = 1/\{[(10^{(LdB/10)}) + 1]/[50(10^{(LdB/10} - 1] - (1/R_3)\}$ (12)

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Typically, the selection of the bit topology for a given attenuation is based on the resulting resistor values using the design equations shown above. This decision is made on the corresponding geometry or physical size of a given resistor that can be realized in the manufacturing process coupled with die size and layout restrictions, linearity requirements, and the parasitic characteristics of the respective bit structures. Attenuator bits with lower values of attenuation (below 16 dB) are usually in the “T” topology, where higher attenuation values are typically realized with the “pi” structure. **Table 1 and Table 2** show ideal resistor values using the “T” and “pi” attenuator bits, respectively, for various values of attenuation, assuming that $Z_{IN} = Z_{OUT} = 50\ \Omega$.

When using computer-aided-engineering (CAE) simulation software and precise device models, a device designer must still scale the resistor values shown in the tables to include the effects of pHEMT FET “on resistance” (R_{ON}) and “off capacitance" (C_{OFF}) along with die and packaging RF parasitic characteristics that invariably affect attenuation

accuracy over the band of interest. An RF designer must meticulously simulate and lay out attenuator die using both lumped-element circuit simulators and electromagnetic (EM) simulation tools to mitigate potential RF coupling issues and parasitic elements that can impact performance.

Tuning components in parallel or series with the attenuator resistors are sometimes used to maintain flat attenuation response over the specified bandwidth for parasitic element compensation. All attenuator states, 64 states for the SKY12347- 362LF (0 to 31.5 dB attenuation) and 128 states for the SKY12343- 364LF (0 to 31.75 dB attenuation), must be simulated to ensure monotonic response between adjacent states over the specified bandwidth. All of this would not be possible without novel design automation features implemented into the CAE software design simulation tools.

One of the major issues an RF designer often encounters during the design process is that the attenuation for the higher-order states is reduced as a function of increasing frequency. That is, the $|S_{21}|$ attenuation response "rolls up" towards 0 dB with increasing frequency. This can be attributed to the COFF of the bypass FETs, RF coupling between bits on the GaAs die, and to parasitic effects in the shunt portions of the attenuation bits. A designer must pay close attention to this attenuation response "roll up" effect for all states to ensure that the attenuation response versus frequency for a given attenuation state remains within a design specification and avoids becoming nonmonotonic with respect to control signal values. For most applications, it is critical that DSAs maintain monotonic attenuation with respect to the specified frequency range for all attenuation states. The 6- and 7-b attenuators developed by Skyworks implement a novel GaAs fabrication process feature in the shunt portion of the attenuation bits to minimize parasitic inductances of the die and packaging.

The insertion loss of the attenuator with all bits in the bypass mode is another critical parameter that a DSA designer must consider during the design process. Where the frequency response of the attenuation for all states is referenced with respect to the insertion loss, the DSA designer must ensure that the inevitable insertion loss increase with respect to frequency is minimized and that the parasitic elements of the die are managed to ensure a smooth insertion loss rolloff with respect to frequency. Any degradation in the return loss due to parasitic elements will have adverse effects on the insertion loss and corresponding attenuation accuracy and frequency response.

The insertion loss in dB (ILdB) for a series and shunt network is given by the following equation:

$$IL_{dB} = 10\log_{10}\{[1 + (R_S/2Z_0)]2 + [(Z_0 + R_S)/2X_C]^2\} \quad (13)$$

where:

R_S = the "on" drain-source resistance of the series FET biased "on" in the ohmic region and
X_C = the "off" drain-source reactance of the shunt FET biased "on" in the ohmic region. The "off" reactance can be found by the following equation:

$$X_C = 1/(2\pi f C_{OFF})$$

These equations show that smaller "on" resistance and "off" capacitance parameters result in improved insertion loss. Insertion loss will increase with frequency as the "off" reactance of the pHEMT FETs in the shunt portions of the attenuator decrease. On the surface, it appears that a larger gate periphery (W) FET in the bypass position will yield better insertion-loss performance. This is true to a point. A DSA designer must realize that larger devices will also have larger features that can potentially allow signals to couple to adjacent portions of the RF circuit, even through the GaAs substrate to ground, adversely affecting circuit performance.

Because of the increasing use of digital modulation schemes in modern communications systems, DSA designers must pay particular attenuation to linearity performance, including the second-order intercept point (IP2) and third-order intercept point (IP3). Linearity must be simulated and verified over the specified band prior to DSA tape out in order to confirm specification compliance in addition to the frequency response characteristics discussed above. The CAE design tools for the Skyworks pHEMT GaAs process includes appropriate circuit modules for simulating and verifying linearity. If necessary, an RF DSA designer can make the appropriate design modifications to ensure linearity and then verify the results of the frequency response simulation.

The second and third order intercept points for a series PHEMT FET in the "on" or ohmic region are expressed as follows[2]:

$IP2 = (Z_0\alpha^4_1)/(2\alpha^2_2)[1 + 2\alpha_1 Z_0]^2$ (14)
$IP3 = (Z_0\alpha^3_1)/(2\alpha^3)[1 + 2\alpha_1 Z_0]$ (15)

where:

α_1 = the inverse of the channel series resistance, R_C:

$\alpha_1 = 2(ID_{Sat}/V_p) = 1/R_C$ (16)
$\alpha_2 = 2(ID_{Sat}/V_p) \times \{(\mu_1/2\mu_{LF}) - [(0.5 + \gamma)/Vp]\}$ (17)
$\alpha_3 = 2(ID_{Sat}/V_p) \times [(\mu 2/3\mu_{LF}) - \mu_1(\gamma/2 + 1/3)/\mu_{LF}V_p]$ (18)
$\gamma = -v_{GS}/v_{DS}$ (19)

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where:

μN = the mobility expansion coefficient.

The gate-to-source voltage and drain-to-source voltage relationship from the HEMT AC equivalent-circuit shown in ref. [2] is represented by γ.

From these equations, it is evident that linearity improves with increasing drain saturation current, I_{DSat}. This is due to the lower FET channel "on" resistance, R_C. These parameters improve by reducing the gate length (L) and increasing the gate width (W). The gate length (L) is usually fixed for a given manufacturing process. Therefore, a DSA designer must scale the FET gate width (W) or periphery accordingly to a desired frequency response and linearity, requiring an attentive DSA designer to analyze the interaction between linearity and small-signal response as FET sizes are scaled during the design process.

For a FET in the off state, the intercept points are related by the coefficients of the voltage-dependent FET capacitance. These coefficients are expressed with units of Farads per Volt (F/V) for C_{GS1} and Farads per Volt squared (F/V^2) for C_{GS2}:

$C_{GS1} = eW/[2(V_{bi} - V_{io}) \times V_p/[(V_{bi} - V_p - V_{io})]^{0.5}$ (in F/V) (20)
$C_{GS2} = (CGS1/2) \times [(1/2(V_{bi} - V_p - V_{io}) + 1/(V_{bi} - V_{io})]$ (in F/V^2 (21)

where:

e = the permittivity of GaAs;
W = the pHEMT FET gate width;
V_p = the pHEMT FET pinchoff voltage;
V_{bi} = the metal gate semiconductor junction potential (or built-in voltage); and
V_{io} = the reverse bias voltage on the gate electrode.[3]

These equations show that the harmonic current can be reduced by increasing the gate reverse bias voltage for a given FET.

Electrostatic discharge (ESD) is yet another concern for an RF DSA designer. While GaAs pHEMT FETs are known for excellent RF performance, they tend to suffer poor ESD tolerance. Special attention must be paid to any parts of the attenuator circuit electrically exposed to the outside world during handling and assembly. Because the Skyworks DSAs incorporate silicon CMOS controllers with NVGs, no ESD susceptible parts of the attenuators are exposed to the outside world. In addition, the GaAs fabrication process used to mitigate the parasitic elements in the shunt portions of the circuit actually helps improve the ESD tolerance of these attenuators. The only portions of the GaAs chip exposed to the outside world are the attenuator input/output pins. When unbiased (i.e., during handling and at end-user assembly), these pins are connected to the attenuator ground/common node via a low-resistance path through the shunt portions of the circuit, enhancing the ESD tolerance of the overall part.

The aforementioned points merely touch upon a few of the major concerns and issues faced during the design process for DSAs. As an RF designer, one quickly realizes that features of a circuit that are ideal for one parameter in the specifications are often at odds with another specification. For example, a design attribute of a circuit that is good for third order intercept may or may not be good for attenuation accuracy. An attribute beneficial for the low band operational characteristics may degrade performance at the high band. An RF circuit characteristic designed to enhance ESD tolerance may or may not, as in this case, adversely affect insertion loss and/or linearity, and so forth. The responsibilities of the RF designer include possessing comprehensive knowledge of the manufacturing process capability, understanding the design tradeoffs and then managing the RF circuit topology, layout and inevitable parasitic elements to ensure a specification- compliant part within the process variation window over the specified operational conditions of the device.

Similar to the meticulous simulation through the use of automated design tools, the DSAs are thoroughly characterized by means of automated test systems, evaluating performance of all states of the 6-b SKY12347-362LF (64 states) and the 7-b SKY12343-364LF (128 states) over the specified bias and temperature conditions. The data presented in **Fig. 2**, **Fig. 3**, **Fig. 4**, **Fig.5**, **Fig. 6**, and **Fig. 7** represent data sets compiled and averaged together for all attenuator devices in the respective characterization lots. Such information allows everyone from the design engineer to the process engineering team to analyze the statistical data for specification compliance verification within the process window and provide beneficial inputs to the fabrication engineering and device modeling teams.

As noted in the previous section, ensuring consistent insertion-loss rolloff with respect to frequency is one critical parameter that must be addressed in order to maintain the corresponding attenuation accuracy specifications. **Figure 2** shows the insertion loss of the SKY12343-364- LF with respect to frequency. Inspection of the graph shows that the DSA design meets the consistent insertion loss rolloff criteria with no significant abrupt discontinuities in the insertion loss curves.

Additionally, the insertion-loss variation with respect to temperature is minimal as compared to that of other technologies with about 0.18 dB variation for operating temperatures from -40 to +85°C at 4 GHz.

Figure 3 and **Figure 4** show input/output port return-loss measurements with respect to frequency for all major states of the SKY12343-364LF. The return loss increase above about 1 GHz for all states is due to the unavoidable parasitic elements of the circuit. Managing these parasitic elements during the design process is a key to maintaining specification compliant insertion loss, return loss, and attenuation accuracy parameters.

Figure 5 shows bit errors for the major bits of the SKY12343-364LF. The attention to detail in the design process can be seen in the high accuracy reflected in these plots. Even the 31.75 dB setting, which typically produces the worst case error for a DSA, is well within ±0.5 dB of error or ±1.6%.

Figure 6 shows actual versus desired attenuation at 900, 1800, 2200, and 3800 MHz. Ideally, this would be a straight line with a slope of 1. Any “bumps” or change in slope would be the result of attenuation errors or accuracy issues. Even at 3800 MHz, only minor “ripple” is evident, showing attenuation error slightly increasing with frequency. **Figure 7** shows the input third-order intercept point (IIP3) tested with two RF signals (tones) at +18 dBm per tone and 20 MHz spacing, from 500 to 3000 MHz. With the GaAs attenuator biased at +5 VDC, this plot shows IIP3 from +48 to +60 dBm for the major attenuation states over the specified frequency range. Increased demand for better-performing RF communications systems is challenging RF IC designers to develop effective component solutions. These versatile DSAs with integrated CMOS controllers are providing practical solutions for amplitude control in a wide range of communications systems.

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