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Match The Ports Of Differential Devices

This straightforward approach shows how to match the impedances of high-frequency, differential devices both with discrete components and microstrip circuit elements.

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Differential or balanced devices are widely used in communications systems for their high immunity to noise. However, they can be difficult to integrate since the widely used S-parameter matching method cannot simply be applied. Fortunately, a generic method derived from the mixed-mode S-parameter concept can be used to match differential devices. It is simple and effective, as will be borne out by verification via four-port vector network analyzer (VNA) and analysis with electronic-design- automation (EDA) software.

Impedance matching is the practice of tuning a load impedance (Z) to the optimum impedance (Z_{opt}-) of a connected device. It requires three main steps:

1. Finding Z_{opt}- (the process is not detailed here but is usually achieved by tuning the load impedance of the circuit until the performance, i.e., the output power for a transmitter or the noise figure for a receiver, is met;
2. Measuring the Z that must be matched (this is done in the same way that the optimum impedance is measured); and
3. Determining the matching circuit that tunes Z to Z_{opt}. To perform impedance matching on an example twoport network (***Fig. 1***), a VNA was used to measure the RF impedance at the network's ports, resulting in the singlemode S-parameter (S_{sm}) matrix of Eq. 1. The variables a1 and a2 represent incident waves while b_1 and b_2 represent reflected waves.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = S_{sm} \times \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \qquad (1)$$

where

$$S_{sm} = \begin{pmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{pmatrix} \qquad (A)$$

Equation 2 details the relationship between the S-parameters and impedance:

$$Z_i = Z_0 \times \frac{(1+s_{ii})}{(1-s_{ii})} (i \in [1,2]) \quad (2)$$

while Eq. 3 calculates the voltages and currents at the two nodes:

$$\begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} v_1^+ + v_1^- \\ v_2^+ + v_2^- \end{pmatrix} = \begin{pmatrix} Z_1 \times i_1 \\ Z_2 \times i_2 \end{pmatrix} = \begin{pmatrix} Z_1 \times (i_1^+ - i_1^-) \\ Z_2 \times (i_2^+ - i_2^-) \end{pmatrix} \quad (3)$$

where v_i+ and i_i+ represent the forward voltage and current, respectively, and v_i– and i_i– represent the reverse voltage and current, respectively.

For differential circuits, S-parameter theory has been extended to introduce the concept of mixed modes.[1,2] Therefore, ***Fig. 1*** could represent either a two-port single-ended circuit or a single-port mixed-mode circuit. The model has two modes of propagation: common mode and differential mode, which are also referred to as even and odd mode when considering each port separately. For both modes, incident waves a_c, a_d, and reflected waves b_c, b_d, a_s well as voltages and currents v_c, v_d, i_c, and i_d are defined using Equations 4 through 10.

$$\text{If:} \quad M = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & -1 \\ 1 & 1 \end{pmatrix} \quad (6)$$

then, as shown in Eq. 7, and

$$v_c = \frac{1}{2}(v_1 + v_2) \text{ and } \quad i_c = (i_1 + i_2) \quad (8)$$

$$v_d = (v_1 - v_2) \text{ and } \quad i_d = \frac{1}{2}(i_1 - i_2) \quad (9)$$

$$\begin{pmatrix} v_d \\ v_c \end{pmatrix} = \begin{pmatrix} Z_d \times i_d \\ Z_c \times i_c \end{pmatrix} \quad (10)$$

For the mixed-mode analysis, when referencing the signal to ground, the even and odd impedances (Z_e and Z_o) of each port are also defined. If the device structure is symmetrical, $Z_e = 2Z_c$ and $Z_o = Z_d /2$. Mixed mode S-parameters are defined by:

$$\begin{pmatrix} b_d \\ b_c \end{pmatrix} = S_{mm} \times \begin{pmatrix} a_d \\ a_c \end{pmatrix} \qquad (11)$$

where S_{mm} is

$$S_{mm} = \begin{pmatrix} s_{dd} & s_{cd} \\ s_{dc} & s_{cc} \end{pmatrix} \qquad (12)$$

and S_{dd} refers to the differential mode S-parameter needed to determine the differential impedance; S_{cc} is the common- mode parameter; and S_{dc}, S_{cd} are cross-mode parameters.

Each of the cross-mode parameters represent the amount of transfer from common to differential mode, and vice versa, that propagates through the circuit. For an ideal balanced circuit, mixed terms S_{dc} and S_{cd} are zero.

As part of achieving impedance matching, a goal is to determine the differential-mode circuit impedance Z_d. For this purpose, only the differential mode propagation must be evaluated (the common-mode propagation can be omitted). There is no RF common source (a_c = 0) even if the DC supply can be present on each side of the balanced port.

Bockelman et al.[2] demonstrates that mixed-mode parameters can be derived from-single mode parameters:

$$(S_{mm}) = M \times S_{sm} \times M^{-1} \qquad (13)$$

Therefore, Smm can be redefined as:

(See Equation 14)

Assuming the circuit shown in ***Fig. 1*** is perfectly balanced, parameters S_{ll} and S_{22} are equal as are S_{l2} and S_{2l}-. Therefore, from Eq. 14, S_{dc} and S_{cd} are zero. Using Eq. 2, the differential impedance can be expressed as:

$$Z_d = Z_{0d} \times \frac{(1 + s_{dd})}{(1 - s_{dd})} \qquad (15)$$

where $Z0_d$ is the differential reference impedance and is defined by

$$Z_{0d} = 2 \times Z_0 \qquad (16)$$

From Eqs. 14 and 16, Z_d can be defined as Eq. 17.

The SKY65336-11 front-end module (FEM) from Skyworks Solutions served as an example of a device that might be matched in a differential arrangement. The normalized (50-Ohm reference) 2450- MHz single-mode S-parameters of the differential transmit input were measured and plugged into Eq. 1 to yield Eq. B.

Solving Eq. 12 for Sdd where the differential reference impedance, Z0d, is 100 Ohms yields S_{dd} = -0.361 + j0.374. Solving Eq. 17 for Z_d yields Z_d = 36.6 + j37.5 Ohms.

The differential-mode S-parameter, S_{dd}, was also simulated using the Advanced Design System (ADS) suite of simulation software programs from Agilent Technologies. Results were plotted on a Smith Chart (***Fig. 2***). The single-mode, Sparameters derived from the software simulation agreed with measurements using a four-port VNA.

The process of impedance matching involves tuning a device's port impedance to a required impedance. The use of discrete inductors and capacitors is an easy way to achieve impedance matching. If area is not a constraint, using transmission lines and stub tuner elements is a cost-competitive alternate solution. This method provides a lower loss but is not as flexible as using discrete elements since new matching means a new printed-circuit-board (PCB) design.

Using a shunt element, a balanced circuit keeps its symmetry because the element is placed between two ports. When a series component is introduced, the circuit is no longer symmetrical. When lumped elements L and C are added to the balanced load, Z (S and S-- are equal), $S_{l'l'}$ and $S_{2'2'}$ of the matched load, Zopt, are now different (***Fig. 3***). Based on Eqs. 12 and 14, mixed terms S_{dc} and S_{cdopt}, of circuit A in ***Fig. 4***, which is given by:

(See Equation 18)

where XC and XL represent the impedance (purely imaginary) of the ideal capacitor and inductor, respectively.

Equation 18 can be rewritten as:

$$Z_{opt} = \frac{1}{j2C\omega} + \frac{1}{j2C\omega} + (jL\omega \,||\, Z)(C)$$

This equation provides the impedance of circuit B in ***Fig. 4*** and, therefore, demonstrates that circuits A and B are equivalent. However, only circuit B maintains the symmetry ($S_{l'l'}$ = $S_{2'2-'}$).

The impedance of the circuit C in ***Fig. 4*** can be calculated by:

$$Z_{opt} = X_L + (X_C \,||\, Z) = jL\omega + (\frac{1}{jC\omega} \,||\, Z) \text{ (D)}$$

which can be rewritten as:

$$Z_{opt} = \frac{jL\omega}{2} + \frac{jL\omega}{2} + (\frac{1}{jC\omega} \,||\, Z) \text{ (E)}$$

In this case, circuit D in ***Fig. 4*** is equivalent to circuit C in ***Fig. 4***. When working w

ith transmission-line impedance matching, the simple transformation of the series element described above will not work. However, there is another simple technique available.

As shown in ***Fig. 5*** (where Zi and Li denote the transmission line impedance and length, respectively), the balanced differential circuit is divided into two identical half single-ended structures. The dividing line is at the ground potential because of the circuit symmetry. The result is that the series elements of both single-ended and differential circuits are identical, although the shunt element is cut in half (including the loads, Z and Z_{opt}).

Rather than matching Z to Z_{opt}, the new exercise becomes matching the half circuits, or matching Z/2 to $Z_{opt}/2$. Eventually, a fully differential matched circuit is derived by bringing half structures back together. Note that this technique can be also used with lumped elements (***Fig. 5)***.

For example, a differential Z circuit and a single-ended Z/2 circuit are shown in ***Fig. 6*** (with Z = 38 + j × 37 Ohms and Z/2 =19 + j × 18.5 Ohms). Parameter E in the transmission- line model refers to the electric length or phase shift (in deg.), or E = 360(L/λ).

The simulation results shown in ***Fig. 7*** demonstrate that the single-ended circuit is matched to $Z_{opt}/2$ and, using the transformation described above, the differential is actually matched to Zopt. The Smith Chart reference impedance of the single-ended circuit is 50 Ohms, with an impedance of 100 Ohms for the differential circuit.

Differential impedance matching can be shown by an example: matching the SKY65336-11 ZigBee FEM to the model EM250 transceiver from Ember. The transmit and receive differential-port S-parameters for the SKY65336-11 and the SKY65337-11 FEMs were measured; their corresponding differential impedances are listed in the table. Various ZigBee-compliant transceivers are available with different RF port impedances. They also specify Z_{opt}, which represents the impedance that the transceiver should see for best performance. Ember[4] suggests an optimum reflection coefficient of 0.79/65 deg.

(expressed in magnitude and phase) for maximum transmit power and best sensitivity. The reference impedance is 50 Ohms. This corresponds to a load impedance (Z_{opt}) of 19.5 + j75 Ohms or 308 Ohms in parallel with an inductance of 5.2 nH.

The SKY65336-11's transmit impedance of Z = 38 + j37 is matched to the Ember transceiver's Z_{opt} = 19.5 + j75 Ohms, with both impedances represented on a Smith Chart (***Fig. 8***). The two traces (shown with arrows) show the course of impedance Z by adding a shunt inductor (6.8 nH) and a series inductor (2.8 nH). The differential structure of ***Fig. 9*** results from applying the impedance transformation approach.

Even the most compact, practical board design includes transmission lines to connect the different components.4 Traces from the source and load devices to the lumped matching elements contribute to impedance matching and must be taken into account especially at high frequencies. For a differential circuit, the two traces must be identical to maintain symmetry, which means the same length, width, and distance to ground. For such differential transmission lines, coupled microstrip lines are often used. The characteristic impedance of the differential mode in these transmission lines can be analyzed using the mixed-mode concept. Assuming the structure is symmetric, the differential, and that the coupling between the two lines is negligible, the differential and common modes propagate uncoupled, and the characteristic impedance of the differential mode is given in ref. 5: $Z_{0d\_microstrip} = 2_{Z0\_microstrip}$, where $Z_{0\_microstrip}$ is the characteristic impedance of the single microstrip line.

The transmission impedance needed to connect the different devices still must be determined. Usually, a 50-Ohm trace impedance is used as a standard to interconnect single- ended devices. For differential devices, several standard impedances (e.g., 50, 75, and 100 Ohms) are widely used. PCB stack-up constraints include minimum reliable trace width and PCB cost; both contribute to the final design.

Assume a PCB stack up with H = 8 mil, dielectric relative permittivity (er) of 4.3, conductance of $59.6e^{+6}$ S/m, and thickness (t) of 1.4 mil, and loss tangent of 0.02. A 75-Ohm reference impedance transmission line design has narrower traces compared to a 50-Ohm line. That allows such a design to be spaced out more to minimize the coupling, which is always difficult to estimate. The matching circuit shown in ***Fig. 10*** is composed of two identical 75-Ohm transmission lines, TL1 and TL2, and one shunt inductor, L1, that tune the load impedance Z/2 to $Z_{opt}/2$. Since a 75-Ohm trace impedance is used for matching in this example, the Smith Chart reference impedance should also be 75 Ohms so that when a transmission line is added to the load, Z, the impedance navigates on a constant VSWR circle (***Fig. 11***).

To create a microstrip line with an impedance of 75 Ohms and an electrical length of 10 deg., Eqs. 19 and 20 are used to compute the width (W = 6 mils) and the length (L = 80 mils) of the microstrip line:

(See Equation 19)

$$L = \frac{E}{T \times f_0 \times 360} \qquad (20)$$

where H is the dielectric thickness (8 mils), er is the dielectric relative permittivity, t is the conductor thickness, f0 is the frequency (2.45 GHz), E is the electrical length (10 deg.), and T is the propagation delay. The actual single-ended structure is shown in ***Fig. 12 (web only, www.mwrf.com)***. Assuming there is no coupling between the two single-ended transmission lines, the differential structure as described in the previous section is derived by combining the two singleended structures as shown in ***Fig. 13 (web only, www.mwrf.com)***.

The results were compared on a Smith Chart (***Fig. 14, web only***), which confirms that the differential matched load – S(5,5) on the plot – is Zopt (19.5 + j75). This point on the chart is slightly different because of the approximation of the transmission line (negligible coupling between the two microstrip lines). However, because the matched load close, the approximation has no effect on performance.

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