Single Die Broadband CMOS Power Amplifier and Tracker with 37% Overall Efficiency for TDD/FDD LTE Applications

Florinel Balteanu,
Skyworks Solutions, Inc., Irvine, CA 92617, USA

Abstract—This paper presents a 2.3GHz - 2.7GHz broadband CMOS FDD/TDD LTE Band 7, 38, 40 and 41 power amplifier (PA) fully integrated with a fast envelope tracker (ET) on a single 0.18µm CMOS die. The PA and the tracker achieve a 37% overall efficiency for 26.5dBm and -39dBc ACLR. The entire design including the input/output match uses an active silicon area around 2.7mm².

Index Terms—CMOS, GaAs, LTE, power amplifier, envelope tracking (ET).

I. INTRODUCTION

Modern high data rate communication cellular systems such as Long-Term Evolution (LTE) use complex digitally modulated signals, such as 16/64QAM, to increase data rates. These spectrally efficient modulation schemes with a high peak-to-average power ration (PAPR) place stringent linearity demands on the RF power amplifiers (PAs) to achieve high efficiency and high linearity for a wide power range, as presented in Fig.1.

Fig.1. Peak-to-average power ratio

TDD LTE systems with asymmetrical uplink/downlink ratio (such as 1/3) stress more the uplink chain. In this scenario for TDD-LTE the bandwidth requirements to have the same uplink data stream throughput is at least 4 times higher. Therefore 40MHz TDD-LTE is required to reach the same peak bandwidth as for 10MHz FDD-LTE, as presented in Fig.2. The cost and size for smart phones are very important for consumer products. CMOS technology does follow Moore’s law for intensive digital products and has made inroads for CMOS PAs. There are still challenges for CMOS PAs and unfortunately the size of matching networks doesn’t reduce with CMOS technology scaling as stated by Moore’s law.

II. CMOS POWER AMPLIFIER AND TRACKER

Using CMOS for PAs has several challenges due to the lower transistor breakdown voltage and reduced intrinsic linearity for CMOS transistors compared with GaAs. To overcome this, CMOS PAs for LTE use envelope tracking (ET) to increase linearity and efficiency. ET used with CMOS PAs increase the adjacent channel leakage-power ratio (ACLR) and error vector magnitude (EVM) to higher degree than for a GaAs PA. This paper presents a single die broadband CMOS PA and tracker integrated on the same die manufactured in high resistivity CMOS 0.18µm CMOS technology with trough wafer vias (TSVs).

Fig.2. FDD/TDD LTE uplink/downlink schedule

Using CMOS for PAs has several challenges due to the lower transistor breakdown voltage and reduced intrinsic linearity for CMOS transistors compared with GaAs. To overcome this, CMOS PAs for LTE use envelope tracking (ET) to increase linearity and efficiency. ET used with CMOS PAs increase the adjacent channel leakage-power ratio (ACLR) and error vector magnitude (EVM) to higher degree than for a GaAs PA. This paper presents a single die broadband CMOS PA and tracker integrated on the same die manufactured in high resistivity CMOS 0.18µm CMOS technology with trough wafer vias (TSVs).

For GaAs HBT technologies a semi-insulating substrate is used so devices fabricated will have reduced parasitic capacitances and higher Ft devices. Also GaAs technologies usually feature backside TSVs that connect the front side metallization of the die to the back side ground plane. These features provide a low impedance path to the common ground plane and a good thermal conductor. In order to deal with these limitations the CMOS PA designs have tried to use flip-chip techniques and use laminate substrate for output matching networks. Still losses and size for CMOS and CMOS_SOI PAs using flip-chip are higher than GaAs PAs. For this reasons this design uses High Resistivity CMOS substrate (3kohm). The most difficult issue with CMOS technology scaling is the need to overcome the overvoltage stress. Using stacked cascode transistors has the benefit of improving the reliability of CMOS PAs. Fig.3. shows the block diagram of the implemented CMOS PA with the tracker integrated on the same die.
The PA has been designed with two stages both using 1.8V/3.3V cascode structures. The use of low feature size 1.8V transistors for RF drive (M1) does help to increase the RF gain and PA efficiency. The top transistors (M2) are thick gate 3.3V CMOS which handle the high voltage stress. Also all the power transistors sit in separate deep n-well to increase linearity through extending the breakdown CMOS region [1]. The wells are connected through high value resistors to the highest potential. This technique together with symmetrical layout and use of TSVs helps with stress power handling as well with balancing the power through the power cells. For the same output power the CMOS power cell size itself is quite small compared with a GaAs or SiGe BJT power cell. For this reason, dense TSVs are better suited for power balance compared with cheaper flip-chip solution. Also compared with a flip-chip design this design allows the use of bond-wire inductors for High Q matching circuitry. In order to provide broadband characteristic the PA is using a CMOS class-E structure with additional third harmonic 3fo trap [2], [3]. Then to improve the power added efficiency PAE and linearity a fast envelope tracker has been integrated on the same die with the PA. The fast tracker works together with a buck DC_DC buck converter, providing approx. 20% of the power required by the PA. For an output power of 26.5dBm the buck DC voltage Vdc-dc is set at 2.7V and provides the 80% of the PA power with more than 94% efficiency. This DC low voltage provides protection for CMOS devices but it does require the PA to operate at low load line. Unlike in GaAs technology, increasing the load line to get better efficiency through lower losses in the output match is not desired in CMOS due to higher $fCV^2$ losses and breakdown limitation. Integrating the fast tracker with the PA core on the same die and the AC coupled hybrid architecture does help with the TDD LTE operation compared with a standalone ET controller. The envelope signal is used to dynamical bias the top cascode transistor and keeps the main RF transistor in the approximate constant $gm$ region.

III. MEASUREMENTS

The CMOS die (1.6mm x 1.7mm) has been packaged in a 3mm x 3mm 16L-QFN package. Tested under 10MHz, 50RB LTE signal the overall system efficiency observed was 37% at 26.5dBm for -39dBc ACLR1 and -50dBc ACLR2, as presented in Fig. 4. The gain measured was 22dB, lower than 29dB simulated due to different substrate modelling for high resistivity substrate. The envelope signal was provided through an ET signal generator aligned with the RF signal and the ET shaping table was optimized to get the best ACLR. There was no digital signal processing DSP applied to compensate for residual AM-PM and improve further the linearity.

IV. CONCLUSIONS

A fully integrated 0.18µm 2.3GHz-2.7GHz broadband CMOS PA and Tracker was presented and its performance characterized. The author thanks Andrei Grebennikov for his valuable help at RFaxis, where this work was performed.

REFERENCES