Modeling of SOI FET for RF Switch Applications

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***Abstract* — This paper presents the modeling of an SOI FET for RF switch applications. Given that the HF small-signal predictability, i.e. the insertion loss and the isolation, is a common state of the art, the study focuses on the modeling of the non-linearity of the FET. The non-linearity of an SOI FET switch arises from not just the transistor, but also the SOI substrate through various mechanisms. First the non-linearity is caused by the voltage imbalance, a direct result of the substrate loss, in a switch made of many FETs stacked in series. The voltage imbalance is the main non-linearity contributor to a FET switch at high-power levels. Secondly the substrate itself is non-linear and sets the harmonic floor. Besides the substrate, the impact of other important SOI physics, such as the floating-body effect and the parasitic BJT effect, to the switch linearity will also be discussed. Finally a hybrid model that combines PSP as the FET core and a layout-dependent non-linear SOI substrate model is presented, and excellent non-linearity predictability was demonstrated on a real-life RF switch.**

***Index Terms* — RF switch modeling, PSP model, SOI model, floating-body effect, parasitic BJT effect**

I. INTRODUCTION

A typical front-end module (FEM), which is frequently employed in a cellular handset as the interface between the external world and the internal RF transceiver and baseband ICs, consists of tens to hundreds of Si, non-Si, and discrete components, including pHEMT switches, GaAs/InGaP PAs, and Si controllers as well as other matching passives. In addition to the demand of smaller footprint, the fast pace of commoditization of the cellular application has driven development of FEMs to use a MOSFET switch to replace the pHEMT switch for its low cost as well as its natural capability to have the controller integrated on the same die. It has been known that, because of its limited high-voltage (HV) isolation from the substrate, the MOSFET would have inferior performance in terms of high-power handling capability, insertion loss, and linearity compared to the pHEMT counterpart. Although the SOIFET was initially developed for high-speed and low-power digital applications [1], it is a natural candidate -- as opposed to the bulk MOSFET -- for high-power switch applications and a few research papers have been published in the past few years, demonstrating its feasibility [2][3].

While Si-based technology is famed for low cost in volume production, it tends to have higher non-recurring engineering (NRE) costs and longer development times. To mitigate the disadvantage, an accurate model and simulation methodology is required to reduce the number of mask spins to achieve comparable NRE and time-to-market. Also, since a design with higher integration is always more difficult to debug at the hardware level, a predictive model would be a powerful and cost-effective diagnostic tool.

This paper discusses various effects in an SOIFET and their impact to an RF switch application. As the linearity of a switch is very stringent in cellular applications, even very weak non-linear effects in the device need to be accounted for. A typical GSM application requires the switch 2nd and 3rd harmonics to be below -40dBm level at 34dBm input power and below -33dBm under 3:1 VSWR conditions.

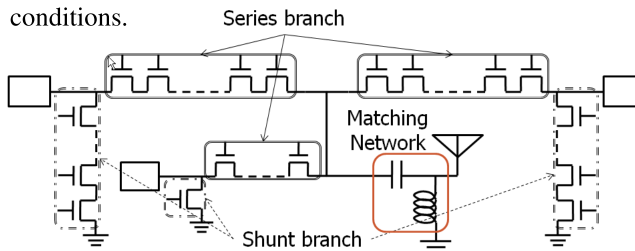

Fig. 1 A simplified switch schematic

The paper is organized as follows. In section II, modeling of a switch will be presented with a focus on the physics that influence the linearity of an RF switch. Section III describes the model implementation for a switch application. Section IV presents the measured data of the switch test structures. Section V concludes the paper with a summary.

II. MODELING OF A SWITCH

In our experience, the small-signal behavior of a switch is not difficult to model, no matter if it is in ON or OFF mode. Most foundry-provided models predict the ON insertion loss right out of the box, even if the model is based on a simple modeling methodology with only DC and large-area AC capacitance measurement. The reverse isolation of such a simple model might be a little bit off. It is because most of modeling methodology is based on measurements taken on transistors in the common-source (CS) configuration, where the OFF capacitance (C_{OFF}) is not a prominent component. The problem can be easily resolved with s-parameter measurements on a few

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common-gate (CG) structures with high and low gate resistance.

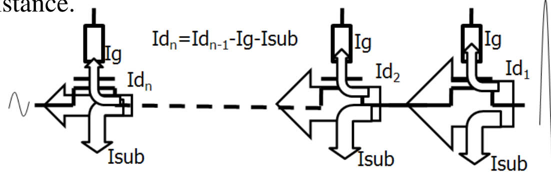

Fig. 2 Different amount of Id flowing through each transistor in a long chain causes voltage imbalance

The challenge of an SOIFET model is its non-linearity prediction. Depending on the mode of operation, the non-linearity of a FET is caused by different mechanisms. A typical switch consists of a number of transistors stacked in series and in shunt to ground as shown in Fig. 1. The number of stacked transistors in series is determined by the maximum voltage for reliable operation of a transistor as well as the maximum voltage switch at the antenna port. When a transistor is fully ON, the non-linearity is mainly contributed by the transistor ON resistance. When a transistor is OFF, the linearity is influenced by not only the C_{OFF}, but also other parasitics. At higher power levels the high voltage swing appearing at the antenna port can turn the first few transistors weakly ON through a significant amount of voltage imbalance, i.e. the voltage drop is not evenly distributed across each transistor in a chain. As shown in Fig. 2, voltage imbalance of a transistor chain is caused by the additional currents required to supply the loss through the substrate and the gate resistor. It can also induce gate-induced drain leakage (GIDL), enhanced by the parasitic bipolar effect in an SOI FET.

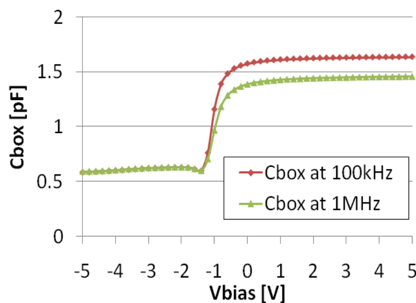

Fig. 3 CV measurement of a large active area over the box oxide

Besides the non-linearity caused by the transistor, the substrate is also an important source of non-linearity. It is commonly perceived that the buried box oxide capacitance to the substrate is a constant, thereby introducing minimal non-linearity to the overall system. However, a simple CV measurement on a large active area over the buried box oxide reveals it behaves just as non-linear as a MOS capacitor. Fig. 2 shows the CV measurement of a large active area over an SOI substrate. The measurement reveals that 1) the capacitance is far from being a constant over the voltage; 2) the substrate, i.e. the semiconductor side of the MOS cap, behaves more like an N-type substrate rather than a P-type; and 3) the effective capacitance decreases as the measurement frequency increases.

The frequency dependence observed in Fig. 3 is mainly dictated by how fast the accumulation layer underneath the box oxide can be charged and discharged. The good news is that the high substrate resistance limits the bandwidth of the non-linear response of the box oxide capacitance. However, the box capacitance is still fairly non-linear at the GHz range. Fig. 4(a) shows the impedance into the substrate as a function of the bias voltage measured at 1GHz. Although the percentage change of the box capacitance is bandwidth limited, the effective impedance looking into the substrate still appears quite significant at high frequencies. The non-linearity of the box oxide capacitance can also be observed through the HF coupling between two adjacent active structures, as seen in Fig. 4(b).

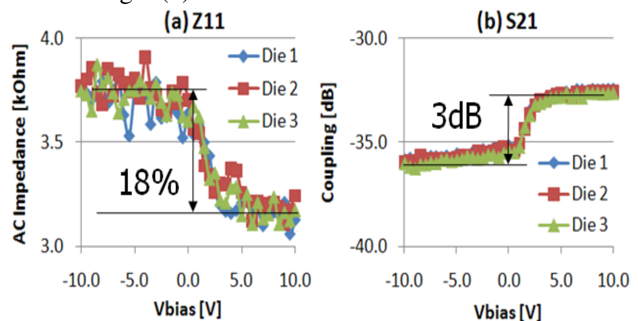

Fig. 4 Two-port s-parameter measurement result on an active-to-active coupling test structure: (a) measured impedance (Z11) looking into the substrate from an active island through the box oxide; (b) measured coupling (S21) between two adjacent active structures at 1GHz.

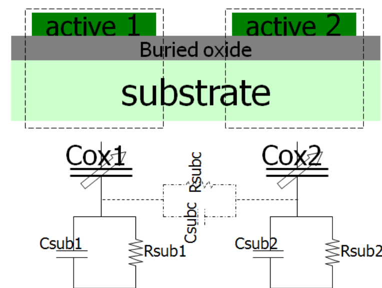

Fig. 5 A simple model for the non-linear substrate

According to an analytical calculation, the amount of AC current going into a substrate of 1000Ohm-cm through a 0.5um thick box oxide represents ~5% of the total AC current going into the drain side of the transistor when it is OFF. The percentage of the substrate current could become higher if the effective substrate resistivity is lower. Assuming a simple non-linear model as shown in

Fig. 5 that produces a small-signal response of Fig. 4, simulation indicates that the non-linear substrate will set the 2nd and 3rd harmonic floors to -50 and -60 dBm levels respectively at an input power of 35dBm, and the result was confirmed with a simple measurement on a plain metal line on the substrate.

III. MODEL IMPLEMENTATION

The PSP model was selected for the SOI FET in the switch simulation for three reasons: 1) being a body-referenced model, PSP is more appropriate than a source-referenced model like BSIM for switch simulation purposes; 2) the bulk version of the PSP model enables simple integration of a user-defined substrate model; and 3) the model is readily available in major simulators such as ADS and Spectre. However, the bulk-version of the PSP model, as compared to PSPSOI [4], is incapable of modeling the floating body effect and the enhanced parasitic BJT effect [5], which are the main physical mechanisms differentiating an SOI FET from bulk CMOS.

The floating-body effect is most severe in a partially depleted (PD) SOI device and is manifested as a threshold voltage (Vth) change and sudden change of the output conductance, i.e. Kink effect. The floating-body effect results mainly from the minority carrier accumulation in the body, which requires certain current flowing in the channel and a relatively high V_{DS} to trigger some impact ionization in the drain depletion region. Fortunately, the bias condition for these effects to occur is usually quite far away from where a switch is operated. Moreover, these effects are usually DC-like effects, i.e. with relatively high time constants. Therefore, as an RF switch is concerned, these effects can be empirically modeled as a slight Vth adjustment, even if it is not necessary.

The parasitic bipolar effect still needs to be carefully considered as it will inevitably enhance the GIDL current, which could influence the linearity of an OFF transistor when the voltage swing is high. The bulk-version of the PSP model has a built-in GIDL current model, however, without the parasitic bipolar effect. The amount of amplification at higher frequencies is determined by how fast the parasitic BJT can track the high speed signal, i.e. by the bandwidth of the transistor. As the amplification of the parasitic BJT is very difficult to be measured at GHz range, the effect is validated indirectly by the large-signal characterization of a single shunt FET. By the harmonic data obtained so far, it is suggested that the GIDL current of an SOI FET at GHz range behaves more like one with little amplification, as the gain of the parasitic bipolar diminishes with the frequency.

SOI tends to have a more severe self-heating effect than the bulk CMOS, as the oxide layer has a much lower thermal conductivity than Si. Since the time constant of the self-heating effect is usually in µS or even mS range, the device temperature rise can be treated simply as an average ambient temperature change for a switch operating at GHz range. The local temperature rise of a particular arm in a switch can be calculated with the insertion loss, the thermal resistance of the switch section, and the power level.

Fig. 6 shows a simplified diagram of the final hybrid model used for SOI switch application. The FET portion of the switch is modeled by the bulk-version of the PSP model. The body node of the device is then connected to the substrate through a MOS varactor. As the total loss into the substrate is the most critical factor to determine the voltage imbalance of a switch made of many (>10) transistors stacked in series in the OFF state, the substrate network is generated with an electro-magnetic (EM) simulation according to the layout. The substrate loss consists of two components: the vertical loss into the substrate and the lateral loss into the adjacent structures. According to the S-parameter characterization on the active-to-active substrate coupling structures of various sizes and spacing, it is discovered that the lateral loss can be more significant than the vertical loss as the spacing between the two un-related active structures decreases. Therefore, a layout-dependent EM approach was adopted here.

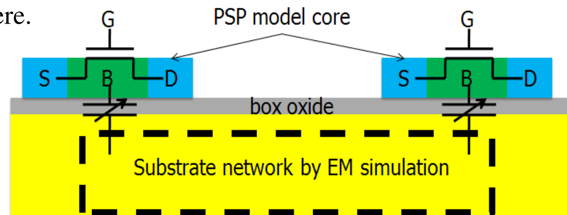

Fig. 6 A simplified diagram of the hybrid model for SOI switch modeling

It is known that EM simulation does not account for any non-linearity. Therefore, the MOS varactor portion has to be excluded from the EM simulation and treated separately. It is done by performing the EM simulation on only the substrate beneath the box oxide with a simple metal contact on top of the substrate, which is equivalent to having the electrical excitation projected from the active area above. The methodology of cascading an external cap on top of the EM simulation of only the substrate is verified to yield the same result of an EM simulation with the box oxide and the active layers. This simple setup makes the EM simulation very efficient for even a very large and complex layout. The EM simulation can be done in the floor planning stage, since it needs only the active area information in the layout.

IV. MEASUREMENT RESULT

The switch test structures were manufactured with a 0.13µm SOI CMOS process. The FET used for the switch design is the 2.5V IO device with thick oxide. The substrate network that accounts for both the vertical loss into the substrate and the lateral loss to the adjacent structures was generated with the 2.5D Momentum simulation. The final switch simulation was performed with ADS Harmonic Balance simulation with RFDE interface, which enables easy co-simulation of schematic and layout-dependent EM simulation result.

Fig. 7 shows the measured harmonic data versus the model of a 12-stacked FET switch of 2.5mm width each. As shown in the figure, the 2nd harmonic is enhanced by the substrate non-linearity by a few dBs. Data of other series switches with different transistor widths indicate that the 2nd harmonic increases with the total FET area, agreeing that the 2nd harmonic correlates with the substrate non-linearity.

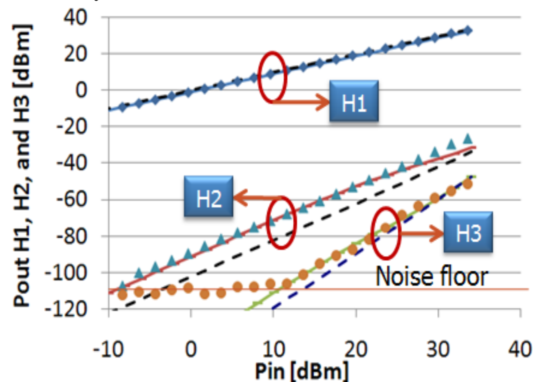

Fig. 7 Harmonic data versus model of a 12-stacked series FET switch of width 2.5mm at VG=2.0V, Freq=900MHz. The solid lines represent the prediction with the non-linear substrate; the dashed lines represent the prediction without the substrate non-linearity.

Fig. 8 shows a comparison of different models for a switch sub-block with a 12-stacked shunt branch and a 12-stacked series branch. As shown in the figure, the simulation of the full-blown model matches the measured data very well. The short-dashed lines show the simulation without any transistor non-linearity. This was done by representing the transistor by just an ON or OFF resistor, according to its state. As shown by the short dashed lines, the 2nd harmonic is pretty much dictated by the substrate non-linearity. As shown by the long dashed lines, the 2nd harmonic prediction could be off by more than 20dB if the substrate non-linearity is not properly accounted for.

V. CONCLUSION

A hybrid modeling methodology that combines the mature bulk PSP model and a layout-dependent nonlinear substrate model is introduced for SOI switch applications. The proposed model is shown to be sufficient for switch harmonic simulation up to a very high power-level of ~35dBm required by cellular applications.

ACKNOWLEDGEMENT

The authors wish to acknowledge their colleagues Ed. Lawrence in Cedar Rapids, IA and Steve Sprinkle in Woburn, MA, in the switch modeling discussion and in providing the system-level characterization data.

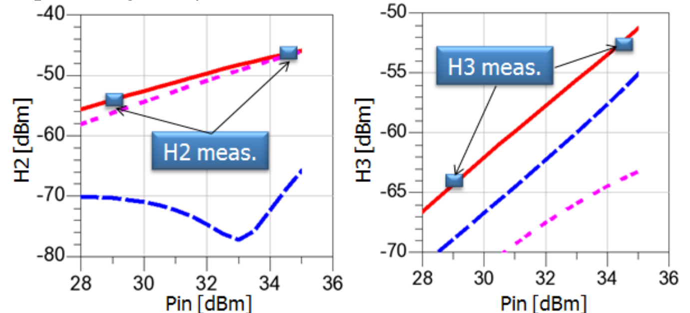

Fig. 8 Harmonic simulation of a 12 stacked shunt switch and 12 series switch together. The two symbols are the measured data at Pin=29 and 34.5 dBm; the solid lines represent the prediction of the full-blown model with the non-linear substrate, while the long-dashed lines with the linear substrate and the short-dashed lines with the transistor modeled as a linear resistor.

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