Power Detection and Control
For Mobile Handset Applications

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Part 3. Power Control Feedback

Direct detection architectures can sample the amplifier output directly but will suffer from similar VSWR inaccuracy that was observed in the indirect architectures. Often a directional coupler is required to sample the RF waveform and provide visibility to the forward power delivered to the load. This coupler can be integrated on the detector die, implemented with discrete components or embedded with the printed circuit board. Figure 1 shows an example embedded coupler used in low cost amplifier modules. Along with the coupler, a complex termination is often required to optimize the coupler directivity over a narrow bandwidth.

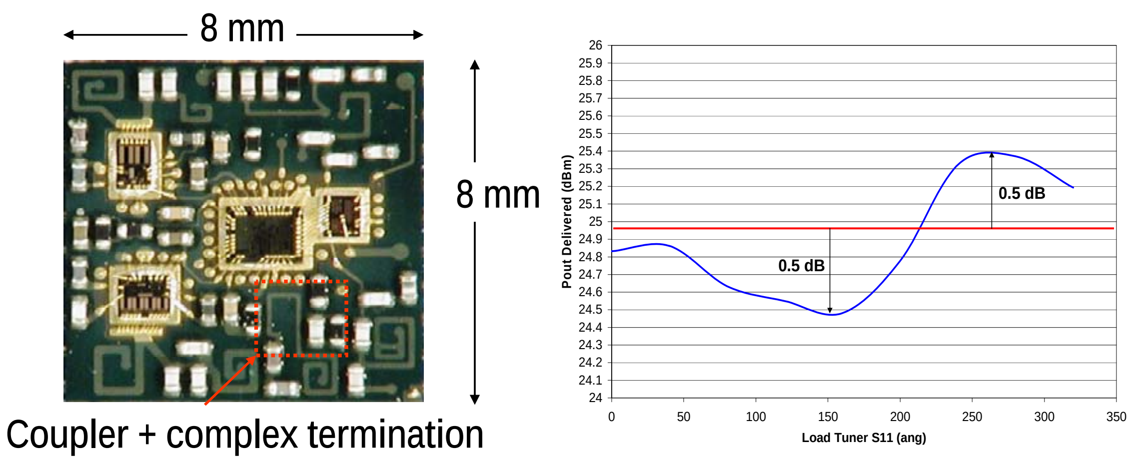

Fig. 1. Example embedded coupler and resulting closed loop control accuracy.

With careful design of the impedance characteristics at the coupler interface and attention to isolation and signal routing, extremely high directivity can be achieved providing excellent power detection accuracy into non-ideal load conditions. The plot of figure 1 shows typical detection accuracy using a log detector interfaced with a tuned, embedded coupler.

As discussed in part 1 of this article, the various power control techniques exhibit significant sensitivity to temperature, supply, and RF drive levels while the indirect and direct detection techniques offer very accurate indication of the transmit power. Feedback is required to autonomously adjust the amplifier bias and maintain a constant detected voltage. Design of this feedback loop must consider offset accuracy, bandwidth, noise, and transient characteristics. The feedback commonly makes use of an integration amplifier to compare a reference control voltage against the detected output signal as shown in figure 2. The bandwidth of this control loop is often selected to be as high as possible while still maintaining stability and transmit noise performance. Significant variation of the bandwidth over the full output dynamic range is often observed due to the large variation in the derivative of the amplifier control and detector response characteristic. The loop bandwidth and stability must be checked over the entire dynamic range.

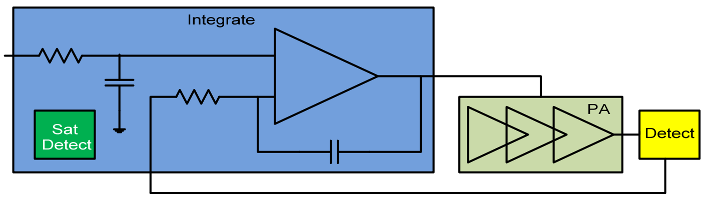

Fig. 2. Control Loop with integrating feedback.

Also associated with loop bandwidth is slew rate and acquisition time. The time required for the integrator to slew its output is indirectly proportional to the magnitude of the input voltage. In the case of a simple peak detector and current sense, the input voltage is very small at low output powers which requires high bandwidth or an extended time requirement for the loop to reach steady-state. As shown in figure 3a, limited time is allocated for the power amplifier to active, stabilize and ramp to the desired power level. The greater low power voltages associated with voltage sense and log detection provide significant advantage for the turn-on timing of the amplifier burst.

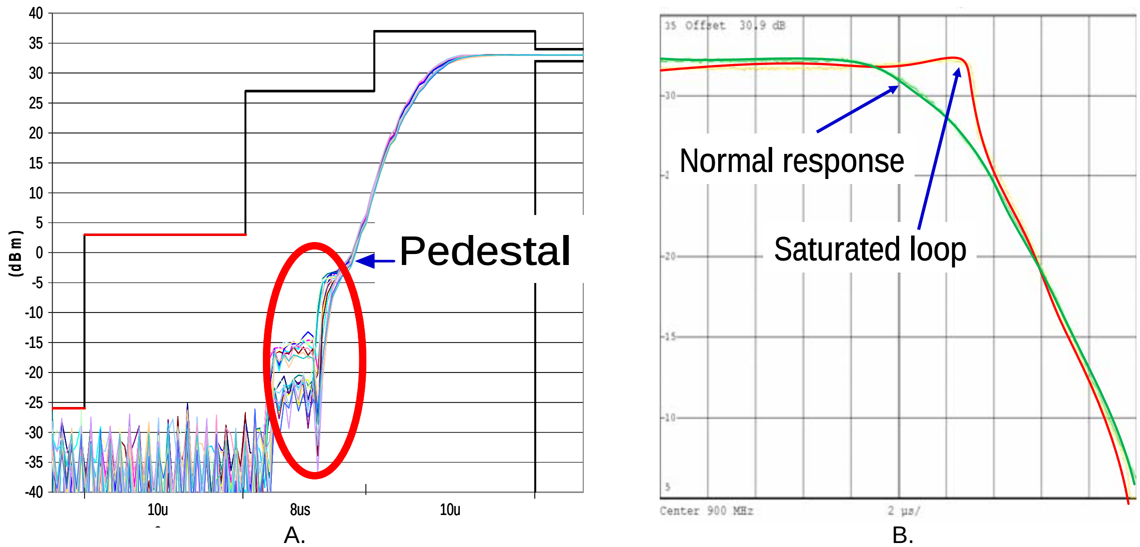

Fig. 3. Control loop transient response. A. Rising edge showing critical acquisition timing. B. Falling edge showing effects of saturated control loop.

Saturation of the amplifier output power is unavoidable when operating at low battery conditions and into non-ideal load conditions. This limited output power condition of the amplifier leads to saturation of the power control loop as it acts to increase the amplifier bias and increase the output power. Often, the integrator output will be driven to its maximum value during the transmit burst. At the end of the transmit burst, the reference input to the integrator is reduced and the integrator output will begin to slew down in an attempt to reduce the output power. As shown in figure 3b, the slewing of the integrator output from the maximum value down to a bias point at which the output power begins to respond results in significant delay and distortion in the ramp shape as the output power "snaps" down. This same effect occurs in the linear regulator for the voltage control architecture as the feedback loop in the regulator saturates at low supply.

Significant design effort must be spent to control the loop characteristics in saturation. Initially, a method of detecting saturation must be defined. For current sense and voltage control, saturation detection is nearly impossible. These architectures need to directly address the transient characteristics by preventing saturation of the integrator or controlling the slewing characteristics as it exits saturation. Detection of saturation for loops using peak detection and log detection is straight-forward. Often, when saturation is detected, this signal is used to trigger slight reduction in the reference voltage until the loop comes out of saturation. In nearly all cases the maximum power of the amplifier must be sacrificed to ensure a clean transient response.

Many performance aspects must be considered in the design of power amplifier bias control and power detection. Next generation products combining multiple modes require even more complex solutions to meet the increasing demands of the market. New and unique applications of the fundamental components discussed in this paper will be required to meet the challenging size and cost requirements of new products while delivering unprecedented accuracy, noise, and transient performance.

David S. Ripley received his B.S. degree in electrical engineering from Iowa State University, Ames, in 1992 and the M.S. EE degree from National Technical University (NTU), Minneapolis, MN, in 2002. From 1992 to 1999, he worked in the Cellular Subscriber Division, Motorola, Libertyville, IL, where he was involved in the design and development of TDMA and AMPS handsets including RFIC design of receiver and synthesizer functions. Since 1999, he has been with Skyworks Solutions, Inc. (previously Conexant Systems, Inc.), Cedar Rapids, IA, where he has been involved with the design of multiband HBT power amplifiers modules for the GSM and CDMA cellular handsets. He holds seven patents.