Recent Progress in III-V Devices and Modules for Next Generation Mobile Handsets

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Over the past decade, III-V devices, and modules containing them, have dominated the market for RF front end electronics in mobile handsets. GaAs-based hetero-junction bipolar transistors (HBTs) have solidified their position as the technology of choice for fabricating wireless handset power amplifiers (PAs) and GaAs-based field effect transistors (FETs) have become the preferred choice for the high performance RF switches used in most of the smart phones today. With wireless broadband data clearly becoming the new catalyst igniting the growth of next generation mobile devices, RF front end architectures and solutions demand greater flexibility to support multimode, multiband (MMMB) operation and at the same time meeting the competitive requirements of high efficiency, good linearity, compact module size, reduced component counts, low cost, and short time to market. To meet these stringent size, cost, performance and schedule challenges in a rapidly evolving wireless communication industry, a high yield and comprehensive III-V process and module technology portfolio with short product design cycle times is critical to marketplace success. Skyworks Solutions is in a unique position - possessing strong in-house GaAs HBT and FET manufacturing capability, multi-chip module packaging expertise, and assembly/test technologies. Taking advantage of the combination of this strong technology portfolio and our RF design expertise, Skyworks is providing innovative RF front end solutions with functional integration at both the die and package level. In this invited talk, Skyworks' development strategies for HBT- FET integration (on-die co-integration and/or die stacking approaches) to address the needs of increasing functionality and design flexibility will be presented.

There are numerous publications describing the integration of III-V FETs and HBTs [1-5] dating back to the late 1980s. We have evaluated several of these possible on-chip integration approaches and found most of these methods having drawbacks with respect to high-volume manufacturing. Due to our stringent yield requirement in a cost conscious environment, a merged BiFET approach was selected and developed as the best compromise. A schematic cross sectional profile of this high yield, manufacturable BiFET is shown in Figure 1. In a high-volume GaAs HBT production environment, the starting epitaxial materials need to be "pre-screened" for important parameters and sufficient quantities should be kept in inventory or in consignment for lot starts. A "quick-lot" (QL) process is often used by material suppliers to ensure that the HBT wafers they ship meet desired specifications. Certain critical HBT parameters such as beta, turn-on voltage, and sheet resistances must be within a specified range. With the addition of the FET to the technology, it is desirable to establish a similar "FET QL" to determine important FET parameters, such as pinch off voltage, V_p, and saturation current, I_{dss}, before processing the wafers. Failure to implement this sort of QL strategy can result in very costly yield issues or scrapped lots since FET data is not normally collected until after all of the effort, and expense, of fully processing the wafer. An etch stop layer is included in the BiFET profile to ensure better process and pinch-off voltage control. The merged construction of the FET in the emitter of the HBT has also led to an excellent analog 4 terminal FET device, rather than a conventional 3 terminal FET when integrated below the HBT sub-collector. By connecting the 4th terminal (indicated as BG in Fig.1) to either Gate (G) or to source (S), one can effectively tune the threshold, control the leakage, and double the effective trans-conductance. To add the FET into the HBT profile, an important epi design consideration is that the HBT RF performance and circuit level yield cannot be compromised. With careful design, this embedded FET with an added etch-stop layer does not degrade the HBT performance. A BiFET process with good RF power performance has been demonstrated and comparable line yields and circuit yields between our merged BiFET process and our standard high yield HBT process are obtained at Skyworks' Newbury Park fab.

FETs in the above mentioned merged BiFET technology are primarily used in the bias circuits and low-frequency switching applications, which are less demanding for RF performance, due to the higher on resistance (R_{on}) and relatively poor RF isolation. Modern multimode RF front end architectures require high performance and/or high throw count RF switches with stringent requirements for insertion loss, harmonics and inter-modulation performance

at operating frequency bands. High performance RF switches demand optimized FET device topologies to achieve best-in-class performance at the module level. Although a monolithic integration of RF FET in an HBT technology may lead to reduced form-factors at the module level, fabricating all of the RF subsystem on a single chip (SOC) can result in poor yield and sub-optimal performance. To overcome the yield and performance concerns of SOC, die stacking and/or MCM technology or system in a package (SiP) approaches provide alternative solutions to the problem of incorporating various RF functions, if such advanced packaging solutions are readily available at low cost. Using our internal state-of-the-art production assembly capability provides improved module performance with high yields and a cost-effective design and manufacturing solution by die-stacking. An example of a pHEMT based switch stacked on top of a HBT PA in a 3 mm X 3 mm form-factor WCDMA PA module without sacrificing performance or size, is shown in Fig. 2. The tradeoffs and challenges of die stacking especially for RF dies and the accomplishments which have been achieved will also be discussed in the presentation.

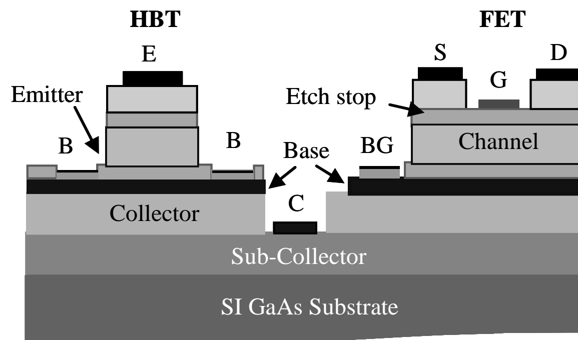

Figure 1: Schematic cross section of an integrated HBT and FET. S, D, G, BG are the source, drain, gate and back-gate contacts of the FET and E, B, C are emitter, base and collector contacts of the HBT, respectively.

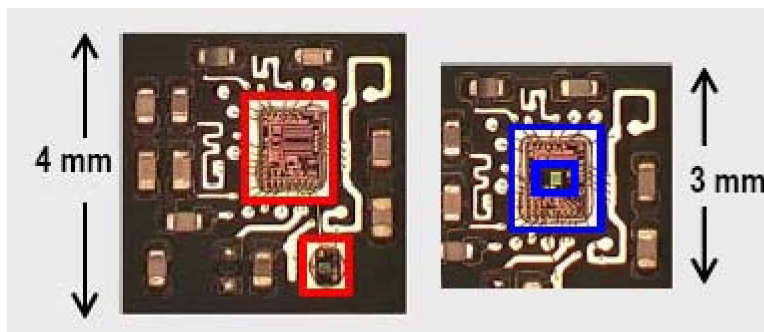

Figure 2: Die stacking the pHEMT switch on top of the HBT power amplifier reduces package size from 16 mm^2 to 9 mm^2.

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