APPLICATION NOTE

Direct Digital Modulation Using the SKY72300, SKY72301, and SKY72302 Dual Synthesizers/PLLs

Direct digital modulation is a unique modulation method that eliminates many previously required components from a radio transmitter to create a simple, flexible, cost effective alternative.

This Application Note describes a modulation method (see Figure 1) in which a synthesizer directly generates a modulated carrier frequency. The synthesizer acts as a "digital-to-frequency" converter. The output can be frequency modulated by simply changing a digital word. The direct digital modulation feature allows quick stepping of the carrier (Voltage Controlled Oscillator [VCO]) through a range of frequencies, effectively creating an Frequency Modulation (FM), Frequency Shift Keying (FSK), Minimum Shift Keying (MSK), Gaussian Minimum-Shift Keying (GMSK) or other constant envelope continuous phase signal.

To design with this feature, a mathematical expression for the modulated signal is needed to determine the instantaneous frequencies. The offset (difference between the desired instantaneous frequency and the channel carrier) is programmed into the synthesizer using a serial interface. A modulated signal is created from many rapid, momentary discrete frequency steps. The programming values used to create this modulated signal can be stored in a simple look-up table, so little or no system CPU processing power is needed.

Modulation schemes that modulate the carrier's Binary Phase-Shift Keying (BPSK), Quadrature Phase-Shift Keying (QPSK), and their variants possess sudden steps in phase ($\pm\pi$ or $\pm\pi/2$) at the symbol boundaries (i.e., they are not phase continuous). These steps in phase translate into frequency impulses. The instantaneous frequency offset at the symbol boundaries during these phase steps is infinite, assuming an ideal modulator. This frequency impulse can be approximated using the SKY72300, SKY72301, or SKY72302 with a momentary, transient frequency change. This Application Note only discusses frequency-based modulation schemes such as FM, FSK, MSK, and GMSK.

Skyworks SKY72300, SKY72301, and SKY72302 dual synthesizers have the required architecture to support accurate direct digital modulation of continuous-phase, constant-amplitude modulation schemes at high RF frequencies (up to 6 GHz).

Designing With The Direct Digital Modulation Feature

Four parameters need to be considered when direct digital modulation is used to design an application using either the SKY72300, SKY72301, or SKY72302 synthesizer: step size, maximum date rate, modulation data word length, and peak deviation.

Step Size

The step size defines the minimum discrete frequency step that the synthesizer can use to generate the modulated carrier.

Skyworks dual synthesizers have an 18-bit fractionality giving 2^{18} or 262144 steps between integer-N boundaries at the VCO frequency. The equation used to determine step size is:

$$Step\ Size\ (Hz) = \left(\frac{F_{xtal} / R}{2^{18}} \right)$$

where: F_{xtal} = the crystal frequency reference.

R = an integer value ranging from 1 to 32 used to divide the crystal reference frequency to arrive at the internal reference frequency, F_{ref} (also referred to as the comparison frequency).

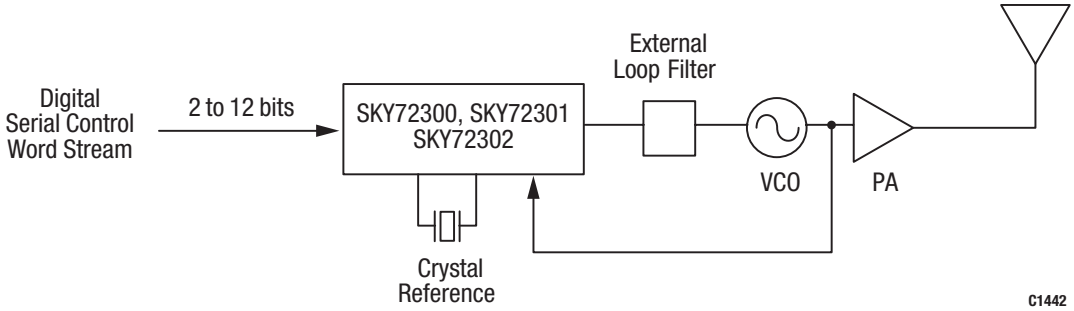

Figure 1. Crystal Frequency vs Temperature Curve

Example 1:

Using a 20 MHz crystal and a reference division of $R = 1$:

$$Step\ Size = \frac{20\ MHz / 1}{262144}$$

$$Step\ Size = 76.29\ Hz$$

This represents the minimum step size achievable with a 20 MHz crystal oscillator and $R = 1$.

Example 2:

Using a 50 MHz crystal and a reference division of $R = 2$:

$$Step\ Size = \frac{50\ MHz / 2}{262144}$$

$$Step\ Size = 95.4\ Hz$$

This represents the minimum step size achievable with a 50 MHz crystal oscillator and $R = 2$.

It is recommended that the value of the internal reference frequency divider, *R*, be set to 1 or 2 as this will be a limiting factor on the data rate.

Data Rate

The maximum data rate is limited by three factors: loop bandwidth, internal reference frequency, and serial interface and sample rate.

Loop Bandwidth Affect. The SKY72300, SKY72301, and SKY72302 synthesizers all feature the ability to increase the loop bandwidth relative to conventional integer-N synthesizers since they allow operation with a very high internal reference frequency (up to 25 MHz) while still maintaining fine resolution step size (<100 Hz).

Using the direct digital modulation technique, the data is actually inside the Phase Lock Loop (PLL). In other words the loop bandwidth in Figure 1 is wide enough to pass the modulation frequencies to the VCO. The VCO output (carrier plus data) is fed back to the internal Phase/Frequency Detector (PFD).

The loop bandwidth must exceed the data bandwidth. Otherwise, the loop attenuates the data.

An expression to approximate the maximum allowable data rate in a given bandwidth or, in this case, the loop bandwidth is given by Equation (1):

$$datarate_{max}(bps) \approx \frac{1}{BT} \times loop\ bandwidth \qquad (1)$$

where: BT = the data bandwidth multiplied by the bit period, in Hz/bps. This is also equal to the data bandwidth divided by the data rate.

Table 1. Relative Bandwidth for Various Modulation Schemes

Standard	Relative Bandwidth (*BT*)
GMSK	0.5
MSK	1.5
OFSK	2.0

BT is called the *relative bandwidth* or *bandwidth expansion factor* and is related to spectrum efficiency through Shannon's equation. Spectrum efficiency is a function of how many bits per second of data for each Hz of bandwidth are available. Some *BT* values are listed in Table 1 for several modulation schemes.

Example 3:

Approximate the maximum data rate given a GMSK system with a loop bandwidth of 100 kHz and $BT = 0.5$:

$$datarate_{max} \approx \frac{1}{0.5} \times \frac{bps}{Hz} \times 100\ kHz$$

$$datarate_{max} = 200\ kbps$$

Therefore, in a GMSK system with $BT = 0.5$, the maximum data rate in a 100 kHz loop bandwidth would be 200 bps.

Internal Reference Frequency Affect. The second limit on the data rate is imposed by the choice of internal reference frequency, F_{ref}. This limitation is due to the internal $\Delta\Sigma$ modulator used to generate the fractional divides.

Fractional divides operate by momentarily dividing by pseudo-randomly selected integer values of N. Averaged over a long period of time, these integer N values result in a specific fractional divide value. If the applied data rate is too high, the $\Delta\Sigma$ modulator is not allocated sufficient time to output enough pseudo-randomly chosen divide values to yield the required fractional divide value (which ultimately specifies the required momentary VCO frequency).

The formula to approximate the maximum data rate is given by Equation (2):

$$datarate_{max}(bps) = \frac{1}{BT} \times \frac{(F_{xtal}/R)}{100} \times \frac{1}{\#\ samples\ per\ symbol} \qquad (2)$$

where: R = F_{xtal} divided by F_{ref}

samples per symbol = number of frequency steps per data symbol required to generate the modulated carrier.

Example 4:

Using the GMSK loop bandwidth example where $BT = 0.5$, approximate the maximum modulation data rate by using a 50 MHz crystal frequency and a divider ratio of $R = 2$.

Assume that the number of frequency steps per data symbol is 10 *(# samples per symbol* = 10). This implies that for each data bit transmission, there will be five incremental frequency steps up to the maximum frequency deviation followed by five frequency steps back to the carrier frequency.

$$Data\ Rate_{max} \approx \frac{1}{0.5} \times \frac{bps}{Hz} \times \frac{50\ MHz/2}{100} \times \frac{1}{10}$$

$$Data\ Rate_{max} = 50\ kbps$$

Therefore, the maximum data rate using an internal reference frequency of 25 MHz would be 50 kbps.

Serial Interface and Sample Rate Affect. The time required for a frequency change to be initiated by the synthesizer is given by Equation (3):

$$t_{FrequencyChange} = t_{3IntRefCycles} + t_{ModWordLength} \quad (3)$$

In this equation, $t_{ModWordLength}$ is determined by the serial interface clock rate and the modulation data word length. The value of $t_{3IntRefCycles}$ is three period times of the internal reference frequency (comparison frequency). The serial interface chip select signal ($\overline{CS}$) must go high for a minimum of three cycle periods of the internal reference frequency between Modulation Data Register (address 0x9) writes.

Once it's known how to determine the time needed to initiate a frequency change, the maximum sample rate can be determined. In this case, sample rate implies the rate at which modulation data words are written to the synthesizer to create the modulated signal.

$$Sample\ Rate_{max} = \frac{1}{t_{FrequencyChange}} \quad (4)$$

The maximum sample rate determines the maximum number of discrete frequency steps that can be used to create a symbol element of the modulation scheme. Some schemes allow as few as one frequency step per bit or symbol while others, analog FM for example, require many intermediate frequency steps to "sweep out" the modulation signal.

The sample rate does not necessarily have to operate at its maximum limit to achieve good performance. The type of modulation scheme and the degree of emulation that the designer needs to achieve determines the minimum allowable sample rate. Best emulation of the modulation scheme is usually, but not always, offered with a high sample rate.

A design example for MSK is provided at the end of this Application Note. This example shows that the required sample rate for MSK is equal to the desired transmitter bit rate. To achieve a 100 kbps transmit data bit rate, a sample rate of only 100 ksamples per second is required.

The minimum serial interface data rate is given by Equation (5):

$$Serial\ Rate_{min} = \frac{Sample\ Rate \times Bits\ per\ Sample}{1 - t_{3IntRefCycles} \times Sample\ Rate} \quad (5)$$

It is important to understand the meaning of this calculated serial interface rate. Although Equation (5) appears complicated, it merely ensures that there is sufficient time allocated between the modulation data word writes to allow $\overline{CS}$ to cycle high. Recall that between each modulation data word write cycle, $\overline{CS}$ must go high for a minimum of $t_{3IntRefCycles}$. $\overline{CS}$ must cycle for each register write; it cannot be left low for multiple register writes.

Example 5:

Calculate the maximum sample rate of a direct digital modulator if the serial bus is clocked at 50 MHz and the modulation word length is 12 bits with a 25 MHz internal reference frequency. Also calculate the minimum serial interface data rate required.

$$t_{FrequencyChange} = \frac{3}{25\ MHz} + \frac{12}{50\ MHz}$$

$$t_{FrequencyChange} = 360\ ns$$

The maximum sample rate is:

$$Sample\ Rate_{max} = \frac{1}{360\ ns}$$

$$Sample\ Rate_{max} = 2.777\ Msamples\ per\ second$$

This is the fastest allowable sample rate for a system using a 50 MHz serial clock with a 12-bit modulation word length and 25 MHz internal reference frequency.

Therefore, using Equation (5) the minimum serial interface data rate is:

$$Serial\ Rate_{min} = \frac{2.777 \times 12}{1 - \frac{3}{25} \times 2.777}$$

$$Serial\ Rate_{min} = 49.979\ MHz$$

Example 6:

Assuming that each data symbol of a GMSK signal can be represented with 25 samples, determine the maximum GMSK data rate given a serial interface speed of 50 MHz with a 12-bit modulation word length and 25 MHz internal reference frequency.

Example 5 showed a maximum sample rate of 2.777 Msamples per second. Each data symbol requires 25 samples. Therefore, the maximum data rate is:

$$Data\ Rate_{max} = \frac{2.777}{25}$$

$$Data\ Rate_{max} = 111.08\ kbps$$

Example 7:

Assuming that each data symbol of a GMSK signal can be represented with 10 samples, determine the maximum GMSK data rate given a serial interface speed of 50 MHz with a 12-bit modulation word length and 25 MHz internal reference frequency.

Again, using 2.777 Msamples per second from Example 5, the maximum data rate is:

$$Data\ Rate_{max} = \frac{2.777}{10}$$

$$Data\ Rate_{max} = 277.77\ kbps$$

As this example and Example 6 indicate, the number of samples per data symbol greatly influences the allowable data rate.

Data Rate Limit Summary. The lowest of the above three data rate limits imposes the upper limit on the data rate.

Depending on the required system spectral efficiency, the above GMSK example using a 100 kHz loop bandwidth, 50 MHz serial clock with 12-bit modulation data word length, and 25 MHz internal reference frequency could allow a maximum data rate ranging from 50 to 200 kbps.

Programmable Modulation Word Length

The modulation data word is adjustable in length from 2 to 12 bits. The Modulation Data Register (address 0x9) uses a signed 2's complement format with maximum range of –2048 to +2047 (2^{12}). The desired word length is selected by truncating the chip select signal after the desired number of bits have been transferred to the synthesizer. The word length ultimately defines the maximum number of frequency steps between the carrier frequency and the peak deviation frequency. Not all the frequency steps need to be used; however, more steps enhance the emulation of the modulation scheme.

Instantaneous frequency deviation is determined by the value programmed into the Modulation Data Register and the step size. The calculation is as follows:

$$Deviation\ (Hz) = ModData_{10} \times Step\ Size$$

The Modulation Data Register is programmed using either the Data or the Mod_in pins (27 and 2, respectively) of the synthesizer. It is this register that is repeatedly accessed to create the modulation waveform.

Example 8:

Calculate the instantaneous deviation assuming a step size of 76.29 Hz and the maximum modulation data word of 2047_{10} (12-bit word length).

$$Deviation\ (Hz) = 2047 \times 76.29$$

The maximum deviation that the Modulation Data Register can accommodate given a 76.29 Hz step size is 156.165 kHz.

Programmable Peak Deviation

Peak deviation defines the maximum frequency change from the carrier frequency for the specific modulation scheme. The peak deviation offered by the Modulation Data Register can be scaled allowing the designer two possible benefits:

- The actual step size can be increased (multiply by 2^x) if the step size defined by the internal reference frequency is too small.
- The maximum range of frequency deviation for a given modulation word length can be increased (maximum peak deviation is multiplied by 2^x).

This scaling is performed by the Modulation Data Magnitude Offset factor (address 0x8, bits 7 to 4). When this is used, the instantaneous frequency deviation is determined by the value programmed into the Modulation Data Register, the step size, and the Modulation Data Magnitude Offset factor. The calculation is as follows:

$$Deviation\ (Hz) = ModData_{10} \times 2^{ModMagOffFactor} \times Step\ Size$$

The Modulation Data Magnitude Offset factor is programmed using the Data pin (pin 27) of the synthesizer. Valid values range from 0000_2 to 1100_2 depending on the modulation word length. This defines the number of column bit shifts that the 2 to 12-bit modulation data word is shifted (multiplied by) once inside the SKY72300, SKY72301, or SKY72302. The Modulation Data Magnitude Offset factor is only programmed once for a specific modulation format.

Example 9:

Calculate the peak deviation based on a step size of 76.29 Hz and a Modulation Data Magnitude Offset of 0000_2.

$$PeakDev\,(Hz) = 2047 \times 2^{0} \times 76.29$$

Therefore, given a step size of 76.29 Hz, the maximum frequency deviation is 156.165 kHz (with the same configuration as in Example 8).

Example 10:

Calculate the peak deviation based on a step size of 76.29 Hz and a Modulation Data Magnitude Offset of 1100_2 (12_{10}).

$$PeakDev\,(Hz) = 2047 \times 2^{12} \times 76.29$$

Therefore, given a step size of 76.29 Hz, the maximum frequency deviation is 639.65442 MHz. Obviously, this combination of word length and Modulation Data Magnitude Offset is not a practical configuration.

In any given application, it is not always required or possible to achieve the full scale frequency deviation that the combined Modulation Data Register and Modulation Data Magnitude Offset can provide. The required peak deviation is always determined by the system requirement.

Although the Modulation Data Register (address 0x9) is a 14-bit register, a maximum of 12 bits can be transferred to it using the serial interface. To use all 14 bits of the register, it is necessary to use the Modulation Data Magnitude Offset feature which shifts the serial word up into the two inaccessible MSBs of the register.

It should be apparent that the maximum value of the Modulation Data Magnitude Offset is determined by the modulation data word length. Examples 11 and 12 illustrate how to calculate the maximum Modulation Data Magnitude Offset values.

Example 11:

Calculate the maximum *ModMagOffsetFactor* assuming a 2-bit A/D converter is used to feed modulation data words to the synthesizer.

$$ModMagOffsetFactor_{max} = 14\ bits - 2\ bits$$

This means that a 2-bit A/D word can be shifted a maximum of 12 bits in the 14-bit register.

Example 12:

Calculate the maximum *ModMagOffsetFactor* for a 12-bit A/D converter. Using the same equation as in Example 11, a 12-bit A/D word can be shifted a maximum of 2 bits in the 14-bit register (14 bits – 12 bits).

Design Example for MSK Applications

Assume a 902 MHz synthesizer is used to generate a 100 kbps MSK data signal using an internal reference frequency of 20 MHz. The low-cost microcontroller to be used with the synthesizer runs at a serial port rate of 2 MHz.

The conventional approach to this design problem is to "pull" the reference crystal of the synthesizer. The amount of pull is determined by the data bit value. This requires many additional components (varactor, capacitors, resistors, inductors) combined with a calibration/alignment exercise after manufacture.

With either of the SKY72300, SKY72301, or SKY72302 synthesizers, the MSK modulated signal can be generated without additional components and requires no alignment procedure. This offers significant cost savings.

Mathematical Definition of an MSK Waveform

Analysis of MSK signalling indicates that the resulting signal consists of two tones equally spaced on either side of the carrier signal, f_c. The output tones appear at $f_c + \frac{1}{4}T$ and at $f_c - \frac{1}{4}T$, where $T = 1/(\text{bit rate in bps})$. Minimum tone spacing for MSK is $\frac{1}{2}T$.

The modulated MSK signal toggles between these two frequencies and is synchronized with the data transitions. For example, transmission of a +1 data symbol results in a tone at $f_c + \frac{1}{4}T$, while transmission of a –1 results in a tone at $f_c - \frac{1}{4}T$.

In this example, $T = 1/100$ kbps, which yields a frequency step of $\pm$25 kHz from the carrier.

The system's microprocessor must exercise protocol layer management with respect to data segmentation and addition of framing, channel synchronization, and seizure bits to the data stream. After these computations have been performed, the physical layer bit stream is known and the SKY72300, SKY72301, or SKY72302 can be programmed accordingly.

When the bit stream indicates a +1 for transmission, the processor sends a short digital word (possibly as small as two bits depending on system parameters) to the synthesizer instructing it to go to a new frequency of f_c + 25 kHz, or 902.025 MHz (keep in mind that if the previous bit was also a +1, the synthesizer is already at the correct frequency (with MSK modulation, frequency changes only occur if there is a change of data bit polarity. That is, +1 followed by –1 or vice-versa).

If the next bit in the stream is a –1, the processor sends another digital word to place the synthesizer at f_c – 25 kHz, or 901.975 MHz.

This exercise of writing to the synthesizer occurs at a 100 kHz rate, or every 10 μs as dictated by the bit rate.

The resolution step size for this example is given by:

$$Step\ Size = \frac{20\ MHz / 1}{262144}$$

$$Step\ Size = 76.293945\ Hz$$

The Direct Digital Modulation system on the synthesizer must step the carrier a total of:

$$Number\ of\ \ Steps = \frac{25\ kHz}{76.293945\ Hz}$$

This is equal to 327.68 resolution steps above and below the carrier frequency (rounded to 328). This requires a modulation data word length of 10 bits (2^{10} = 1024). This word length provides a maximum positive offset (deviation) of 511 step sizes and a maximum negative offset of 512 step sizes.

The modulation data word can be sent to the synthesizer using the Mod_in or Data pins (pins 2 or 27, respectively). Since this example uses a truncated transfer (only 10-bit), the Modulation Address Disable bit (address 0x8, bit 9) must be set to 1; otherwise, full 16-bit (address plus data) transfers are expected.

When a +1 data bit is to be transmitted, the associated modulation data word is $+328_{10}$ or 0101001000_2. A –1 data bit is transmitted by using a modulation data word of $–328_{10}$ or 1010111000_2 (the Modulation Data Register uses signed 2's complement format).

With these modulation data word values, the resulting modulation deviation is ±25024 Hz (+328 x 76.29 and –328 x 76.29), an error less than 0.1 percent.

Can this combination of data rate and internal reference frequency be accommodated by the synthesizer? The first limitation on data rate is imposed by the loop bandwidth. Using Equation (1):

$$100\ kbps \approx \frac{1}{1.5} \times loop\ bandwidth$$

Therefore, to transmit 100 kbps the required loop bandwidth is 150 kHz. The SKY72300, SKY72301, or SKY72302 can easily accommodate loop bandwidths in this range. Lower bandwidths can be used depending on required spectral efficiency.

The second limitation on data rate is related to the internal reference frequency. Using Equation (2):

$$Data\ Rate_{max}(bps) = \frac{1}{1.5} \times \frac{20\ MHz / 1}{100}$$

With an internal reference frequency of 20 MHz, the maximum data rate is 133.33 kbps. A rate of 100 kbps is below this maximum rate.

A third limitation on data rate is imposed by the serial interface rate and the sampling rate. Using Equation (3):

$$t_{FrequencyChange} = \frac{3}{20\ MHz} + \frac{10}{2\ MHz}$$

The time required to implement a frequency change is, therefore, 5.15 µs. Using this value in Equation (4):

$$Sample\ Rate_{max} = \frac{1}{5.15\ \mu s}$$

This provides a maximum allowed sample rate of 194.174 ksamples per second. The required sample rate is defined by the symbol rate and the number of discrete frequency steps required per symbol.

In the case of this MSK example, the symbol rate is equal to the bit rate and the required number of samples per symbol is only one. Therefore, one modulation data word is written to the synthesizer every 10 µs. This is an effective sampling rate of 100 ksamples per second, which is below the maximum sample rate calculated above.

Using Equation (5) to calculate the resulting minimum serial interface data rate:

$$Serial\ Rate_{min} = \frac{100\ ksamples \times 10\ Bits\ per\ Sample}{1 - \frac{3}{20\ MHz} \times 100\ ksamples}$$

The minimum serial interface data rate is, therefore, 1.015 Mbps, equal to a 1.015 MHz serial clock rate.

This meets the requirements of the problem statement (2 MHz). For each 10 µs symbol period, the microcontroller must deliver the 10 modulation data word bits and ensure the $\overline{CS}$ line is high for at least 3 internal reference frequency cycles (150 ns).

Although this serial clock rate is acceptable, some designers may want to reduce it further. The modulation data word length can be reduced if the deviation error is allowed to increase. This requires the use of the Modulation Data Magnitude Offset feature previously discussed. If the modulation magnitude bits (address 0x8, bits 7 to 4) are programmed to 4_{10}, then the modulation data word is multiplied by 2^4, or 16.

This implies that the modulation data word should be reduced by a factor of 16, to ±21 (±328/16). This effectively reduces the required modulation data word length to 6 bits (2^6 = 64) from 10. With these modulation data words (010101b and 101011b) the resulting modulation deviation is ±25635 Hz (+21 x 16 x 76.29 and –21 x 16 x 76.29), an error of 2.5 percent. The resulting serial clock rate is now only 609.14 kHz.

Another approach can be applied to reduce the modulation data word length to the minimum value of 2 bits. Again, this uses the Modulation Data Magnitude Offset feature. It also requires a modification to the internal reference frequency. The internal reference frequency must be chosen so that the desired deviation (25 kHz) is a binary multiple of the resolution step size. In other words, the resolution step size must be set so that it can be multiplied to 25 kHz by a binary factor of 2, 4, 8, 16 … 128, 256 ... 2048, or 4096 by use of the Modulation Data Magnitude Offset bits.

The most likely choice of Modulation Data Magnitude Offset for the example used here is 512 (resulting Modulation Data Magnitude Offset bits of 1001_2). The product of this value (2^9) with the resolution step size should yield 25 kHz. The required resolution step size is then 48.828125 Hz (25 kHz/512). This requires an internal reference frequency of 12.8 MHz (48.828125 Hz x 218).

With this configuration, the modulation data word is two bits long and uses two values. The first value, 01_2, specifies an offset of +25 kHz, which indicates a +1 data bit transmission. The second value, 11_2, specifies an offset of –25 kHz for a –1 data bit transmission.

Using a two-bit modulation data word length reduces the serial rate to a mere 203.045 kHz.

The modulation data word length is a design parameter that depends on available serial interface bandwidth. Multiple synthesizers or other system resources may share the serial interface. Reduction of the modulation data word length can help alleviate bus congestion, which may result in shared bus applications.

Conclusion

The example described in this Application Note demonstrates the simplicity that Direct Digital Modulation offers with the SKY72300, SKY72301, or SKY72302 synthesizers compared to existing design approaches.

Processing power required from the system processor is very low, no additional hardware components are required, and no production alignment procedures are needed. All of these benefits mean lower system cost, a simplified Bill of Materials, and improved reliability. At the same time, this allows software configurable modulation deviation and data rate selection.

This MSK example can be expanded to include other modulation schemes such as GMSK. Mathematical modeling tools (e.g., MathCADTM) can be used to determine the instantaneous frequencies generated by the modulation scheme. This information is then used to create a short look-up table of modulation data words required to “assemble” data symbols from the data bit stream.

In addition to data modulation schemes, conventional analog voice frequency FM can be generated by using an A/D converter between the microphone and the synthesizer serial interface.