APPLICATION NOTE

APN1011: A 5–6 GHz Switch Using Low-Cost Plastic Packaged PIN Diodes

Introduction

Short-range wireless LANs are being developed for use in the ISM frequency bands between 5.15 and 5.875 GHz. Using low-cost, plastic packaged, surface mount components, such as PIN diodes, is problematic in this frequency range because of package parasitics. In traditional designs, using low-cost packages like the SOT-23, coverage is limited to about 2.5 GHz. In this Application Note, a new design for an SPDT switch in the 5–6 GHz range will be described using PIN diodes in a low inductance SOT-23 package. The design has performance approaching 1 dB insertion loss and 20 dB isolation.

PIN Diode Switch Fundamentals

PIN diodes are widely used in switches at frequencies below 2.5 GHz. A typical design for a simple SPDT switch, covering a fixed bandwidth, consists of shunt connected PIN diodes each connected a quarter wavelength from the common input port, as shown in Figure 1. Using low-cost plastic packaged PIN diodes, the isolation of this circuit is limited by package inductance. The expression for attenuation based on the inductance, L, and resistance, R, of PIN diode is shown above. A PIN diode in a SC-79 package with typical inductance of 0.7 nH and PIN diode resistance of 1 Ω results in approximately 9 dB isolation, in this switch design at 5.8 GHz. This level of performance is not satisfactory.

This paper describes the design and performance of an SPDT switch covering 5–6 GHz using low-cost, commercially available PIN diodes in SOT-23 packages that use a low inductance internal lead configuration. The design is based on a Libra IV simulation.

$$ISO = 10 \log \left[1 + \frac{RZ_0 + Z_0^2/4}{R^2 + (\omega L)^2} \right] + 6 \text{ dB}$$

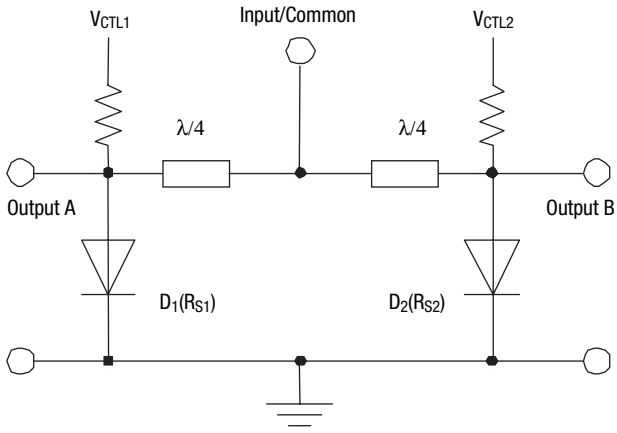

Figure 1. Typical SPDT Switch Design

The Libra IV Circuit Model

In the Libra IV model shown in Figure 2, the PIN diodes, X_1 and X_4 are shunt connected to the RF path. The PIN diodes X_1 and X_4 are designated to work complimentary. That is, when the PIN diode in one arm is forward biased (isolation or OFF state) the diode in the other arm is reverse biased (insertion loss or ON state). This operation is provided by defining X_1 bias voltage as V_{CTL}; therefore, the bias for X_2 is $V_{CTL2} = 3 - V_{CTL}$. Thus, switching V_{CTL} from 0–3 V, V_{CTL2} would toggle from 3–0 V synchronously. The function of the transmission lines T_{L6} + SRLC1 + T_{L7} and T_{L5} + SRLC2 + T_{L10} is to match the impedance of the forward and reverse-biased PIN diodes, X_1 and X_4 at the coupling point TEE_1, to the 50 Ω source. Since both RF branches (Port 2 and Port 3) are symmetrical, the input impedance at Port 1 should not change as the switch changes its state from ON/OFF to ON/OFF, or opposite.

The transmission lines T_{L1} and the DC decoupling capacitors SRLC4 and SRLC3 match the impedance of the ON diodes to the 50 Ω RF ports.

The decoupling capacitors SRLC1–SRLC4 are modeled as series RLC networks to account for both the parasitic inductance (L = 0.75 nH) and ohmic loss (R = 0.2 Ω) typical for 0402 ceramic capacitors.

Capacitors C_1, C_3, C_4, C_5, C_6, C_7, C_9, C_{10} and C_{11} are modeled as parasitic effects of component mounting pads on the PCB. Inductors L_1 and L_3 are modeled as the inductive effects of grounding VIA-holes and connecting lines.

DC biasing is provided through the 3 k resistors, R_1 and R_2, which are connected to the RF lines through transmission lines T_{L7} and T_{L9}.

The variable values of the circuit-like capacitances and transmission line lengths and widths were optimized to fit both minimum insertion loss and maximum isolation requirements in the band from 5–6 GHz.

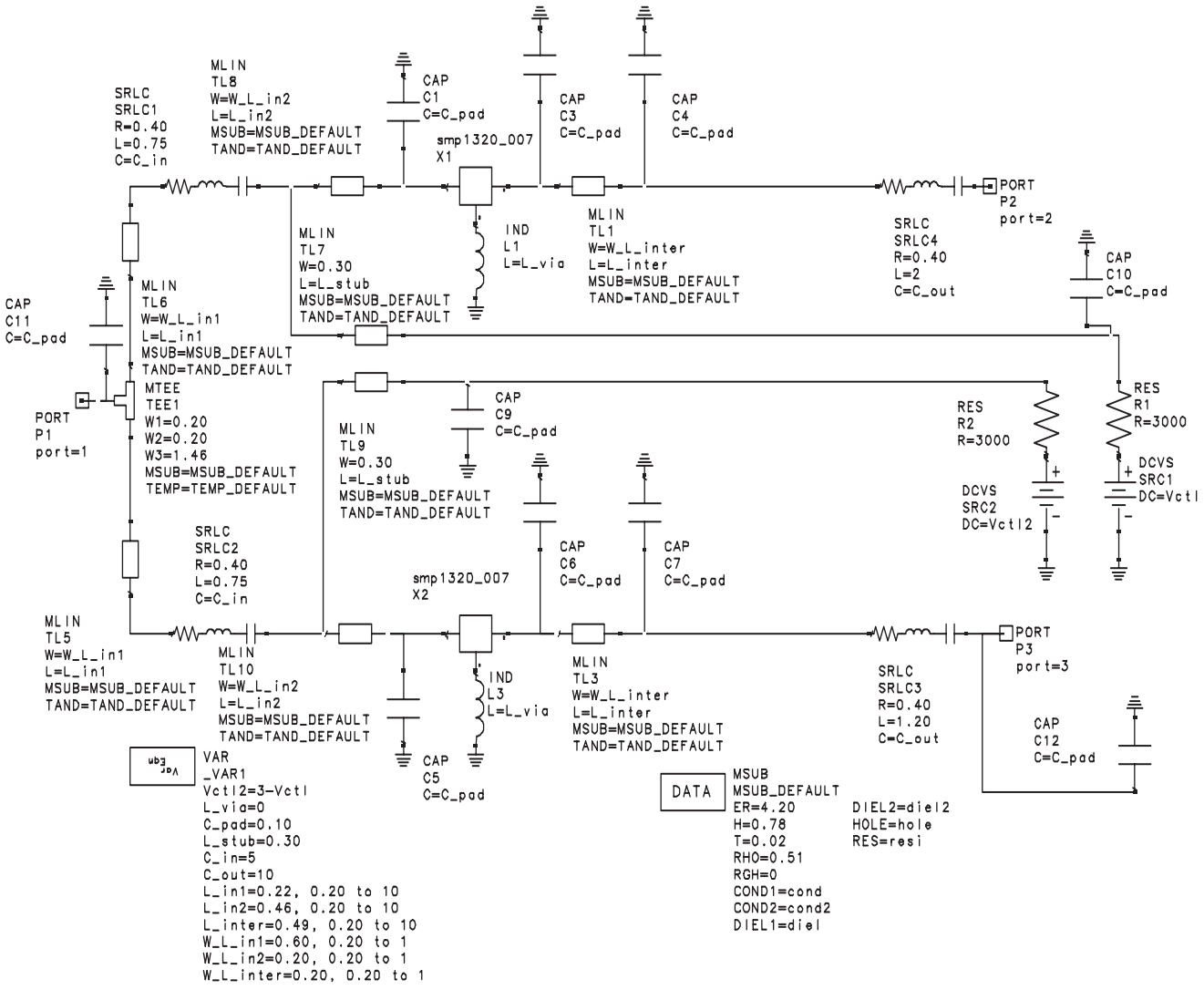

Figure 2. Libra Switch Model

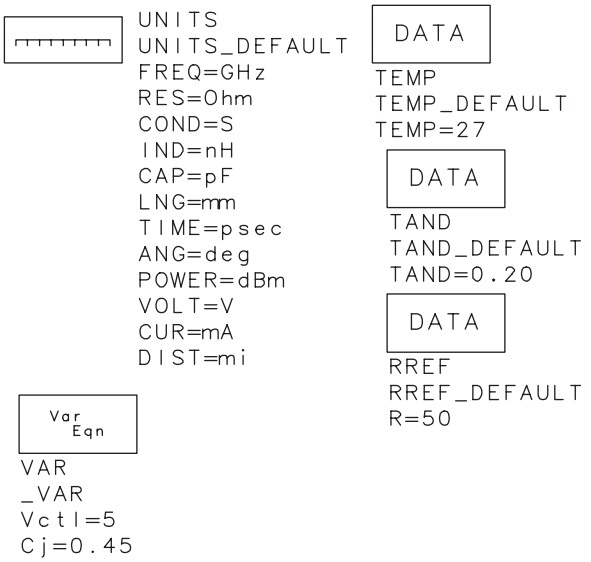

Figure 3. Default Bench Values

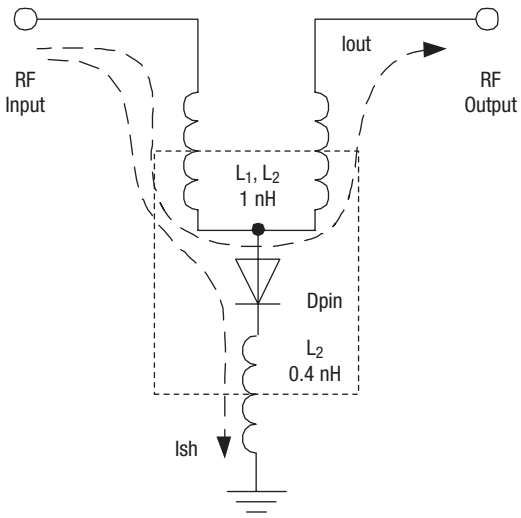

Figure 4. Low Inductance SOT-23

SMP1320 and SMP1304 SPICE Models

The SMP1304-007 and SMP1320-007 are silicon PIN diodes with I region thickness of 100 um and 8 um respectively and carrier lifetimes of 1.0 us and 0.4 us respectively. Both devices exhibit a wide range of resistance vs. current and are capable of operating with low distortion as a switching element. For the same RF resistance, the SMP1320 requires less DC current than SMP1304. However, at zero bias the SMP1304 has higher impedance.

The 007 low inductance package style for the SOT-23 was designed to minimize inductance for shunt connected diodes. To be effective, it must be inserted with each anode contact attached to either side of a gap in a microstrip trace, as shown in Figure 4. When the Dpin diode is OFF (no DC current) the diode is at high impedance and the current, Ish, is minimal. The RF input current primarily flows directly to the output, I_{OUT}. Parasitic inductances, L_1 and L_2, formed mostly by bonding wires and partially by the package leadframe, combine, resulting in about 2–2.5 nH total inductance on the I_{OUT} current path.

When the diode Dpin is ON, the forward bias condition, the shunt current Ish is high. The voltage drop between Dpin anode and the ground is mostly due to the small (0.4–0.5 nH) inductance of the lead and the PCB VIA-hole. This small shunt impedance causes the through current, I_{OUT}, to be relatively small. This allows the PIN diode in this package to provide useful attenuation at frequencies to beyond 6 GHz.

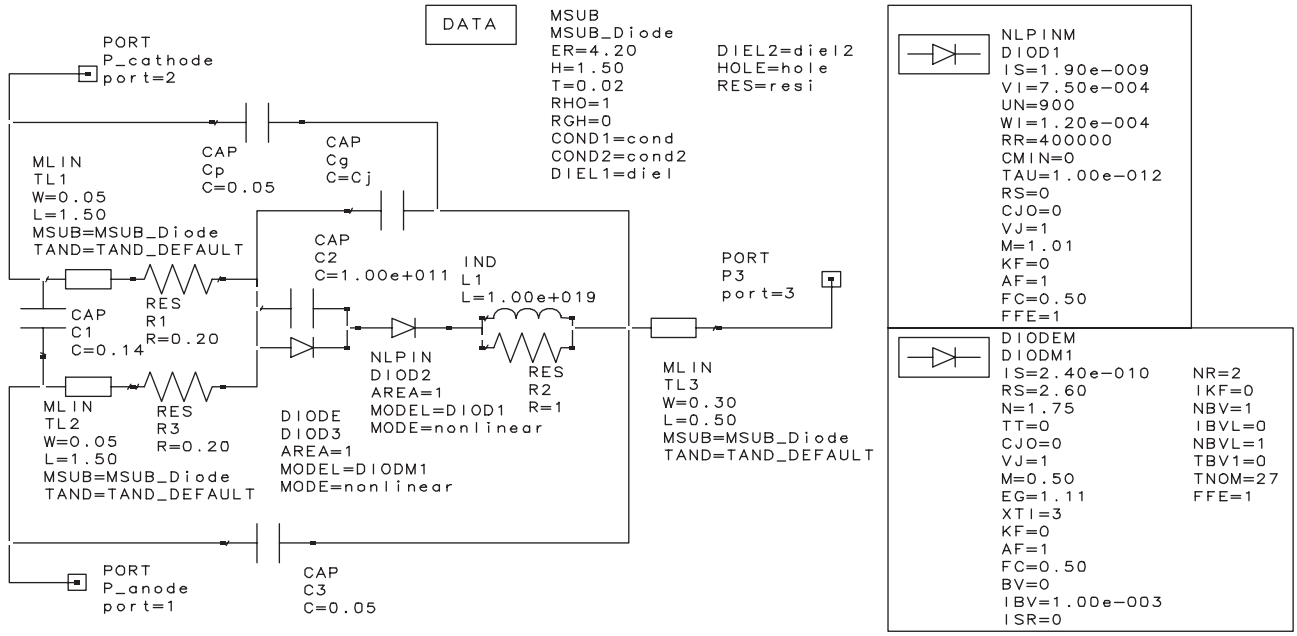

Figure 5. SMP1320-007 Small-Signal SPICE Model

SPICE models for the SMP1320-007 and SMP1304-007 PIN diodes defined for the Libra IV environment are shown in Figure 5 with a description of the parameters employed. In each model, two diodes were used fitting both the DC and the RF properties of each PIN diode. The PIN diode built-in model of Libra IV is used to model behavior of RF resistance vs. DC current, while the PN-junction diode model is used to model DC voltage-current characteristics. Both diodes are connected in series to ensure the same current flow with the PN-junction diode effectively RF shorted with capacitor C_2 set at 10^{11} pF. The portion of the RF resistance that reflects residual series resistance was modeled with $R_2 = 2.2\ \Omega$. This is in shunt with an ideal inductor, $L_1 = 10^{19}$ nH, to avoid affecting DC performance. Capacitors C_G, C_P and inductor L_2 reflect junction and package properties of SMP1320/1304-007 diodes.

The described model is a linear model that emulates the DC and RF properties of PIN diode. It is described in Reference 2.

For details on the fundamental properties of PIN diodes refer to Reference 1.

Tables 1 and 2 describe the model parameters for a silicon PIN diode and silicon PN diode. It shows default values appropriate for silicon diodes that may be used by the Libra IV simulator. Some of the values of PIN diode built-in model of Libra IV were not used. Those are marked “not used” in the tables.

Parameter	Description	Unit	Default SMP1320/1304
IS	Saturation current (not used)	A	1.9E-9
VI	I region forward bias voltage drop	V	7.5E-4
UN	Electron mobility cm**2/(V*S) (not used)	cm**2/(V*S)	900
WI	I region width (not used)	M	1.2E-4
RR	I region reverse bias resistance	Ω	4E5
C_{MIN}	P_{IN} punchthrough capacitance	F	0
TAU	Ambipolar lifetime within I region (not used)	S	1E-12
R_S	Series resistance	Ω	0
C_{J0}	Zero-bias junction capacitance	F	1.8E-15
V_J	Junction potential	V	1
M	Grading coefficient	-	1.01
KF	Flicker noise coefficient (not used)	-	0
AF	Flicker noise exponent (not used)	-	1
F_C	Coefficient for forward bias depletion capacitance (not used)	-	0.5
FFE	Flicker noise frequency exponent (not used)	-	1

Table 1. Silicon PIN Diode Values in Libra IV Assumed for SMP1320/1304 Models

Parameter	Description	Unit	Default SMP1320	Default SMP1304
IS	Saturation current	A	2.4E-10	2.2E-9
R_S	Series resistance	Ω	2.6	0.62
N	Emission coefficient (not used)	-	1.75	2.0
TT	Transit time (not used)	S	0	0
C_{JO}	Zero-bias junction capacitance (not used)	F	0	0
V_J	Junction potential (not used)	V	1	1
M	Grading coefficient (not used)	-	0.5	0.5
EG	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11	1.11
XTI	Saturation current temperature exponent (with EG, helps define the dependence of IS on temperature)	-	3	3
KF	Flicker noise coefficient (not used)	-	0	0
AF	Flicker noise exponent (not used)	-	1	1
F_C	Forward bias depletion capacitance coefficient (not used)	-	0.5	0.5
B_V	Reverse breakdown voltage (not used)	V	Infinity	Infinity
I_{BV}	Current at reverse breakdown voltage (not used)	A	1E-3	1E-3
ISR	Recombination current parameter (not used)	A	0	0
NR	Emission coefficient for ISR (not used)	-	2	2
IKF	High-injection knee current (not used)	A	Infinity	Infinity
NBV	Reverse breakdown Ideality factor (not used)	-	1	1
IBVL	Low Level reverse breakdown knee current (not used)	A	0	0
NBVL	Low Level reverse breakdown Ideality factor (not used)	-	1	1
TNOM	Nominal ambient remperature at which rhese model Parameters were derived	°C	27	27
FFE	Flicker noise frequency exponent (not used)		1	1

Table 2. Silicon PN Diode Values in Libra IV Assumed for SMP1320/1304 Models

Circuit Design and Layout

The circuit diagram for the switch is shown in Figure 6 and the PC board layout is shown in Figure 7. The bill of materials for the switch is shown in Table 3.

The PC board was made using 0.78 mm thick standard FR4 material. For convenience, the PC board also has a printed TRL calibration. A through-line should be prepared from a spare PCB by cutting it along the designated board cut mark followed by cleaning and polishing the interface surfaces. The RF terminations were shaped to fit the Wiltron 3680 Series Universal Test Fixture.

We do not recommend using SMA adapters because in this frequency range and board thickness a microstrip-to-SMA coaxial may significantly differ from 50 Ω. This may cause substantial measurement errors. The loss of the 10 mm long 50 Ω line on this circuit board was less than 0.2 dB.

The measurement data shown are two-port measurements with the third port loaded with a 50 Ω discrete resistor.

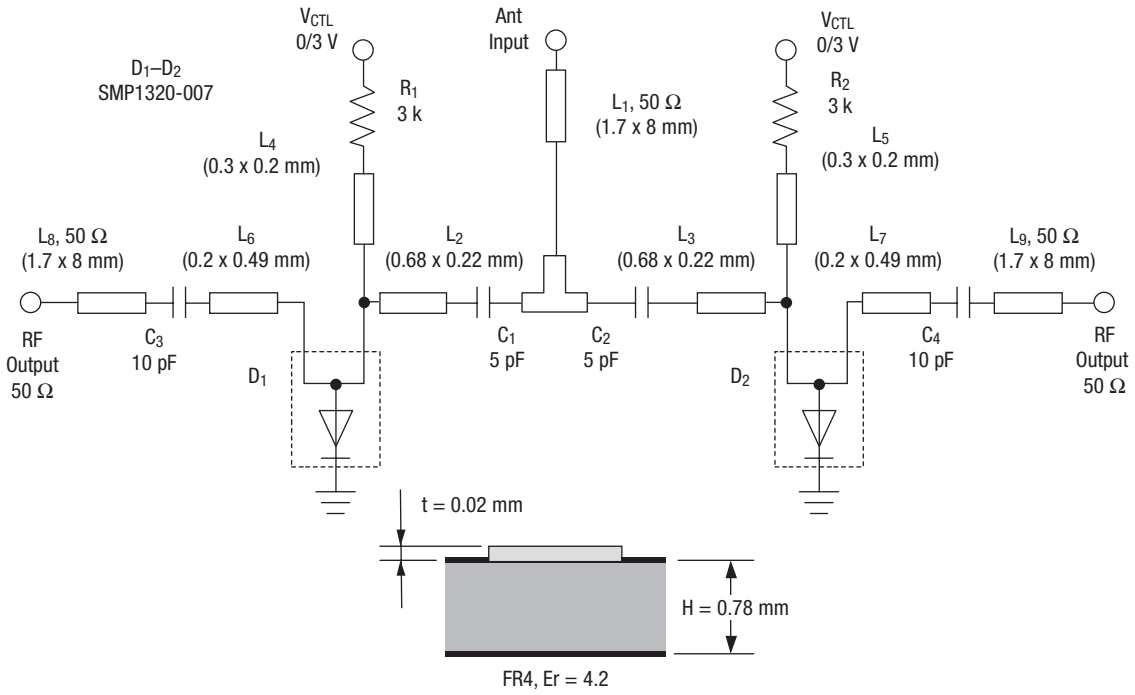

Figure 6. 5–6 GHz Switch Circuit Diagram

Designator	Value	Part Number	Footprint	Manufacturer
C_1	5 p	CM05CG5R0K10AB	0402	AVX/KYOCERA
C_2	5 p	CM05CG5R0K10AB	0402	AVX/KYOCERA
C_3	10 p	CM05CG100K10AB	0402	AVX/KYOCERA
C_4	10 p	CM05CG100K10AB	0402	AVX/KYOCERA
R_1	3 k	CR05-302J-T	0402	AVX
R_2	100	CR05-302J-T	0402	AVX
D_1	SMP1320-007	SMP1320-007	SOT-23	Solutions Solutions
D_2	SMP1320-007	SMP1320-007	SOT-23	Solutions Solutions
L_1	1.7 x 8 mm	MSL, 50 Ω	1.7 x 8 mm	(printed on PCB)
L_2	0.68 x 0.22 mm	MSL	0.68 x 0.22 mm	(printed on PCB)
L_3	0.68 x 0.22 mm	MSL	0.68 x 0.22 mm	(printed on PCB)
L_4	0.3 x 0.2 mm	MSL	0.3 x 0.2 mm	(printed on PCB)
L_5	0.3 x 0.2 mm	MSL	0.3 x 0.2 mm	(printed on PCB)
L_6	0.2 x 0.49 mm	MSL	0.2 x 0.49 mm	(printed on PCB)
L_7	0.2 x 0.49 mm	MSL	0.2 x 0.49 mm	(printed on PCB)
L_8	1.7 x 8 mm	MSL, 50 Ω	1.7 x 8 mm	(printed on PCB)
L_9	1.7 x 8 mm			(printed on PCB)

Table 3. Bill of Materials for the 5–6 GHz Switch

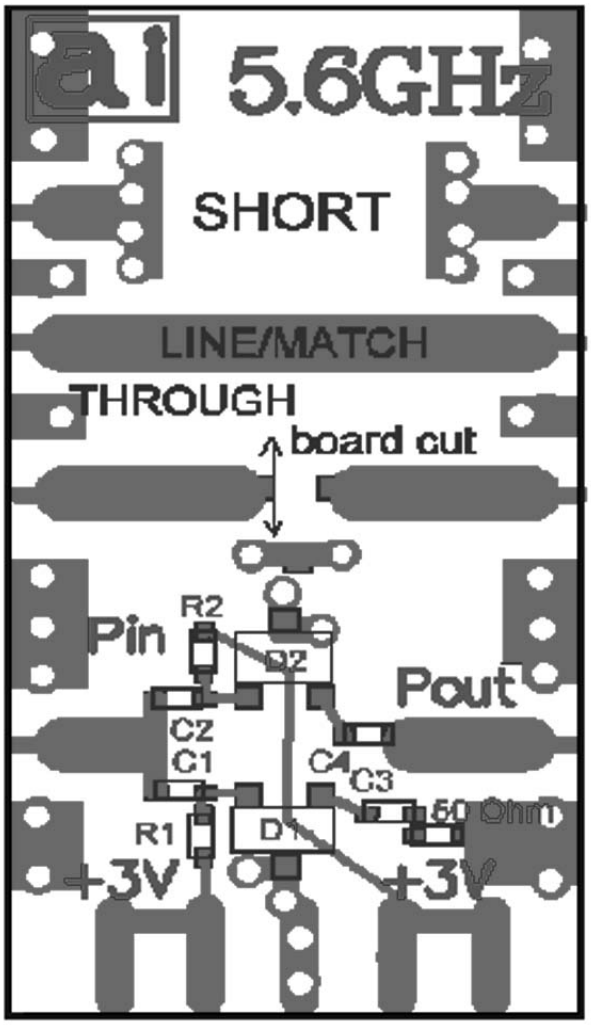

Figure 7. PCB Layout

Switch Performance

Measurement results using the SMP1320-007 are shown in Figure 8 for both ON and OFF states. The dashed line shows that an improvement of at least 0.5 dB in the insertion loss was obtained when the OFF state diode was reverse biased to 5 V from zero bias. This improvement is due to the reduction in junction capacitance for the SMP1320 with increased reverse bias. The forward bias current was less than 2 mA. Our measurements showed approximately 1 dB insertion loss and 15 dB isolation achievable for the SMP1320-007 with 5 V negative bias over the 5–6 GHz frequency range.

Figure 9 shows the simulated switch performance using the SMP1320-007. The PIN diode model used was not able to model capacitance vs. voltage. It was simulated, however, by changing the capacitance value from 0.45 pF to 0.35 pF as shown.

Some of the differences of the measured curves vs. simulation may be attributed to imperfections of the calibration standards, the switch model and/or the components used. For example, dimensionless lumped models were used for the passive elements; at these frequencies the effect of a physical length of even 1 mm may be significant.

The multiple sharp peaks in the measured insertion loss graphs are probably due to imperfections of the calibration standards. Our estimate for measurement accuracy is ±0.25 dB, which is about the size of the peaks shown in the graphs. The reason for this large error is probably the inconsistency of the FR4 material and the standard PCB printing process used, which may have caused impedance deviations in the calibration standards at these frequencies.

Switch performance with the SMP1304-007 diode is shown in Figure 10. This PIN diode, by virtue of its thicker I region width, displays no measured change in capacitance or loss with reverse bias. Because it has about three times higher resistance than the SMP1320-007, at the same forward current, the forward control voltage was raised to 15 V. Both insertion loss and isolation show improvement in the range between 5.5–6 GHz, with insertion loss of about 1 dB and isolation slightly better than 20 dB.

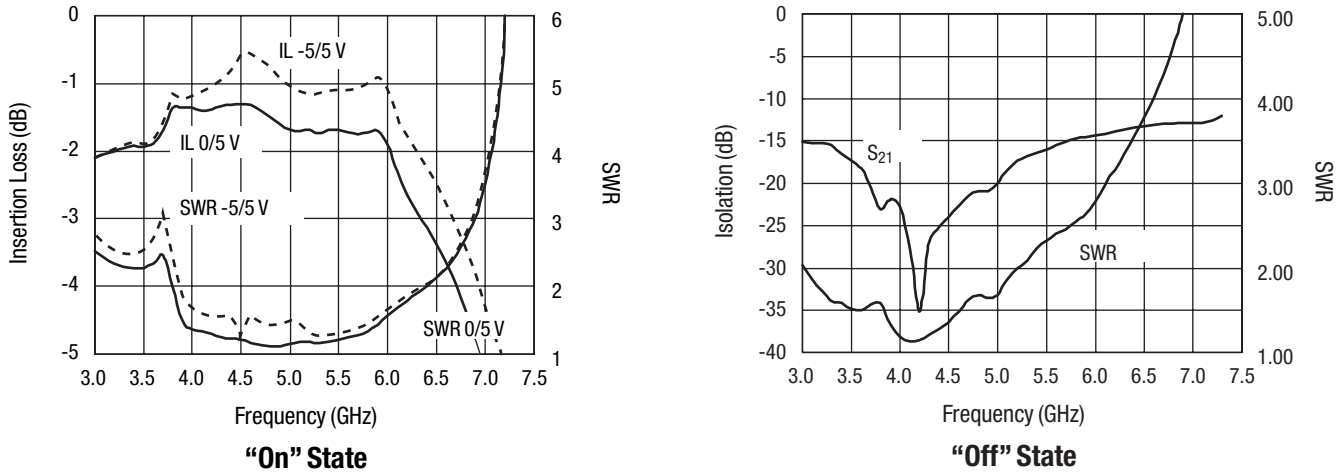

Figure 8. The measurement results for the SMP1320-007

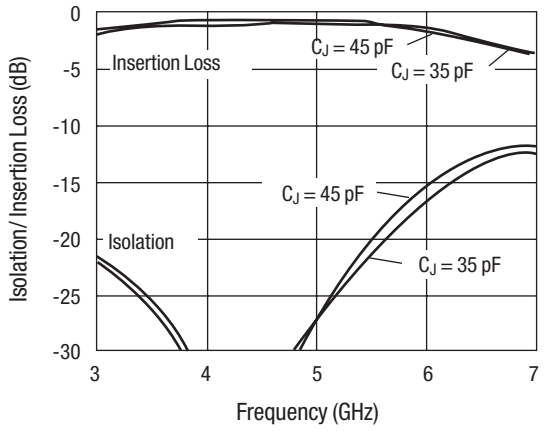

Figure 9. The simulation results for SMP1320-007

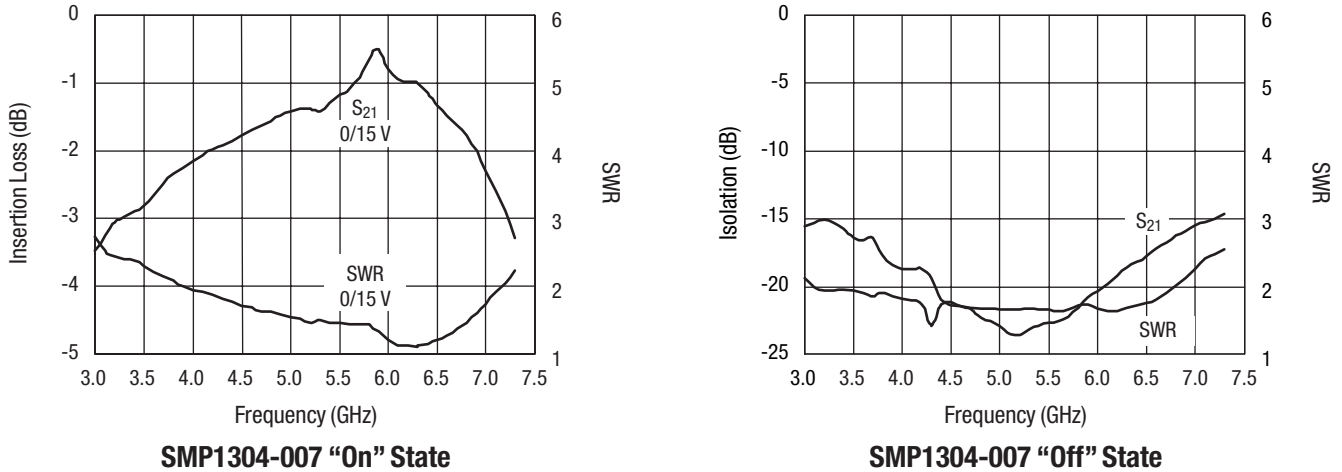

Figure 10. The measurement results for SMP1304-007

References

1. Gerald Hiller, “Design with PIN Diodes,” Applications Note, Skyworks Solutions, Inc.
2. J. Walston, “Spice Circuit Yields Recipe for PIN Diode,” Microwaves and RF, Nov. 1992.
3. Gerald Hiller, “Predict Intercept Points in PIN Diode Switches,” Microwaves & RF, Dec. 1985.
4. Robert Caverly and Gerald Hiller, “Distortion in PIN Diode Control Circuits,” IEEE Trans. Microwave Theory Tech., May 1987.
5. Gerald Hiller and Peter Shveshkeyev, “A Wideband General Purpose PIN Diode Attenuator,” Applications Note, Skyworks Solutions, Inc., 1999.

List of Available Documents

1. The 5.8 GHz switch simulation project files for Libra IV.
2. The 5.8 GHz switch PCB Gerber photo-plot files.