APPLICATION NOTE

APN1015: A Dual-Band Switchable IF VCO for GSM/PCS Handsets

Introduction

Many of today's handset cellular telephones are multifunctional, multiband units. They are complex RF systems with frequency plans requiring multiple RF sources. To accomplish this, the number of VCOs can be increased, however this is expensive and requires more PCB area. This approach strongly contradicts current market trends. A straightforward solution proposed in this application note is using switchable (multiband) VCOs.

Skyworks application note APN1007, *Switchable Dual-Band 170/470 MHz VCO for Handset Cellular Applications*, discusses a switchable Colpitts VCO design switching between the 170 MHz and 420 MHz range. Described here is a solution for higher frequency range switching, 450/640 MHz, using a DC Cascode Colpitts configuration for the VCO. This design is optimized for the lowest phase noise meeting GSM/PCS handset requirements.

The Colpitts VCO Fundamentals

Fundamental Colpitts VCO operation is illustrated in Figures 1a and 1b. Figure 1a shows the Colpitts VCO circuit as it is usually implemented. In Figure 1b, the same circuit is shown as a common emitter amplifier with parallel feedback. The transistor junction and package capacitors C_{EB}, C_{CB} and C_{CE} are separated from the rest of the transistor parasitic components to demonstrate their direct effect on the VCO tank circuit.

In a real low noise VCO circuit, the capacitor, C_{VAR}, may have a more complicated structure including series and parallel connected discrete capacitors used to set required oscillation frequency and tuning sensitivity. The parallel connection of resonator inductor, L_{RES}, and varactor capacitive branch, C_{VAR} , constitutes a parallel resonator (or simply resonator). A fundamental property of the parallel resonator in a Colpitts VCO implementation is that it always shows inductive impedance at the oscillation frequency. This means that its parallel resonant frequency is always above the oscillation frequency.

Loss in the resonator increases as the frequency approaches resonance in the feedback loop, acting as a stop-band filter at resonance. Thus, the nearer the oscillation frequency to parallel resonance, the more loss incurred in the feedback path. However, since more reactive energy is stored in the resonator nearer to the resonance frequency, higher loaded Q (Q_L) is achieved. Obviously, low loss resonators, such as crystals or dielectric resonators, allow oscillation buildup closer to parallel resonance with much lower loss compared to microstrip or discrete component-based resonators.

The proximity of the parallel resonant frequency to the oscillation frequency is established by the value of capacitor, C_{SER}. If the capacitance of C_{SER} were reduced, then the parallel resonator would be more inductive to compensate for the increased capacitive reactance. This means that the oscillation frequency should move closer to the parallel resonance and would result in higher Q_L and higher feedback losses.

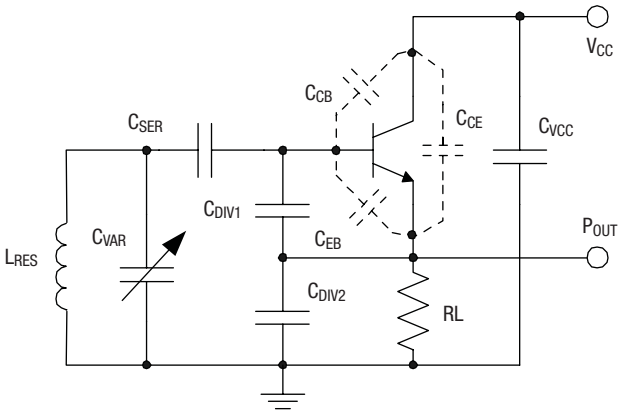

Figure 1a. Basic Colpitts VCO Configuration

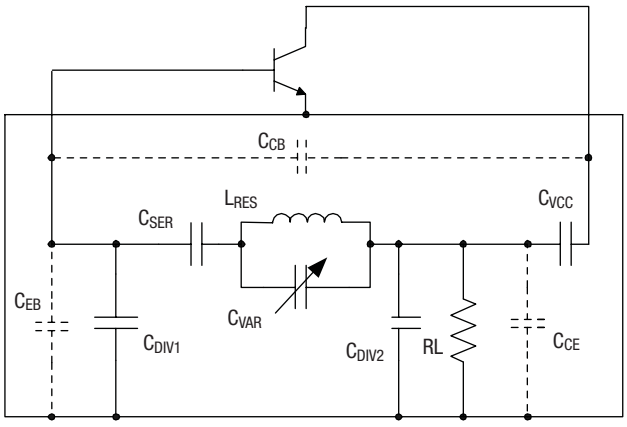

Figure 1b. Common Emitter View of the Colpitts VCO

The Leeson equation, establishing connection between tank circuit Q_L and its losses, states:

$$\xi(f_m) = \frac{FkT}{2P}\left(1 + \frac{f^2}{4Q_L^2 f_m^2}\right)$$

Where F is the large signal noise figure of the amplifier shown in Figure 1b, P is the loop or feedback power (the one which measured at the input of the transistor), and Q_L is loaded Q.

These three parameters have significant consequences for phase noise in a low noise RF VCO. In designing a low noise VCO, we need to define the conditions for minimum F and maximum P and Q_L. The above discussion shows that the loop power and Q_L are contradictory parameters. That is, an increase of Q_L leads to more losses in the feedback path resulting in lower loop power. The optimum conditions for noise also contradict maximum loop power, and largely depend on transistor choice. Usually the best noise is achieved with high gain transistors with maximum gain coinciding with minimum noise at the large signal condition. Because no such specifications are currently available for industry-standard transistors, we can base our transistor choice only on experience.

A Switchable Resonator VCO Circuit

Switchable resonator VCO designs are shown in Figures 2a and 2b. In the switchable resonator concept, two or more separate resonators, tuned and optimized according frequency bands, are activated (switched) by low resistance PIN-diodes (D_3 and D_4). The advantage of switching the entire resonator rather than switching an element within the resonator (capacitor or inductor) is that the control component (PIN diode) is not placed in the resonator current path. That way it exercises control over a small reactance portion of the overall tank circuit. This has significant impact on VCO performance, especially if more than 10% of the switching gap (the difference between designated frequency bands) is required.

To understand the impact of switching on the resonator losses, consider the following example. Assume switching between 0.47 and 0.62 GHz bands using these two concepts. In the intra-resonator-switching scheme in Figure 3a, the capacitance changes from 10 pF to 5.8 pF. In this case, 4.2 pF was added to jump to the lower frequency band. Alternately, in the inter-resonator switching scheme, 2 pF was added to the switching path. Simple analysis shows that the current flowing through the switching component in the intraresonator scheme may be more than double. This results in more than 6 dB additional loss in the lower band compared to the interresonator concept, which may be enough to prevent any oscillation. Even if oscillation could be sustained due to the excess of gain in the oscillator's active portion, there is still the problem of balancing loaded Q and the feedback loop power to optimize the phase noise performance.

Other problems with the intraresonator switching scheme include the lack of flexibility in providing optimum tuning in both frequency bands and extra noise modulation. The PIN diode control current comes from the same source that feeds the rest of the handset circuitry. This current may be carrying low-frequency noise that may not be filterable. Even though these noise fluctuations of DC current are small and relatively fast, the PIN diode is still a semiconductor device with inevitable nonlinear and/or parametric consequences that may result in excess modulation noise.

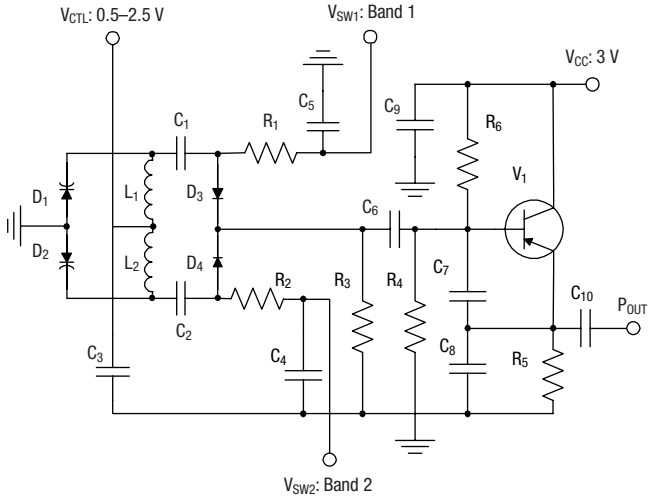

Figure 2a. Switchable Resonator VCO with Simplified Resonator Design

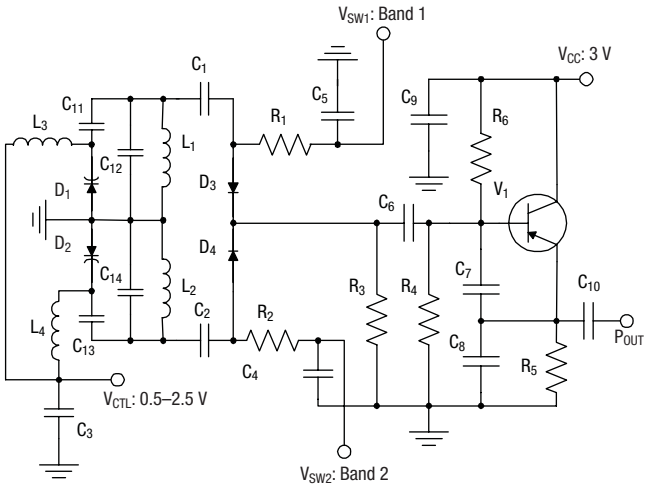

Figure 2b. Switchable Resonator VCO with High-Performance Resonator Design

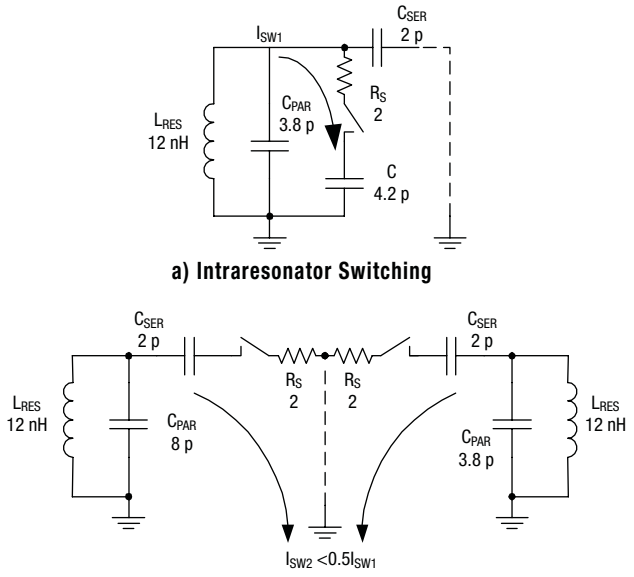

Figure 3. VCO Band Switching Concepts

The two circuits shown in Figure 2 differ only in resonator design. Figure 2a shows a simplified resonator design, minimizing the component count, thus minimizing cost and space. Resonator inductors L_1 and L_2 are also used as varactor biasing chokes.

However, this circuit has some drawbacks. One is a lack of design flexibility caused by discrete choices of available varactors (D_1 and D_2) and inductors (L_1 and L_2) values. Capacitors may be added in parallel to the varactors to improve design flexibility, but this may degrade the tuning sensitivity. Tuning linearity may also suffer in such a circuit because there is no capacitor in series with the varactor.

Alternately, the resonator in Figure 2b has more components, which allows more design flexibility and better tuning linearity, but the component count is higher. The effect of capacitor, C_{SER2}, in series with the varactor is demonstrated in Figure 4. The relative tuning sensitivity is defined as:

$$K_f = \frac{1}{f}\frac{\partial f}{\partial V_V};$$

$$K_f = C_{J0}\ \frac{C_S^2 / K_{DV}}{C^2_{VAR}\ (C_S + C_{PAR}) + C_{VAR}\ C_S(2C_{PAR} + C_S) + C^2_S C_{PAR}};$$

$$K_{DV} = \frac{2V_J}{M}\left(1 + \frac{V_{VAR}}{V_J}\right)^{M+1}$$

$$K_{fVAR} = \frac{K_{f0.5V}\ K_{f2.5V}}{K_{f1.5V}}\%$$

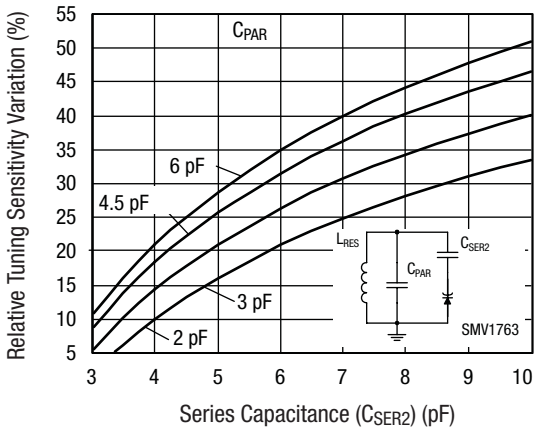

Figure 4. Relative Tuning Sensitivity (K_f) Variation in the Range of 0.5–2.5V for SMV1763-079 as a Function of C_{SER2} and C_{PAR}

Where V_{VAR} is varactor DC bias in the middle of the tuning range,C_{SER2} and C_{PAR} are capacitors in series with the varactor (C_{11} and C_{13} in Figure 2b) and resonator parallel capacitors (C_{12} and C_{14} in Figure 2b), and C_{J0}, V_J, M are parameters describing varactor capacitance [1]: See SMV1763-079 SPICE model section.

According to this equation, relative tuning sensitivity variation is defined as the percent variation of tuning sensitivity per volt in the tuning range from 0.5–2.5 V — typical for most battery handset applications. The graph shows that higher values of C_{SER2} cause larger tuning sensitivity variations. Consequently, high variation of tuning sensitivity would occur across the tuning range without C_{SER2} in Figure 2a.

VCO Model Description

In the circuit in Figure 5 transistors, X_3 and X_9 are connected in DC Cascode sharing the base biasing network consisting of R_1 (R_{DIV2}), R_4 (R_{DIV1}), and R_7 (R_{DIV3}). The bias resistor values were selected to evenly distribute DC voltages between X_3 and X_9. Resistor R_5 (RL) was chosen as low as 100 Ω to minimize the DC voltage drop for the specified 8 mA DC current. At RF frequencies, X_9 works as a common emitter amplifier with the emitter grounded through capacitor SRLC1. The oscillator stage output is fed to the buffer transistor through coupling capacitor C_{17} (C_{CPL}).

The output circuit of the buffer stage consists of discrete inductor, L_4, modeled with parallel capacitor, C_5 (0.38 pF), and output capacitor C_1 (C_{OUT}). For flatter power response over the specified 450/640 MHz range, capacitor SLC2 (for values less than 2 pF), in parallel with inductor L_4 (in Figure 5), may be used for fine trimming.

The dual-band switchable resonator circuit in Figure 6 consists of two identical parts (low band on the left, and high band on the right). The PIN diodes were modeled as parallel RC networks PRC1 and PRC2, with switching resistors, R_{SW_L} and R_{SW_H}, in the low band and high band branches respectively.

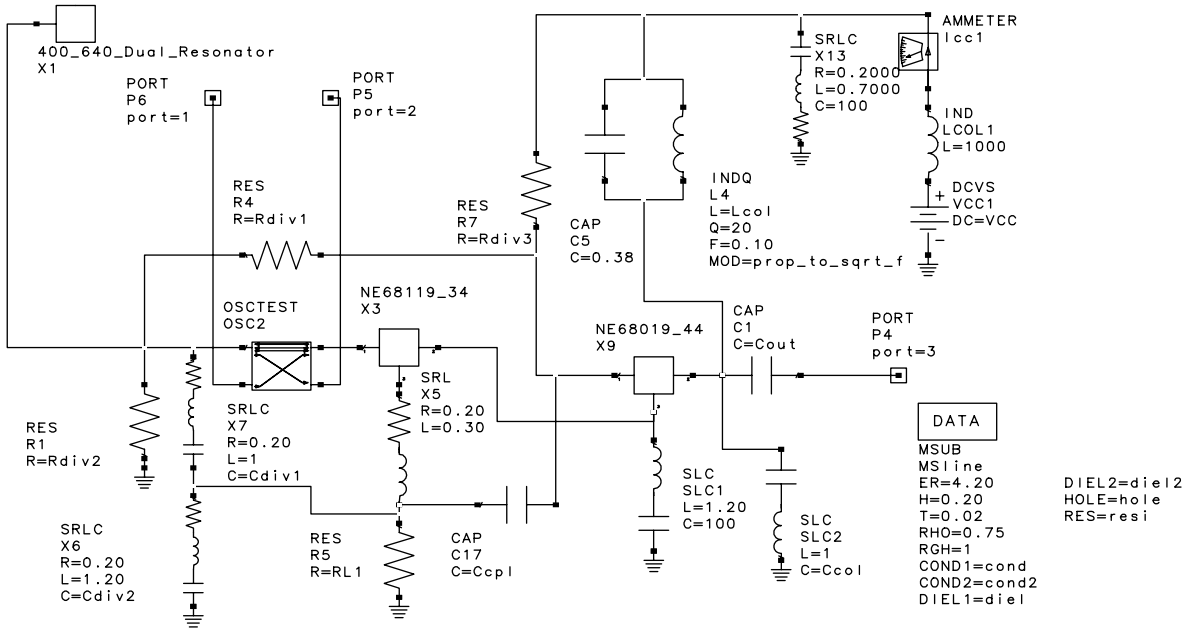

Figure 5. Open Loop Analysis VCO Schematic Bench

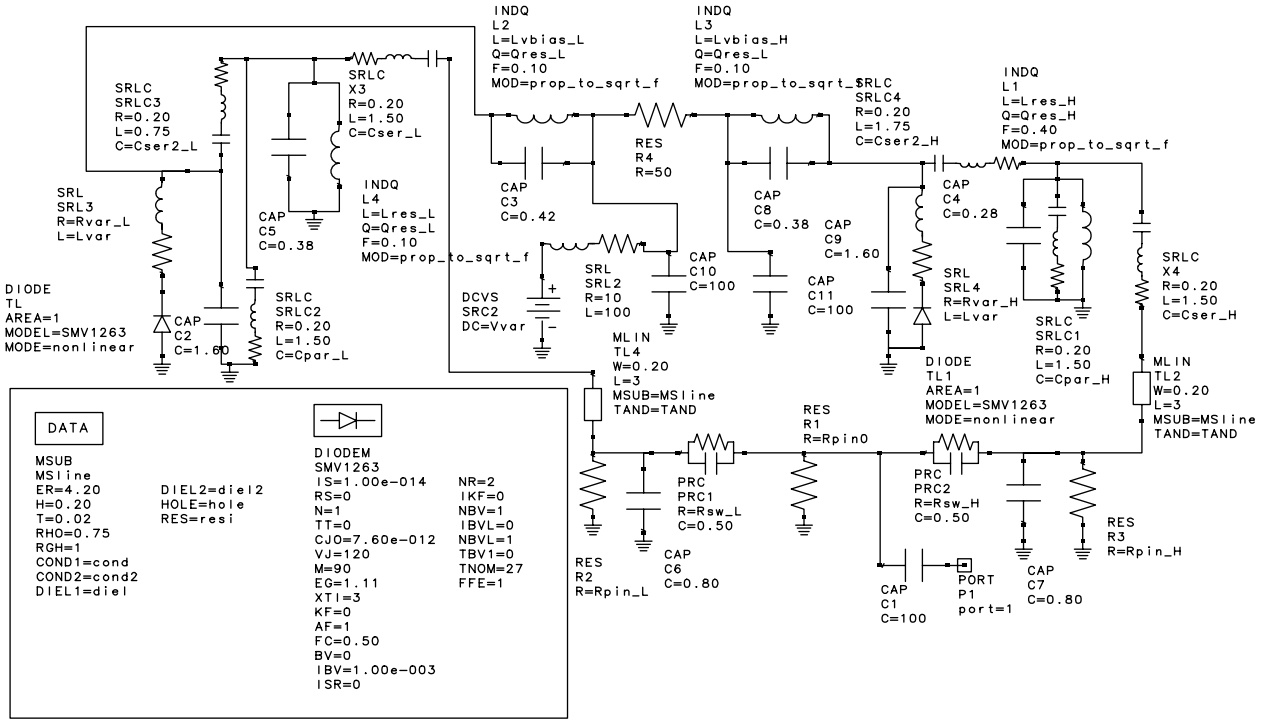

Figure 6. Dual-Band Resonator Schematic Bench

The appropriate biasing resistors, R_1, R_2, and R_3, are shown as shunt elements to ground. The truth table showing the values of R_{SW_L} and R_{SW_H} for the appropriate low/high switching is shown below:

R_{SW_L}	R_{SW_H}	State
3 Ω	3000 Ω	Low band
3000 Ω	3 Ω	High band

Resonator inductors, L_1 and L_4, are modeled as inductance losses with parallel capacitors, C_4 and C_5 respectfully. The resonator's parallel capacitors are presented as series equivalent models, SRLC1 and SRLC2, each with 1.5 nH inductance and 0.2 Ω series resistance. Other discrete capacitors are modeled with similar series SRLC networks. The different inductor values were selected based on the individual RF path layout.

Varactor SMV1763-079, used in this design, is described by the PN-junction diode SPICE model described in the next section.

The variable values used in the circuit are given in the Variable Equation module of the Default Bench shown in Figure 7. The Test Bench is shown in Figure 8. For open loop analysis we use the OSCTEST component supplied in the Libra IV library. This component allows us to observe the open loop VCO feedback gain as a function of frequency and power (in the loop) preserving feedback loading integrity. This is the way the VCO would see it when the feedback loop is closed. (Refer to Libra IV manual for further details of OSCTEST operation).

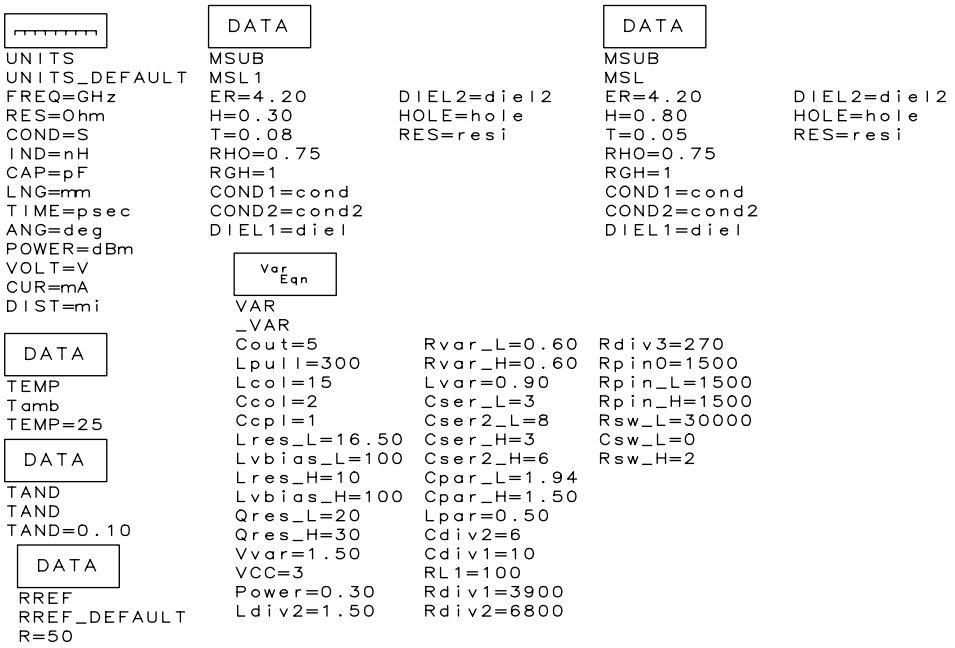

Figure 7. VCO Default Bench

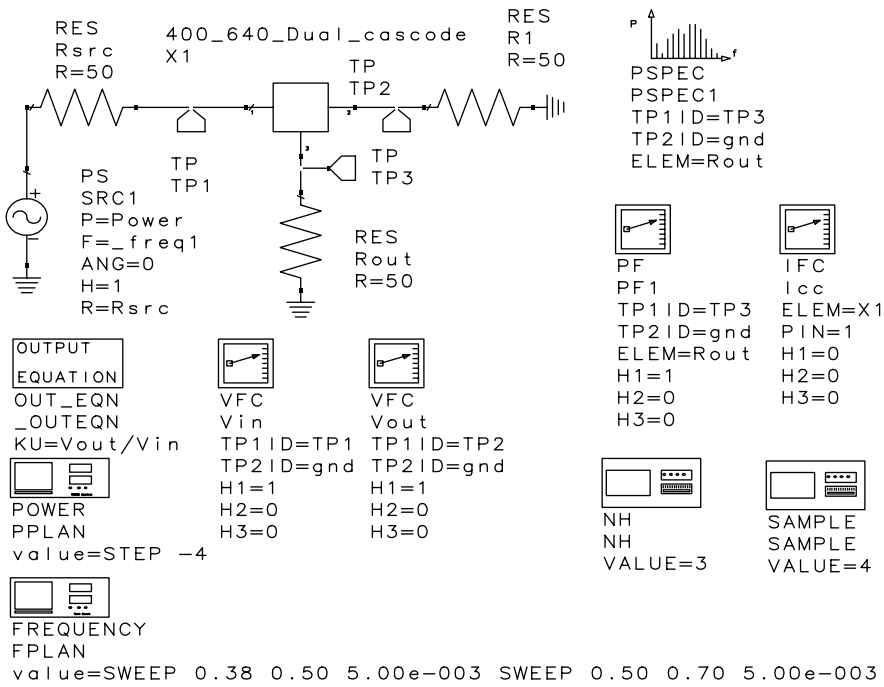

Figure 8. VCO Test Bench

SMV1763-079 SPICE Model

SMV1763-079 is a low series resistance, hyperabrupt varactor diode. It has the industry's smallest plastic package SC-79 with a plastic body size of 47 x 31 x 24 mils (the total length with leads is 62 mils).

The SPICE model for the SMV1763-079 varactor diode, defined for the Libra IV environment, is shown in Figure 9 with a description of the parameters employed.

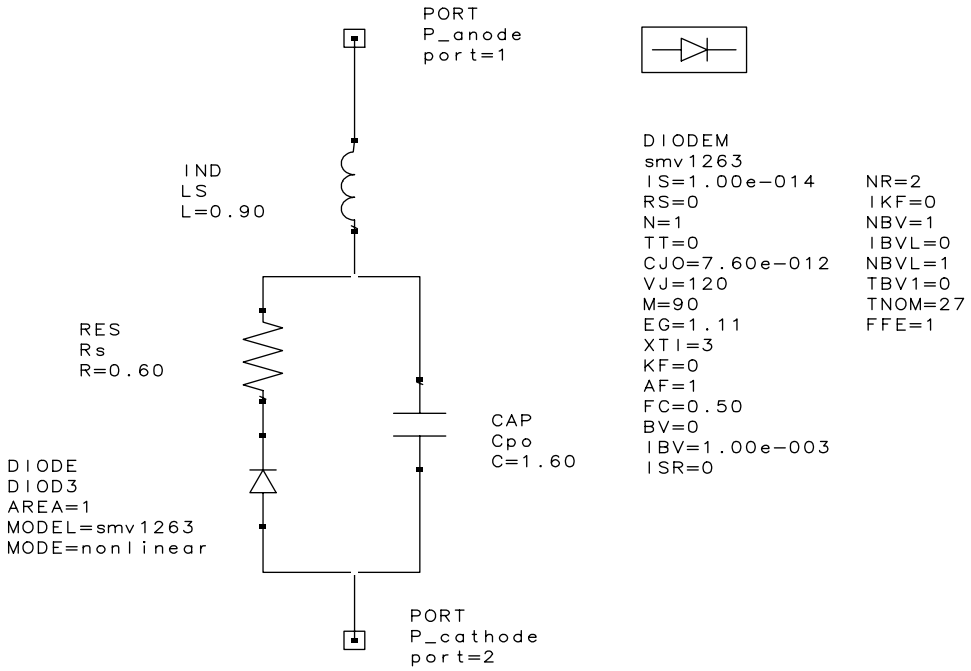

Figure 9. SMV1763-079 SPICE Model for Libra IV

Table 1 describes the model parameters. It shows the appropriate default values for silicon varactor diodes that may be used by the Libra IV simulator.

According to the SPICE model the varactor capacitance, C_V, is a function of the applied reverse DC voltage, V_R, and may be expressed as follows:

$$C_V = \frac{C_{J0}}{\left(1 + \frac{V_R}{V_J}\right)^M} + C_P$$

This equation is a mathematical expression of the capacitor characteristic. The model is most accurate for abrupt junction varactors (like the SMV1408). However, for hyperabrupt junction varactors the model is less accurate because the coefficients are dependent on the applied voltage. To make the above equation work better for hyperabrupt junction varactors, the coefficients were optimized for the best capacitance vs. voltage fit. These simulated coefficients may not have physical meaning.

Note that in the Libra model, C_P, is given in picoFarads, while C_{G0} is given in Farads to comply with the default unit system used in Libra.

Parameter	Description	Unit	Default
IS	Saturation current (with N, determine the DC characteristics of the diode)	A	1e-14
R_S	Series resistance	Ω	0
N	Emission coefficient (with IS, determines the DC characteristics of the diode)	-	1
TT	Transit time	S	0
C_{J0}	Zero-bias junction capacitance (with V_J and M define nonlinear junction capacitance of the diode)	F	0
V_J	Junction potential (with V_J and M define nonlinear junction capacitance of the diode)	V	1
M	Grading coefficient (with V_J and M define nonlinear junction capacitance of the diode)	-	0.5
EG	Energy gap (with XTI, helps define the dependence of IS on temperature)	EV	1.11
XTI	Saturation current temperature exponent (with EG, helps define the dependence of IS on temperature)	-	3
KF	Flicker noise coefficient	-	0
AF	Flicker noise exponent	-	1
FC	Forward-bias depletion capacitance coefficient	-	0.5
B_V	Reverse breakdown voltage	V	Infinity
I_{BV}	Current at reverse breakdown voltage	A	1e-3
ISR	Recombination current parameter	A	0
NR	Emission coefficient for ISR	-	2
IKF	High injection knee current	A	Infinity
NBV	Reverse breakdown ideality factor	-	1
IBVL	Low-level reverse breakdown knee current	A	0
NBVL	Low-level reverse breakdown ideality factor	-	1
T_{NOM}	Nominal ambient temperature at which these model parameters were derived	°C	27
FFE	Flicker noise frequency exponent	-	1

Table 1. Silicon Diode Default Values in Libra IV

Part Number	C_{J0} (pF)	M	V_J (V)	C_P (pF)	R_S (Ω)	L_S (nH)
SMV1763-079	8.87	2.7	4.3	0.1	0.5	0.9

Table 2. SPICE Parameters for SMV1763-079

VCO Design, Materials and Layout

The VCO schematic diagram is shown in Figure 10. The circuit is powered from a 3 V voltage source. The I_{CC} current was set at approximately 8 mA. The RF output signal is coupled from the VCO through capacitor C_{18} (5 pF). Band selection is accomplished by forward biasing either of the PIN diodes D_3 or D_4. Bias current is set by resistors R_2, R_3 and R_4. In the "ON" state, the PIN diodes (SMP1320-079) have about 2 Ω RF resistance with 1 mA control current.

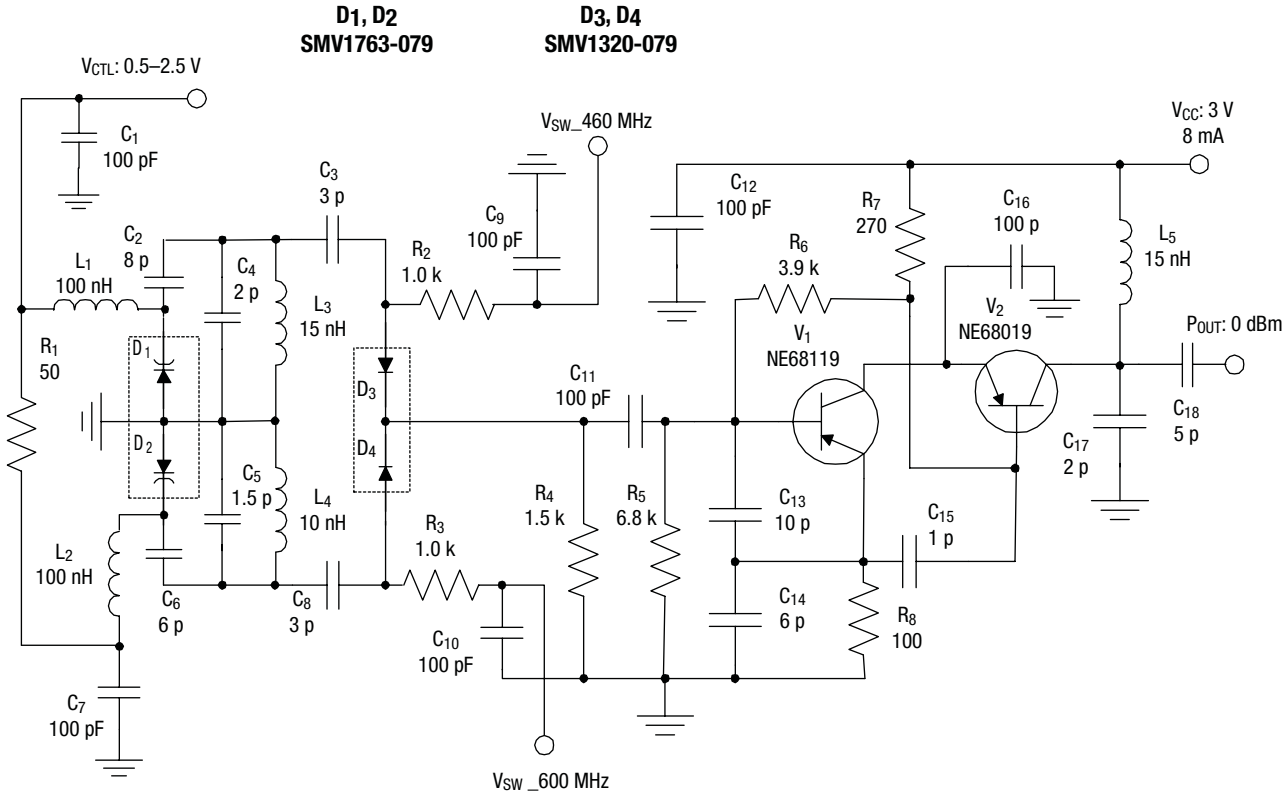

Figure 10. The Switchable VCO Circuit Diagram

The PCB layout is shown in Figure 11. The board was made of standard, 30 mil thick, FR4 material.

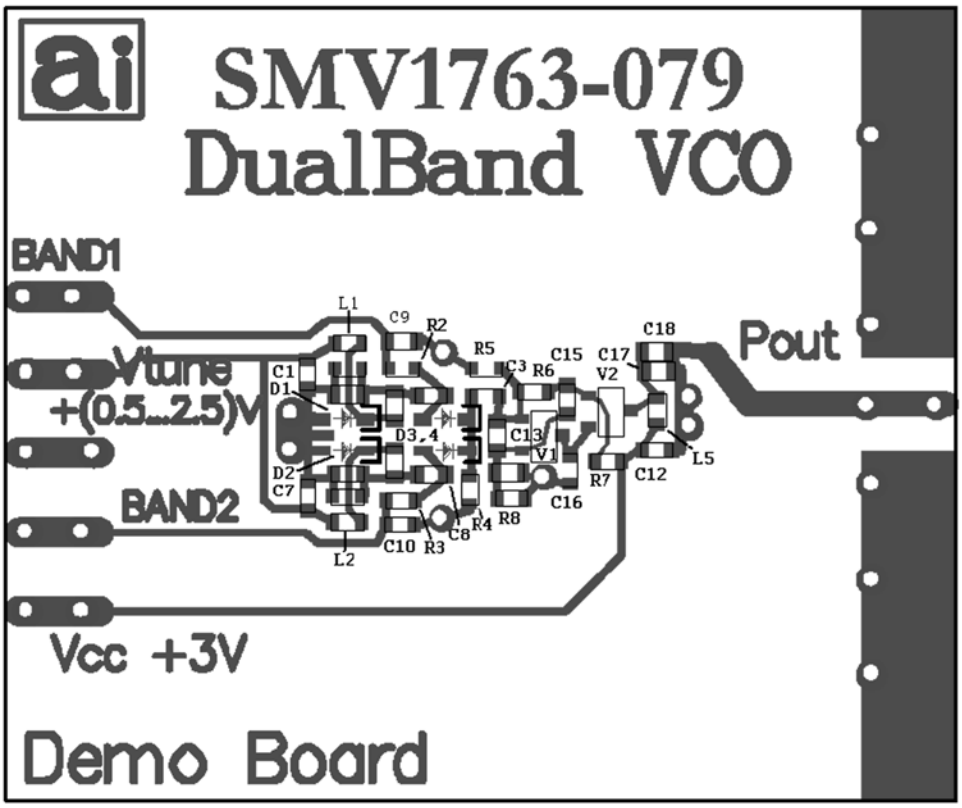

Figure 11. PCB Layout

The bill of materials used is given in the Table 3.

Designator	Value	Part Number	Footprint	Manufacturer
C_1	100 p	0402AU101KAT	0402	AVX
C_2	8 p	0402AU8R0KAT	0402	AVX
C_3	3 p	0402AU3R0KAT	0402	AVX
C_4	2 p	0402AU2R0KAT	0402	AVX
C_5	1.5 p	0402AU1R5KAT	0402	AVX
C_6	6 p	0402AU6R0KAT	0402	AVX
C_7	100 p	0402AU101KAT	0402	AVX
C_8	3 p	0402AU3R0KAT	0402	AVX
C_9	100 p	0402AU101KAT	0402	AVX
C_{10}	100 p	0402AU101KAT	0402	AVX
C_{11}	100 p	0402AU101KAT	0402	AVX
C_{12}	100 p	0402AU101KAT	0402	AVX
C_{13}	10 p	0402AU100KAT	0402	AVX
C_{14}	6 p	0402AU6R0KAT	0402	AVX
C_{15}	1 p	0402AU1R0KAT	0402	AVX
C_{16}	100 p	0402AU101KAT	0402	AVX
C_{17}	2 p	0402AU2R0KAT	0402	AVX
C_{18}	5 p	0402AU5R0KAT	0402	AVX
D_1	SMV1763-079	SMV1763-079	SC-79	Skyworks Solutions
D_2	SMV1763-079	SMV1763-079	SC-79	Skyworks Solutions
D_3	SMP1320-079	SMP1320-079	SC-79	Skyworks Solutions
D_4	SMP1320-079	SMP1320-079	SC-79	Skyworks Solutions
L_1	100 nH	LL1608-FHR10	0603	TOKO
L_2	100 nH	LL1608-FHR10	0603	TOKO
L_3	15 nH	0402CS-15NXJB	0402	COILCRAFT
L_4	10 nH	0402CS-10NXJB	0402	COILCRAFT
L_5	15 nH	LL1005-F15NS	0402	TOKO
R_1	50	CR10-500J-T	0402	AVX/KYOCERA
R_2	1 k	CR10-102J-T	0402	AVX/KYOCERA
R_3	1 k	CR10-102J-T	0402	AVX/KYOCERA
R_4	1.5 k	CR10-152J-T	0402	AVX/KYOCERA
R_5	6.8 k	CR10-682J-T	0402	AVX/KYOCERA
R_6	3.9 k	CR10-392J-T	0402	AVX/KYOCERA
R_7	270	CR10-271J-T	0402	AVX/KYOCERA
R_8	100	CR10-101J-T	0402	AVX/KYOCERA
V_1	NE68119	NE68119	SOT-416	NEC/CEL
V_2	NE68019	NE68019	SOT-416	NEC/CEL

Table 3. The VCO's Bill of Materials

Measurement and Simulation Results

The measured performance of this circuit and the simulated results obtained with the model above are shown in Figures 12 and 13. The simulated results agree with the measurements confirming the validity of the VCO model. A difference of about 1 dB in simulation of the output power at low band may be attributed to the effects of higher harmonics. A more precise VCO simulation would require more accurate modeling of miscellaneous parasitic components such as pad capacitances to the ground, transmission lines and discontinuities. Note that in the simulations, the low band resonator inductor (L_3 = 15 nH in Figure 10) was replaced with a 16.5 nH measured for that type of inductor in our lab. Another reason for the divergence of simulated power response from the measurements may be in the precision of the transistor models used. These models are usually derived for small-signal or relatively weak-signal amplifier applications, and may not reflect the highly nonlinear operation of a VCO.

Both measured and simulated VCO output power variations in the tuning ranges are less than 1 dB. The measured frequency tuning sensitivity in Figures 12 and 13 are relatively linear at 27 MHz/V (low band) and 28 MHz/V (high band) in the 0.5–2.5 V range for battery applications. The simulated frequency tuning response is very similar to the measured one, although a slightly higher tuning voltage was observed in simulations for high band over the 2 V varactor bias voltage.

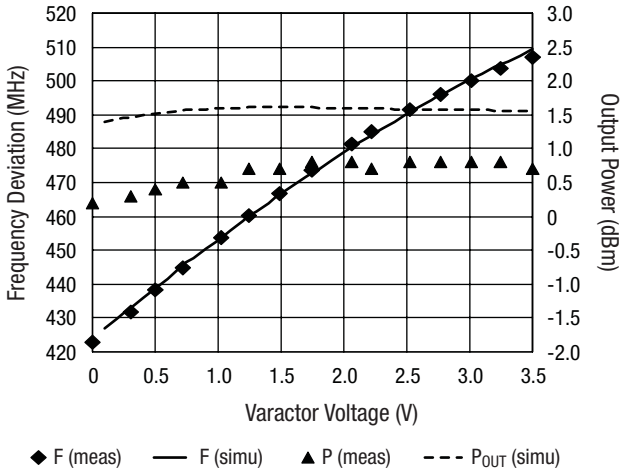

Figure 12. Low Band VCO Tuning Performance

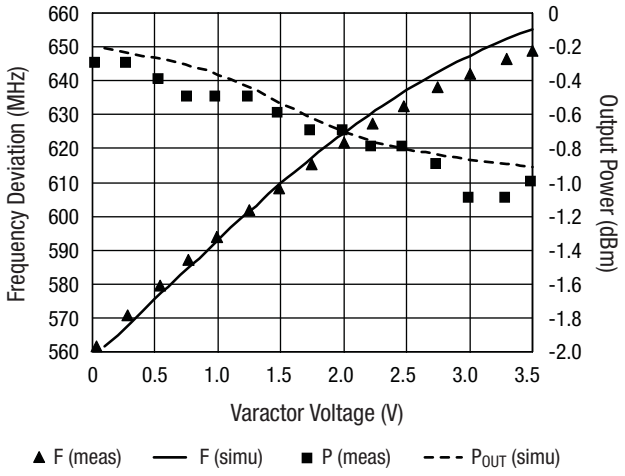

Figure 13. High Band VCO Tuning Performance

Phase noise measurements vs. frequency offset for both low band and high band are shown in Figure 14. It shows -100 dBc/Hz in high band and -105 dBc/Hz in low-band at 10 kHz offset and -120 dBc/Hz and -126 dBc/Hz at 100 kHz offset. The 20 dB/Decade slope is fairly constant to 5 MHz. The measurements were done using a Comstron-Aeroflex PN9000 Phase Noise Test Set in the range of less than 7 MHz offset because of the 100 ns delay-line setup used.

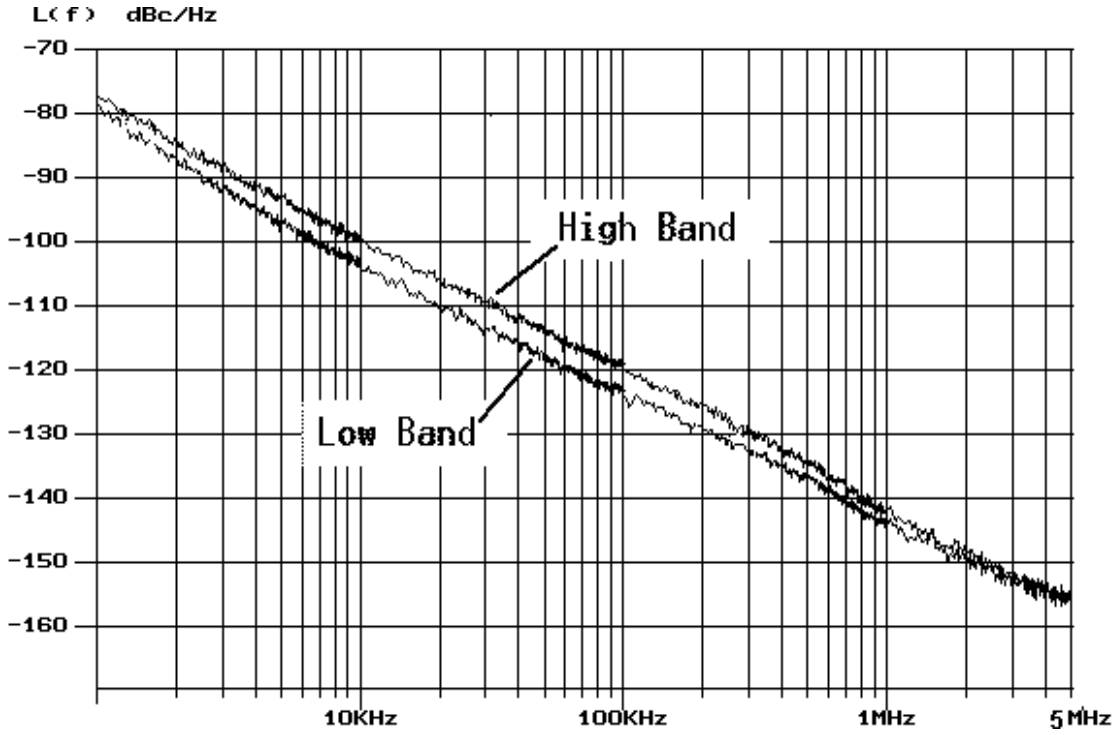

Figure 14. Measured VCO Phase Noise for Low and High Bands at V_{CC} = 3 V, V_{VAR} = 1.5 V

List of Available Documents

The GSM/PCS Switchable IF VCO Simulation Project Files for Libra IV.

The GSM/PCS Switchable IF VCO Circuit Schematic and PCB Layout for Protel EDA Client 1998 version.

The GSM/PCS Switchable IF VCO PCB Gerber Photo-plot files.

VCO Related Application Notes

APN1004: Varactor SPICE Models for RF VCO Applications

APN1006: A Colpitts VCO for Wide Band (0.95 GHz 2.15 GHz) Set-Top TV Tuner Applications.

APN1005: A Balanced Wide Band VCO for Set-Top TV Tuner Applications.

APN1007: Switchable Dual-Band 170/420 MHz VCO For Handset Cellular Applications.

An RF VCO Design for Wireless and Broadband

A Differential VCO for GSM Handset Applications