

APPLICATION NOTE

PCB Design Guidelines for High Power Dissipation Packages

Introduction

This Application Note provides PCB design guidelines for high power dissipation packages that ensure adequate solder coverage and optimize heat transfer. As a general rule, high power dissipation packages can be defined as those that dissipate more than 1.5 W (note that this is not the same as the RF output power). Such packages are generally those with an exposed electrical/thermal ground pad, such as Multi-Chip Modules (MCMs), Quad Flat No-Leads (QFNs), etc.

The amount of power dissipation depends on the RF output power and the Power-Added Efficiency (PAE). Power dissipation in the form of heat is the difference between the combined DC and RF input power, and the RF output power. Good heat sinking is absolutely essential to guarantee the long term reliability of these parts.

Design Guidelines

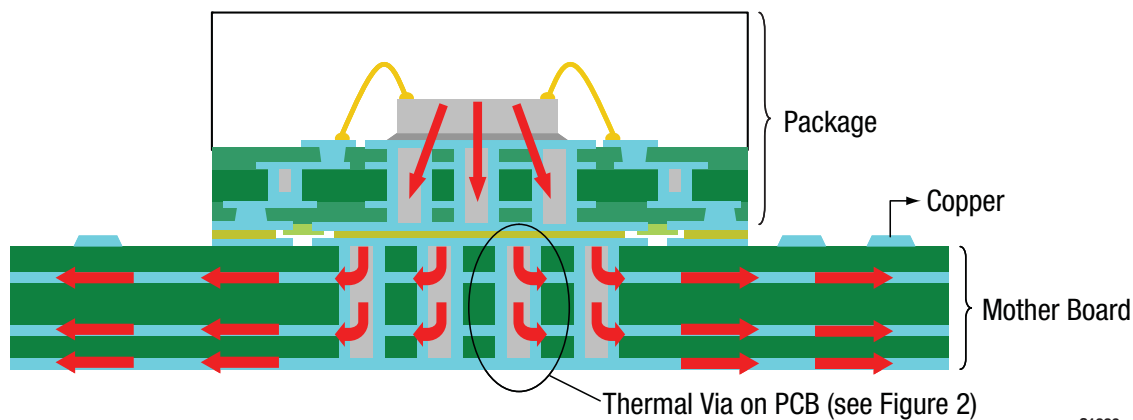
1. The major heat flow path from the package to the ambient is through the copper on the PCB (see Figure 1).
2. Maximize the copper coverage on all the layers to increase the effective in-plane thermal conductivity of the board. This is

especially important when no heat sinks are attached to the PCB on the other side of the package.

3. Add as many thermal vias as possible directly under the package ground pad to maximize the effective out-of-plane thermal conductivity of the board.
4. All thermal vias must be either plated (copper) shut or plugged and capped on both sides of the mother board (see Figure 2). This prevents solder seeping in to the thermal vias resulting in solder voids. Solder voids are highly detrimental to the thermal and electrical performance of the package.

Skyworks recommends using paragraph 3.6.2.11.1 of the *Qualification and Performance Specification for Rigid Printed Boards* [1] as the copper wrap plating specification.

5. To ensure reliability and performance, the solder coverage should be at least 85 percent. This means the total voids on the ground pad should be less than 15 percent with no single void larger than 1 mm. Several smaller voids are always better than a few big voids.



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Figure 1. Major Heat Dissipation Path From The Die to Ambient

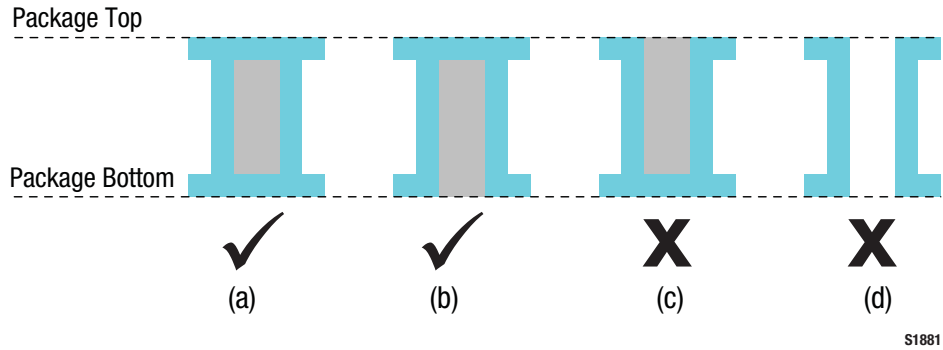


Figure 2. Thermal Via on PCB
(a) & (b) = Correct Via Design; (c) & (d) = Incorrect Via Design

References

1. *Qualification and Performance Specification for Rigid Printed Boards*, IPC-6012B, Amendment 1, December 2006.
[http://www.ipc.org/4.0_Knowledge/4.1_Standards/6012B-Amendment-1\(12-06\).pdf](http://www.ipc.org/4.0_Knowledge/4.1_Standards/6012B-Amendment-1(12-06).pdf)

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