APPLICATION NOTE

Mounting Considerations for Exposed-Paddle Packages

Introduction
Many of Skyworks products incorporate exposed paddles in their packages. The exposed paddle or exposed pad packages operationally decrease the thermal resistance, which provides superior heat dissipation from the die. The packages fall into two main categories: Quad Flat No-Lead (QFN), and inline Dual Flat No-Lead (DFN) as shown in Figures 1 and 2.

Figure 1. QFN Package

Both of these packages add meaningful system-level advantages including reduced electrical parasitic, smaller package footprint, lower package profile (height), and reduced package volume. An example of this type of package is given in Figure 3.

Figure 3. Exposed-Paddle Package

PCB Layout Considerations
Device reliability is directly influenced by junction temperatures within device structures. Improper connection of the exposed paddle can cause an increase in junction temperature, increase in power usage, and poor electrical performance. Heat generated by a surface-mount package is conducted to the PCB and then radiates to the surrounding environment. An exposed paddle I/C augments the heat transfer process by establishing a low thermal resistive path to the PCB. There must be an area of solderable copper underneath the exposed pad. This area is called the “thermal land.”

Thermal Lands
The QFN or DFN thermal land is a copper region under the package and located on the top of the PCB. Its geometry is a square or rectangle and should be the same dimensions (1:1 ratio) as the exposed pad. For a more effective thermal performance, the DFN package can be modified to a shape called a “dog bone” (Figure 4).

Figure 4. Top View of DFN Package Modified to Dog Bone Configuration

The exposed pad is most often, but not always, connected to ground. If it is connected to ground from the top and bottom of the thermal land, there are many possible ways to connect it to the top layer ground plane.

Thermal Layers in the PCB
For a double-sided PCB, using a minimum 1 oz. of copper, the surface layers (top and bottom) must be used to disperse the heat. In a four-layer PCB (two signal layers and two layers for power/ground), the area of the embedded copper layer connecting to the thermal vias has a profound effect on the thermal performance of the package. Figure 5 shows a typical four-layer PCB with the thermal vias connected to a dedicated ground plane. When using a two-layer PCB, an area of copper equal to or greater than the dimensions of the exposed pad must be provided to connect the thermal vias.
Thermal Vias

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes. The number of vias used, the size of the vias, and the finished thickness are all important factors in both the exposed pad package thermal performance and the integrity of assembly.

The number of vias varies with each product being assembled to the PCB, depending on the quantity of heat that must be moved away from the package and the efficiency of the system. Characterization of the heat removal efficiency versus the thermal via copper surface area should be performed to arrive at the optimum number for a given layout. Then the number of vias required can be determined for any new design to achieve the proper thermal removal value.

Guidelines for the Construction of Thermal Via Arrays

As an example, let’s use a QFN44-24 (4 x 4 mm) package with an exposed pad (2.6 x 2.6 mm). Figure 6 shows a staggered array of vias spaced in offset rows with a spacing of 0.38 mm (15 mils) between columns and 0.38 mm (15 mils) between rows. The vias in this example are 12 mils in diameter with a 6 mil hole. A via hole diameter of 0.33 mm (13 mils) or smaller is best when plating with 1 oz. copper. The diameter of the via should be 5 mils greater than the hole size. The vias in the example can be 13 mils in diameter with an 8 mil hole.

All thermal vias must make internal connections to the planes using a continuous connection completely around the hole diameter (never use a relief pattern). The vias on the outer bounds of the pad area are up to 5% more effective than the vias placed centrally. When increasing the number of vias in a pad area, there is a corresponding improvement in package thermal performance. As a general rule, the maximum number of vias is close to the optimal number.

Solder Stencil

Exposed pad packages require solder stencils for correct mounting. Single pattern stencils can be made for the QFN and DFN packages. A standard stencil thickness of 5 mils allows a 1:1 stencil aperture-to-board pad ratio. The exposed pad aperture for the pattern should be reduced between 70% and 85% to prevent overprinting the solder.

For reference, Cookson Electronics can make single pattern stencils using a small Ball Grid Array (BGA) template that can be used for prototyping reference circuits (see the Cookson Electronics website, www.alphametals.com, for the stencil design principles for all types of electronic components).
Rework procedures indicate that part removal from the PCB is successful using conventional techniques. By using standard solder equipment (hot air gun, reflow oven, hot plate, and solder iron), replacement of the QFN and DFN packages can be routinely accomplished.

The main consideration is directing heat to the component body without over-heating adjacent components. After removing the part, clean the area and apply solder paste using a stencil. Carefully position the component and reflow part using the same profile as used for the original assembly. See Figure 7 for a common reflow profile.

Summary
Exposed paddle packages are simple to use, and can be assembled and repaired using standard tools and techniques. With the addition of the thermal land and thermal vias on the PCB, any design can effectively use the QFN and DFN exposed pad packages.