APPLICATION NOTE

SKYA21004: PCB Layout Guidelines

Introduction

PCB layout design is essential to better performance, reliability and manufacturability. Malfunctions from noise, which may hurt the system stability, have become an increasing problem, and may therefore generate more failures and reliability malfunctions in production lines.

In this document, several considerations and guidelines for SKYA21004 PCB layout design are presented to improve performance, reliability, and manufacturability.

Guidelines for Land Pattern and Thermal Vias on the SKYA21004

The SKYA21004 is a QFN 36L package with a center ground pad (exposed pad). The PCB center ground pad serves three major functions: electrical ground, thermal heat sink, and mechanical support. Ground pad size and soldering quality (such as the wetting and voids) directly affect the ground pad functions. Dimensions of the center ground pad are shown in Figure 1. The center ground pad should be well connected to the terminal ground pad and the common ground plane of the PCB to optimize its functions.

Figure 1 shows the recommended land pattern for the SKYA21004.

![Figure 1. Recommended Land Pattern and Thermal Vias for the SKYA21004 (All dimensions are in millimeters)]
Electrical and Thermal Performance

To improve thermal and electrical performance of a mounted SKYA21004, an array of thermal vias placed on the area of the ground pad should be connected to the internal and bottom common ground copper planes of the PCB. In general, there is a direct correlation between the thermal via cross-sectional area and the heat dissipation rate. However, large and excessive thermal vias may introduce more voids in the solder joint and actually reduce overall heat dissipation performance.

Recommended thermal vias are 0.30 mm to 0.33 mm in diameter, and via barrels should be plated with 1 oz. of copper to plug the vias. The thermal via array should be arranged evenly with a pitch of 0.5 mm to 1.0 mm. For the exposed region of the ground pad, if the plating thickness is not sufficient to effectively plug the barrel of the via when plated, solder mask should be used to cap the vias with a minimum dimension equal to the via diameter plus 0.1 mm. This will prevent solder wicking through the thermal via during the soldering process, resulting in voiding.

Another way to plug thermal vias uses solder mask tenting on the bottom of the copper plane. Solder mask tenting must completely cover the vias.

In the SKYA21004 layout, it is recommended to arrange 24ea vias evenly with a pitch 0.6 mm, as shown in Figure 1.

For more detailed information refer to the Skyworks Application Note #101752I.

Guidelines for the Boost Section for LED Backlight Driving and LCD Bias Power

The SKYA21004 is divided into two blocks as its operating purpose. One is a LED Backlight Driving Boost Section and the other is an LCD Bias Power Boost Section. To prevent interactive noise between two individual power blocks (LCD Bias Power and LED Driver), use independent planes for PGND (power ground for LCD Bias Power) and WPGND (power ground for LED Driver).
Layout of LED Driver Boost Section Procedure

1. Connect the inductor and diode as close to the WLX node as possible.
2. Connect Cin capacitor close to the inductor and Cout capacitor(s) close to the diode.
3. Connect the Cout ground return and IC WP冈ND with direct wide and short trace. If needed, connect the ground return on multiple layers with multiple vias connected.
4. Make the PCB traces between Cin and inductor, inductor and WLX pin, WLX pin and diode, diode and Cout as wide and as short as possible.
5. The trace should be wider than 1.5 mm.
6. Isolate the WP冈ND return from the AGND, DGND, SGND, and GND. Connect the WP冈ND to the system ground near the system input.
## Layout of LCD Driver Boost and Charge Pump Section Procedure

1. Connect the inductor and diode as close to the LX node as possible.
2. Connect CIN and COUT capacitor(s) as close to the IC as possible.
3. Connect the COUT ground return and IC PGND as close as possible.
4. Make the PCB traces between CIN and inductor, inductor and LX pin, LX pin and diode, diode and COUT as wide and as short as possible.
5. Trace should be wider than 1.5 mm. Connect all grounds of the charge pump to PGND.
6. Isolate the PGND return from the AGND, DGND, SGND, and GND.
7. Connect the PGND to the system ground near the system input.
Please follow SKYA21004 recommended landing pattern and use 0.3 mm to 0.33 mm thermal vias with 0.5 mm to 1 mm pitch size between vias.

C\text{OUT} ground is returned to WPGND directly.

Place C\text{BP}, C\text{OUT}, Inductor, Diode as close to LX.

C\text{OUT} ground is returned to PGND directly.

Place C\text{BP}, C\text{OUT}, Inductor, Diode as close to WLX.
Guidelines of Analog and Feedback Section

The Analog and Feedback section is an important block for stable system operation. For stable operation, these sections should be isolated from the noise of the boost and charge pump section. Grounds for the analog and feedback sections should be connected to the plane of AGND, DGND, SGND, and GND.

Layout of Analog Section Procedure

1. Connect the resistors and capacitors for IN, OUT, VL, COMP, WCOMP, ISET, FOSC, and OVP as close to the IC as possible.
2. Connect to DGND ground plane for ground return.
3. Use the same ground plane for AGND, DGND, SGND, and GND.

Feedback Layout Design Considerations

- Feedback sensing points – All feedback points including FB, FBP, FBN, and OVP should be sensed from the output capacitor for stable and precise output feedback.
- Routing of the feedback line – To avoid coupling effects, sensitive lines should not be routed on top of the digital or switching signal. Sensitive lines also should not be placed in parallel with a digital or switching signal.

Figure 6. SKYA21004 Analog Section
**Layout of Feedback Section Procedure**

1. Connect the OVP resistors to the OUT capacitors with a dedicated ground shielded trace to avoid interference from other signals. This trace is used as a feedback for the WLED boost regulator.

2. Connect the AVDD/VGH/VGL feedback resistors to the OUT capacitors with a dedicated ground shielded trace.

3. To avoid coupling effects, sensitive lines should not be routed on top of the digital or switching signal.

4. When connecting nodes from the other layer, use at least four 0.4 mm hole diameter, 0.7mm pad diameter vias (conductive filled via is preferred).

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**Figure 7. SKYA21004 Feedback Section**

**Figure 8. Example of Routing the Sensitive Line**
Figure 9. SKA21004 Pinout

Figure 10. SKYA21004 Layout Example (Analog and Feedback Section)

- Share the same ground plane with AGND, DGND, SGND and GND.
- Connection for OVP sensing is close to output capacitor. OVP sensing line is also placed perpendicular to avoid coupling from current sink lines. (Blue line showing the OVP routing on the bottom layer)
- Individual planes for PGND and WPGND and AGND.