APPLICATION NOTE

Thermal Design Considerations and Mounting Guidelines for AWB Series Products

Introduction

The surface-mount package construction and electrical contact (pin) locations of the Skyworks AWB series of power amplifiers require special considerations for proper mounting to printed circuit boards (PCBs).

This application note presents technical background and suggests methods for soldering AWB devices to a PCB that will result in reliable electrical and thermal contacts.

Printed Circuit Board Thermal Design Considerations

The junction temperature (TJ) is defined as the maximum temperature present within the overall structure of the circuit that is fabricated onto the die. The "junction" refers to a point source that emanates thermal energy generated by the combination of DC and RF power dissipated by each active device that constitutes the primary circuit within the amplifier module.

The case temperature (TC) is defined as the external temperature of the bottom surface of the package. This bottom surface is comprised of gold-plated copper and is the main facilitator of thermal energy transfer from the die to the PCB mounting area and heatsink. All thermal calculations are referenced to the case temperature (TC) because it can be directly measured with the appropriate instrument. Conversely, the junction temperature (TJ) can only be calculated indirectly as the die is normally inaccessible.

In general, it is essential to keep the junction temperature (TJ) of the device as low as possible in order to ensure long operating life. This can be accomplished by providing good thermal relief and adequate heat sinking. When mounted to a printed circuit board (PCB), the delta between the device case temperature (TC) and the ambient temperature will be determined by several factors; board thickness and number of layers, copper plating thickness, size and number of vias placed beneath the ground area of the case, the PCB layout, the method of attachment of the PCB to the heat sink as well as the design of the heat sink. For typical applications, it is recommended to maximize the number of vias placed below the package ground area.

Our standard AWBXXX evaluation boards are fabricated using Rogers R4003 PCB material which has a dielectric constant of 3.55, dielectric thickness of 8mils (0.2mm), and copper thickness of 1.4 mils/side (0.0356mm). 59 thru vias are used under the ground paddle to maximize thermal efficiency. Figure 1 shows example using standard EVB of solder stencil coverage for ground paddle.

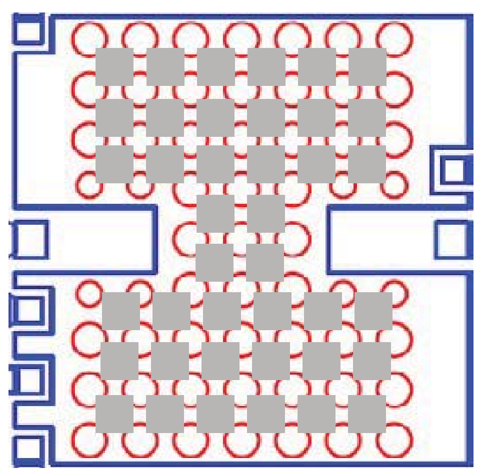

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Figure 1 PCB Via Hole Layout and Solder Stencil for 7x7 mm Package (59 Vias)

The Physics of Heat Transfer

Conductive heat transfer or flow (Q) across any interface is given by the equation:

$Q = kAT\Delta / L$

where:

Q = heat flow

k = thermal conductivity (of the material), W/mm

CA = area (cross section) of the heat flow path, mm2

L = interface thickness (path length), mm

$T\Delta$ = temperature difference (drop) across the interface

The thermal resistance (Rt) is analogous to electrical resistance and is defined as:

$Rt = T\Delta / Q$

Substituting, we have:

$Rt = L / kA$ (C/W)

For a surface-mounted part, the total thermal resistance (Rt-tot) consists of the path from the Amplifier Die through the die-attach (Rt-dat) and the bottom surface of the package (Rt-pkg), through the PCB solder (Rt-sld), then through the PCB vias (Rt-pcb), and finally through the bottom interface (Rt-int) to the Heatsink. This path (from the die to the bottom surface) is the primary conduit for conduction of thermal energy! Very little thermal energy is conducted out to the top of the package or to the sides of the package because the moulding compound filler material that occupies the otherwise empty internal volume of the package possesses poor thermal conductive properties.

Thus the total heat path thermal resistance is:

$Rt\text{-}tot = Rt\text{-}dat + Rt\text{-}pkg + Rt\text{-}sld + Rt\text{-}pcb + Rt\text{-}int$

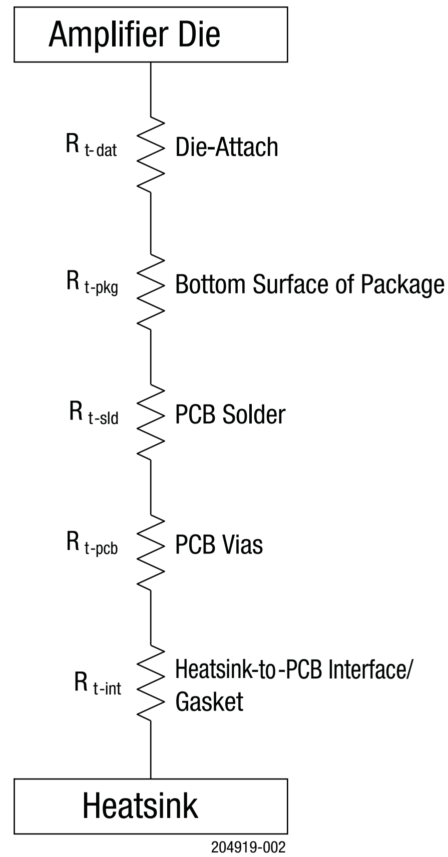

Figure 2. Thermal Resistances

Thermal Resistance of the PCB

The thermal resistance of a single copper via (not solder filled) can be calculated as:

$\theta_{VIA} = L / \{\sigma^* \pi[Ro^2 - (Ro - Rpl)^2]\}$

For a via path length L = 0.274 mm, with drilled hole radius Ro = 0.15 mm, copper plating Rpl = 0.036 mm, and copper thermal conductivity σ = 0.39 W/mm°C, the thermal resistance of each via is 22.39°C/W. Therefore, the θ_{PCB} using 28 non-solder-filled vias is approximately 0.8°C/W.

For solder-filled vias, the thermal resistance of the solder fill can be calculated as:

$\theta_{solder\_fill} = L / (\sigma solder^* Area_{solder\_fill})$

where:

$Area_{solder\_fill} = \pi (Ro - Rpl)^2$

Therefore, $\theta_{solder\_fill} = L / (\sigma solder^* \pi(Ro - Rpl)^2)$

The thermal conductivity of solder (σsolder) = 0.05 W/ mm °C, the thermal resistance of each solder fill is 134.22 °C/W. Therefore, the total θ_{solder_fill} for all vias on the PCB will be: 134.22 / 28 = 4.79 °C/W.

Combining the thermal resistance of the vias and the solder fill, the overall θ_{PCB} with 28 filled vias will be 0.69 °C/W.

Thermal Resistance of the Solder Interface

Solder is the most commonly used interface between the bottom grounding surface of the package and the via-holes that comprise the thermal-transfer area of the PCB footprint. The thermal resistances of the solder attachments ($R_{t\text{-}sld}$) are calculated below for both 4x4 mm and 7x7 mm packages with bottom-grounding surface areas of approximately 9mm^2 and 37mm^2, respectively. A solder thickness of .025 mm is assumed for both packages. This magnitude of thickness is considered be to be a well-executed solder attachment.

Package Type	4x4mm	7x7mm
Ground surface area (mm^2)	9	37

$R_{t\,sld\text{-}4x4} = L / kA = 0.025 / (0.050 \times 9) = 0.056\ °C/W$

$R_{t\,sld\text{-}7x7} = L / kA = 0.025 / (0.050 \times 37) = 0.014\ °C/W$

As can be seen from the above numbers, the added thermal resistance from the solder attach is about two orders of magnitude smaller than that of the vias, and can be safely ignored (as long as the solder is kept to minimum thickness).

Thermal Resistance of the Heatsink Compound and Gaskets

The PCB-to-heatsink interface $R_{t\text{-}int}$ can be similarly calculated, but will vary according to the attachment method used (heatsink compound or gasket) and is hard to quantify (because the average L depends on the smoothness of the heatsink surface). It should be remembered, that the best of heatsink compounds exhibit a k value in the 0.001 to 0.007 W/mm °C range and that the typical 0.2mm thermal gasket sheet such as the *Laird* TFlex™ series has a k value of approximately 2 W/mm °C (vs 0.390 W/mm °C for copper). Therefore, tight fit (screw down) and a smooth surface are important, but in any case, the $R_{t\text{-}int}$ is still a small fraction of the total R_t.

Any decrease in the PCB R_t due to heat transfer in the PCB material can also be ignored due to its poor heat conductance.

Heat Rise

Finally, knowing all of the thermal resistances, we can calculate the resultant temperature difference between the grounding surface on the bottom of the package and the heatsink. For example, using the Skyworks AWB7227 power amplifier module that draws about 750 mA @ 4.5 VDC with a total power dissipation of approximately 2.9 W, a PCB with 59 non-solder-filled vias configured as shown in Figure 2, will be about: 0.38 °C/W * 2.9W = 1.1 °C. Adding an estimated 1.5 °C rise for the solder and PCB mount interfaces, the total temperature rise will be less than 3 °C.

The maximum operating case temperature (T_C) for the AWB7227 device is specified as +85 °C, so it can be seen that should the heatsink (ambient) temperature ever rise to +70 °C a safety margin of more than 10 °C would still exist.