A Screen-Printed Thick Film Copper Pillar Process

Kezia Cheng, Boris Dzyubenko, Michael Duval

Skyworks Solutions, Inc., 20 Sylvain Road, Woburn, MA 01801

kezia.cheng@skyworksinc.com (781) 241-2821

Keywords: Copper pillar bump, screen printing, thick film technology, coplanarity, fine pitch

Abstract

The semiconductor industry is transitioning from wire bonding (WB) with through-wafer vias (TWV) to flip-chip (FC) die attach using copper (Cu) pillars. The improved ground inductance and heat dissipation of flip-chip die attach provide superior performance. The current standard for copper pillar bump (CPB) processes is plated Cu and tin silver (SnAg) solder cap. Plated pillar processes have some inherent challenges. Coplanarity issues and die stress are among the difficulties. Here, we report the successful development of a thick film screen printed Cu pillar bump process for heterojunction bipolar transistors (HBTs). The screen-printed Cu pillars have excellent bump height uniformity. The much lower Young's modulus of the thick film Cu translates into 30% lower die stress. This paper examines the technical advantages of this technique and its transitioning from concept to manufacturing.

INTRODUCTION

In the never-ending pursuit for higher performance, the semiconductor industry is driving the replacement of through-wafer vias (TWV) and wire bonding with flip-chip die attach. This is also spurred on by the higher integration levels (more post power amplifier (PA) losses and higher power levels cause the PA to be driven harder). The motivation for this transition is clear. In a side-by-side comparison, flip chip die attach is demonstrably superior to TWV in heat dissipation [1][2] with lower ground inductance.

Presently, the dominant pillar bump technique is plating. These processes begin with sputtered plating seed deposition. Typical Cu plating rate ranges from 0.3µm/min to 1µm/min. For a pillar height of 30µm, the plating process can exceed an hour.

Pillar coplanarity is a prevalent issue for assembly. Since large area bar bumps plate faster than smaller bump, height differences of greater than 5µm can occur. This disparity can lead to die attach problems. 3D automated optical inspection (AOI) is often employed to screen out dies that fail the coplanarity specification [3].

For assembly, solder surface mount technology (SMT) reflow is conducted at about 250°C. The coefficient of thermal expansion (CTE) mismatch between GaAs, Cu and the laminate can impart substantial stress on the die and lead to die cracking [4] and metal fatigue failure.

THICK FILM TECHNOLOGY

Thick film technology, primarily applied by screen printing, has a history spanning several decades. A metallic paste is screen printed onto hybrid electronics or ceramic packages. The metal paste is then fired in a forming gas furnace that solidifies the paste into metallic traces and contacts. Modern screen printers, designed for semiconductor device fabrication, achieve resolution in the 10µm to 20µm range. The alignment precision and print resolution are adequate for pillar applications. A stencil is used for screen printing metallic pastes. Variables like the stencil thickness, critical dimension (CD) and the paste properties dictate the final print results.

CU PASTE SELECTION

Selecting the right Cu paste is vital to the success of the process. Several criteria must be met. First, the firing temperature cannot exceed 300°C. Equally important is that the final sintered Cu must have low resistivity. Finally, the material viscosity must be suitable for screen printing.

Cu thick film pastes typically require a firing temperature in the 800°C to 900°C range. Advancement in Cu paste technology with new formulations have resulted in much lower sintering temperature. Resonac paste [5], for example, can be fired at 250°C in a formic environment and achieve low resistivity. However, the relatively low viscosity of this paste is not suitable for stencil printing. To leverage the low resistivity and reduced sintering temperatures of Cu pastes, novel processes must be developed.

DRY FILM

Our CPB process begins with dry film resist lamination. Embedding lamination mode is used to ensure the Toray dry film conforms over the HBT topology. The laminated wafer is aligned and exposed on a Quintel mask aligner in proximity

mode. The polyimide dry film requires a post exposure bake (PEB) before developing in tetramethylammonium hydroxide (TMAH).

Unlike plated processes where the photoresist is stripped after plating, we leave the dry film on the wafer for technical reasons. As such, the thermal conductivity, CTE, and the dielectric constant should closely match that of the underfill epoxy and overmold compound. Additionally, the glass transition temperature (T_g) of the dry film must be higher than the sinter temperature of the Cu paste. Otherwise, the resist will reflow, altering the profile of the pillars.

Fig. 1. Cu pillar locations after photo development

Cu Pillar Print

The next process step is filling the openings in the dry film at the pillar locations with the Cu paste. The Cu paste is applied without a stencil on a vacuum screen printer. The rough vacuum ensures no voids are trapped under the pillars.

The wafers are sintered at 250°C for 45 minutes in a formic oven. Some minor shrinkage in the Cu is observed. Nevertheless, the Cu fills the pillar locations squarely to the dry film without voids. The entire wafer now has a planar surface, which serves as the foundation for the subsequent solder bump printing step. The pillar height is defined by the thickness of the dry film, as the Cu paste is filled flush to the film, thereby eliminating coplanarity issues.

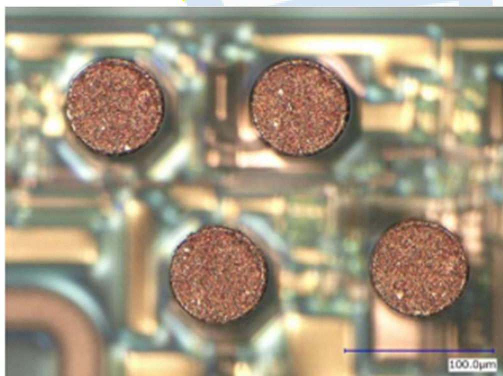

Fig. 2. Cu paste filled the dry film without voids. After sintering, the wafer has a planar surface.

Solder Print

Screen printing of solder paste onto MCM laminates and printed circuit boards (PCB) is a well-established and widely implemented process. We opt to stencil print Type 6 SnAg paste directly on the wafer to form the solder bumps.

The polyimide dry film has similar properties to the solder mask on a PCB in which the solder does not wet the polymer. As the solder reaches the melting point, the molten solder wets and coalesces on the Cu making the process self-aligning. This solder print process is, therefore, tolerant to small print misalignments. Because the Type 6 solder paste contains flux, no additional application of flux is necessary. After reflow, a strip in acetone and NMP removes the solder flux completely from the wafer. The solvent does not affect the underlying polyimide.

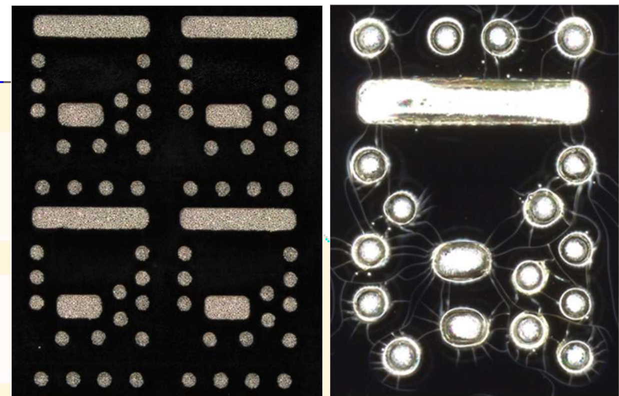

Fig. 3. Left: Type 6 solder paste as printed. Right: After solder reflow.

We processed the wafers through backend wafer grind and singulation. Dies were picked and assembled into modules for small signal and large signal studies. A control group with the process of record (POR) Cu pillar process was included.

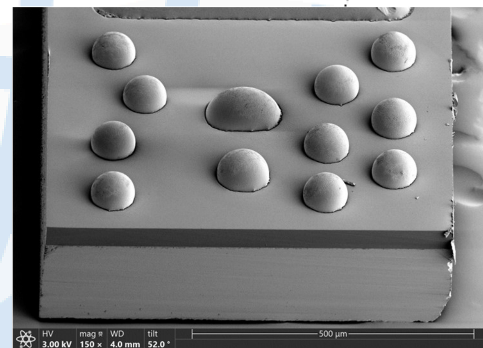

Fig. 4. HBT die with screen-printed Cu pillar bump

A standard infrastructure Wi-Fi module was used as a test vehicle to verify the module level performance. Modules built with the screen-printed Cu pillars passed the small signal test with most parameters closely matching the control group to within 1%.

TABLE I
SMALL SIGNAL TEST RESULTS OF SCREEN-PRINTED PCB MODULES MATCHING THE PERFORMANCE OF POR

	Screen-printed	POR plated	
	Mean (Qty=5)	Mean (Qty=5)	Delta
State 1 SSGAIN	-3.48	-3.45	0.03
State 2 SSGAIN	31.85	31.98	0.13
State 3 SSGAIN	14.83	14.63	-0.2
State 1 IRL	-9.87	-9.82	0.05
State 2 IRL	-9.94	-9.92	0.02
State 3 IRL	-9.52	-9.021	0.499
State 1 ORL	-9.28	-9.11	0.17
State 2 ORL	-11.2	-10.44	0.76
State 3 ORL	-10.92	-11.06	-0.14
State 2 Ant to RX ISO	-48.36	-48.71	-0.35
State 2 TX to RX ISO	-20.2	-20.77	-0.57

Consistent with the small signal test, modules fabricated with screen-printed Cu pillar dies exhibited similar performance in large signal test. All RF parameters were found to be virtually identical to those of the POR modules.

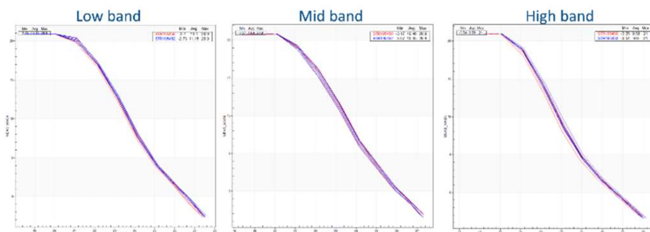

Fig. 5. Screen-printed CPB modules closely matched the plated CPB in RF performance

DISCUSSION

A significant concern in flip chip die attach is the susceptibility of the die to cracking, which results from mechanical and thermal stresses. On post SMT reflow ramp down, the CTE mismatch between the MCM laminate, GaAs and Cu create significant stress. Plated Cu has a Young's modulus consistent with the bulk material at 120GPa. Simulation predicts a corresponding die stress of 144MPa. In contrast, sintered thick film Cu has a significantly lower Young's modulus of 30GPa. This material property implies a higher degree of material compliance. A 75% reduction in Young's modulus reduces the die stress to 103 MPa, a 30% decrease that is expected to minimize die cracking.

Two test boards, one assembled with a screen-printed pillar die and the other utilizing a POR die, were decapsulated for thermal scan. The results indicated that the screen-printed pillar die operates approximately 5°C higher than the electroplated counterpart. The slightly elevated operating temperature is attributed to the thickness of the solder bump. Reducing the tin-silver (SnAg) solder thickness by 5µm is expected to decrease the die temperature and improve gain. The height of the screen-printed solder can be precisely managed by selecting an appropriate stencil thickness. Further fine-tuning of this process is achievable by biasing the CD of the stencil apertures.

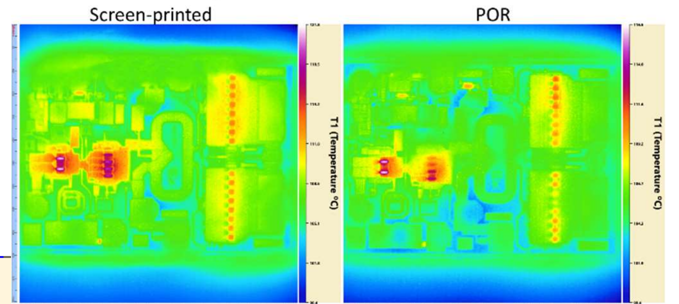

Fig. 6. Thermal scans revealed that the screen-printed Cu pillar die runs 5 degrees hotter than POR

Yield loss due to non-conformance with coplanarity specifications is a frequent occurrence in the plated pillar process. The screen-printing process guarantees consistent pillar and bar bump heights, as the process inherently planarizes the Cu thick film paste within the dry film apertures.

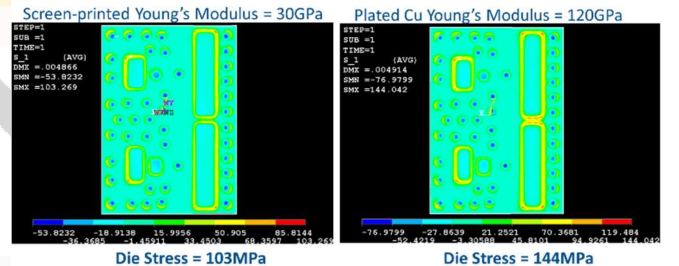

Fig. 7. Simulation shows screen-printed CPB die has 30% lower die stress

Because of the simplified process flow, the screen-printed approach offers superior throughput and reduced cycle time. In contrast, seed layer deposition in a plating process requires a sputter system. The plating bench and the plating solutions demand engineering resources for tool maintenance and bath analysis. Considering capital investment, the screen-printed Cu pillar process requires fewer tools and less capital investment. Furthermore, being a "dry" process, it produces no hazardous byproducts or Cu discharge in the waste stream, thereby eliminating the need for an expensive wastewater treatment system.

The present industry-standard process for fabricating Cu pillars results in free standing pillar structures after electrodeposition. Our technique diverges from this conventional approach by retaining the permanent polyimide dry film on the wafer. The Cu pillars are encased in the polyimide with the solder bumps exposed. The Toray dry film exhibits a dielectric constant closely matching that of the underfill epoxy. Consequently, its presence is not expected to

influence the RF performance of the HBT. Furthermore, the dry film possesses a marginally superior thermal conductivity compared to the molding compound, which is considered a beneficial attribute.

The concern for whether the permanent polyimide dry film impedes the mold compound underfill process was also studied. Both non-destructive X-ray inspection and cross-sectional analysis revealed successful and complete underfill with no evidence of voids in the mold compound.

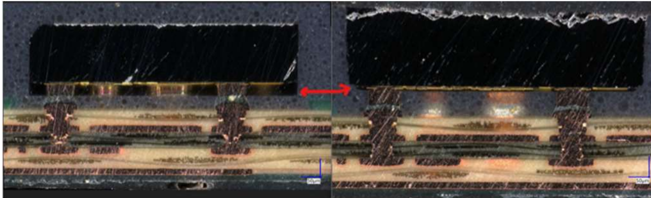

Fig. 8. Mechanical sectioning of packaged dies revealed complete molding compound underfill.

Encapsulating the copper pillars within the polyimide structure, such that only the solder interface is exposed, effectively eliminates the occurrence of solder wicking. This approach addresses the issue of pillar shorting, prevalent in bumping processes, which occurs due to the wicking of solder down the pillar sidewalls. This approach consequently enables finer pitch capability. Integrating the polyimide dry film as a permanent component of the wafer not only enables the realization of fine pitch pillar geometry but also enhances device reliability through the addition of a passivation layer.

Conclusions

We have proven the concept of the CPB process using thick film screen printing technology. Modules assembled using these screen-printed CPB dies demonstrate RF performance that compares favorably to the industry standard plating process in both small and large signal tests. Although thermal scans indicated that the screen-printed CPB die operates at a slightly higher temperature than the POR, the issue is easily addressed by reducing the solder bump height. This height reduction is achievable through further optimization of the printing stencil. The sintered Cu paste has much a lower Young's modulus. Simulation predicts a 30% reduction in die stress. This technique guarantees pillar coplanarity and enables small pitch pillar capability. The screen-printing process is simpler, leading to a significant reduction in cycle time and an increase in overall production throughput. We have demonstrated that the screen-printed Cu pillar is a compelling alternative technique to the conventional standard plated Cu pillar process.

Acknowledgements

The authors express gratitude to the Woburn and Ottawa Characterization teams for their execution of the small and large signal tests, and to Cory Severson for the comprehensive analysis and summarization of the test data. Furthermore, the authors thank Ejiri Yoshinori of Resonac and Yoshi Tanaka of Newlong Seimitsu Kogyo for conducting the Cu print demonstration runs and Toray Industries for supplying the polyimide dry film for this work.

References

[1] V. d'Alessandro, et al., "Simulation comparison of InGaP/GaAs HBT thermal performance in wire-bond and flip-chip technologies", Microelectronics Reliability, 78C, pp. 233-242 (2017).

[2] H.-C. Chang, et al., *Device Characteristics Analysis of GaAs/InGaP HBT Power Cells Using Conventional Through Wafer Via Process and Copper Pillar Bump Process,* 2013 CS ManTech Technical Digest*,* 2013.

[3] JEDEC bump height spec.

[4] V. Lin, et al., *Stress simulation and design optimal study for Cu pillar bump structure,* 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013), Singapore, pp. 598-601, 2013, doi: 10.1109/EPTC.2013.6745790.

[5] Y. Ejiri, et al., *Sintered Cu Paste as a Via-Filling Material for Through-Glass Via*, In 2026 Pan Pacific Strategic Electronics Symposium (Pan Pacific), pp. 101-110. IEEE, 2026.

Acronyms

WB: Wire Bonding
TWV: Through-Wafer Via
FC: Flip-Chip
CPB: Cu Pillar Bump
PA: Power Amplifier
AOI: Automated Optical Inspection
SMT: Surface Mount Technology
CTE: Coefficient of Thermal Expansion
CD: Critical Dimension
PEB: Post Exposure Bake
PCB: Printed Circuit Board
POR: Process of Record

CS MANTECH