



SKY66391-12: 1800 to 1900 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier

Applications

- SFDD and TDD 2G/3G/4G LTE systems
- 3GPP bands 3 and 9 small-cell base stations
- Driver amplifier for micro-base and macro-base stations
- Active antenna array and massive MIMO

The SKY66391-12 is part of a high-efficiency, pin-to-pin compatible PA family supporting all 3GPP bands. Table 1 lists the pin-to-pin compatible parts in the PA family.

Features

- High efficiency: PAE = 34.5% @ +28 dBm
- High linearity: +28 dBm with < -50 dBc ACLR with pre-distortion (40 MHz LTE, 8.5 dB PAR signal)
- High gain: 36 dB
- Excellent input and output return loss for 50 Ω systems
- Integrated active bias: performance compensated over temperature
- Integrated enable on/off function: PAEN = 1.7 to 2.5 V
- Single supply voltage: 5.0 V
- Pin-to-pin compatible PA family supporting all 3GPP bands
- Compact (16-pin, 5 x 5 x 1.3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)
- For RoHS and other product compliance information, see the [Skyworks Certificate of Conformance](#).

Table 1. Pin-to-Pin Compatible PA Family

Part Number	Frequency (MHz)	3GPP Band
SKY66391-12	1800 to 1900	Bands 3 and 9
SKY66399-11	1900 to 2000	Bands 2, 25, 33, 36, and 37
SKY66394-11	2000 to 2300	Bands 1, 4, 10, and 23
SKY66397-12	2300 to 2700	Bands 7, 38, and 41

Description

The SKY66391-12 is a high-efficiency, fully input/output matched power amplifier (PA) with high gain and linearity.

The compact PA is designed for FDD and TDD 2G/3G/4G LTE small cell base stations operating from 1800 to 1900 MHz.

The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.

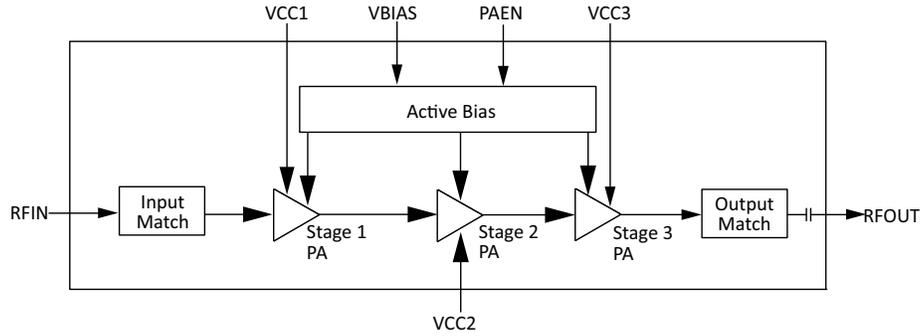


Figure 1. Functional Block Diagram

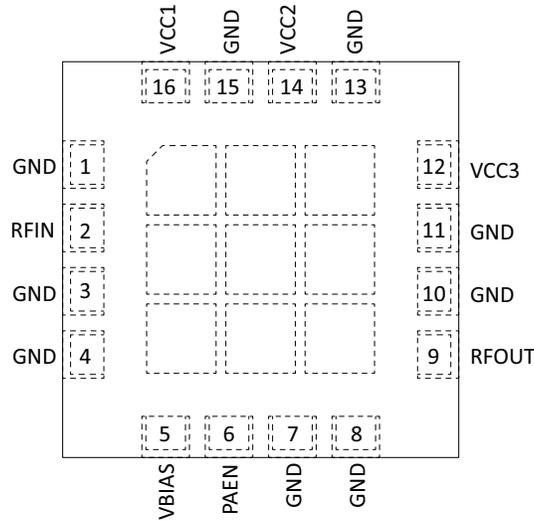


Figure 2. Pinout Top View

Table 2. Signal Descriptions¹

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

1. The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included for both input and output stages, for excellent gain tracking over temperature and voltage variations.

The SKY66391-12 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively).

The dc control voltage that sets the bias is supplied by the VCBIAS signal (pin 5).

Electrical and Mechanical Specifications

Table 3. Absolute Maximum Ratings¹

Parameter	Symbol	Min	Max	Units
RF input power (CW)	P_{IN}		+8	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC}		5.5	V
PA enable	V_{EN}		2.8	V
Operating temperature	T_C	-40	+100	°C
Storage temperature	T_{ST}	-55	+125	°C
Junction temperature	T_J		+150	°C
Power dissipation	P_D		1.4	W
Device thermal resistance	θ_{JC}		20.8	°C/W
Electrostatic discharge: Charged Device Model (CDM) Human Body Model (HBM)	ESD		500 1000	V

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	$V_{CC1}, V_{CC2}, V_{CC3}, V_{BIAS}$	4.75	5	5.25	V
PA enable ON OFF	P_{AEN}	1.7	2.0 0	2.5 0.5	V V
PA enable current	I_{ENABLE}		1	12	μA
Operating frequency	F	1800		1900	MHz
Operating temperature	T_C	-40	+25	+85	°C

Table 5. Electrical Specifications¹

($V_{CC1} = V_{CC2} = V_{CC3} = V_{BIAS} = 5\text{ V}$, $P_{AEN} = 2.0\text{ V}$, $f = 1842.5\text{ MHz}$, $T_C = +25\text{ }^\circ\text{C}$, Input/Output Load = $50\ \Omega$, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		1800		1900	MHz
Small signal gain	S21	$P_{IN} = -30\text{ dBm}$	33	35		dB
Gain @ +28 dBm	S21 @+28dBm	$P_{OUT} = +28\text{ dBm}$	34.8	36		dB
Input return loss	S11	$P_{IN} = -20\text{ dBm}$	11	16		dB
Output return loss	S22	$P_{IN} = -20\text{ dBm}$	10	12		dB
Reverse isolation ²	S12	$P_{IN} = -30\text{ dBm}$		50		dB
ACLR @ +28 dBm	ACLR	$P_{OUT} = +28\text{ dBm}$ (40 MHz LTE, 8.5 dB PAR signal)		-31	-27.5	dBc
Saturated output power	Psat	CW, $P_{IN} = +5\text{ dBm}$		+35		dBm
Output power at 3 dB gain compression	P3dB	CW, reference to small signal gain ($P_{IN} = -30\text{ dBm}$)	+34.5	+36		dBm
Second harmonic	2fo	CW, $P_{OUT} = +28\text{ dBm}$		-30	-24	dBc
Third harmonic	3fo	CW, $P_{OUT} = +28\text{ dBm}$		-55	-45	dBc
Power-added efficiency	PAE	CW, $P_{OUT} = +28\text{ dBm}$	31	34.5		%
Quiescent current	Iccq	No RF signal		80		mA

1. Performance is assured only under the conditions listed in this table.
2. Not tested in production. Verified by design.

Typical Performance Characteristics

($V_{CC1} = V_{CC2} = V_{CC3} = V_{BIAS} = 5\text{ V}$, $P_{AEN} = 2.0\text{ V}$, $f = 1842.5\text{ MHz}$, $T_C = +25\text{ }^\circ\text{C}$, Input/Output Load = $50\ \Omega$, Unless Otherwise Noted)

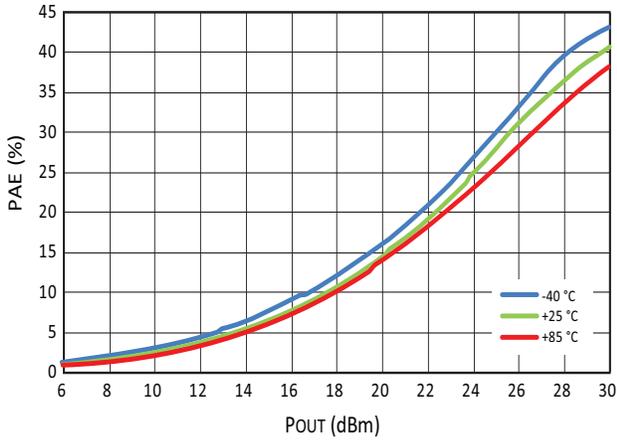


Figure 3. PAE vs. P_{OUT} Across Frequency

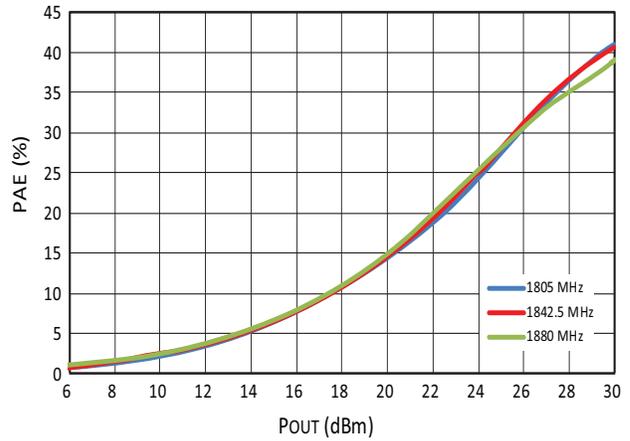


Figure 4. PAE vs. P_{OUT} Across Temperature

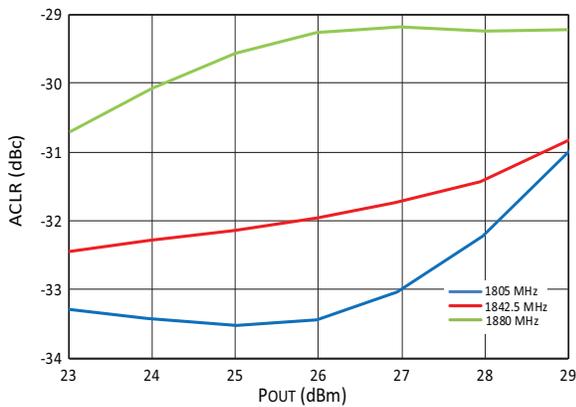


Figure 5. ACLR2 (2x20 MHz) vs. P_{OUT} Across Frequency

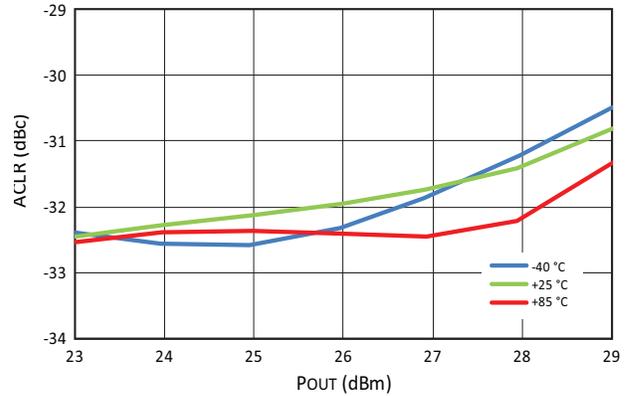


Figure 6. ACLR2 (2x20 MHz) vs. P_{OUT} Across Temperature

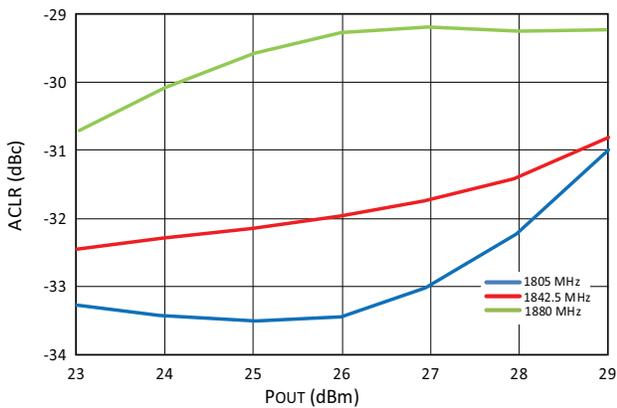


Figure 7. Gain vs. P_{OUT} Across Frequency

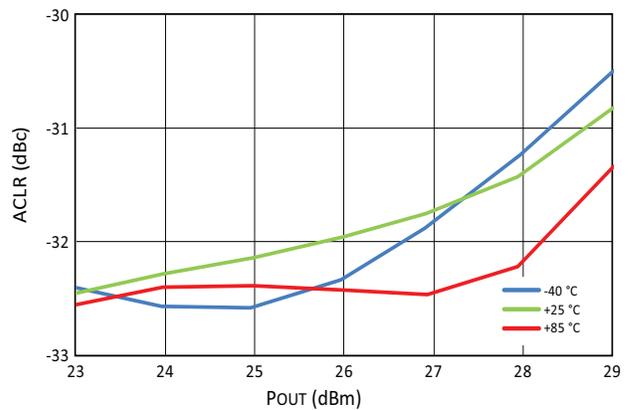


Figure 8. Gain vs. P_{OUT} Across Temperature

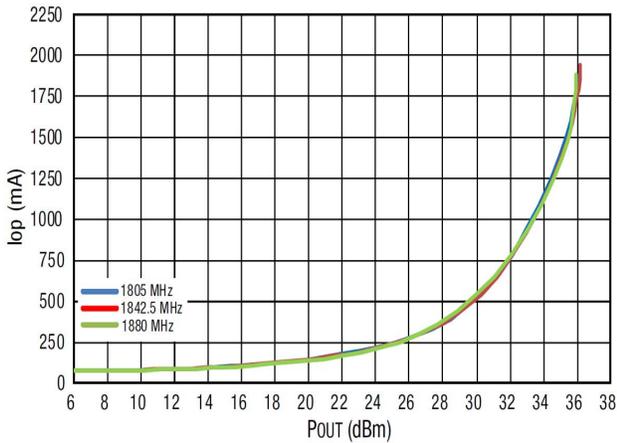


Figure 9. I_{OP} vs. P_{OUT} Across Freq

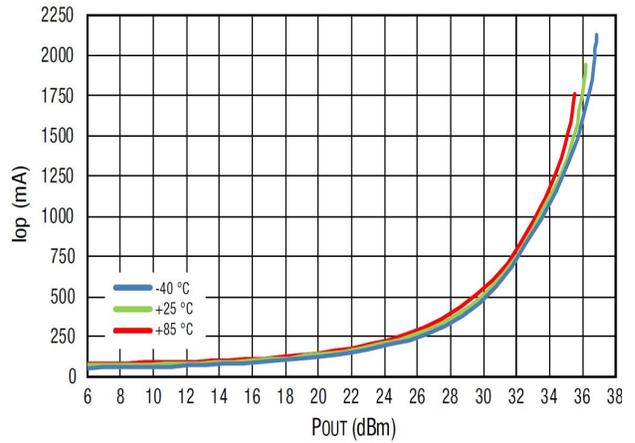


Figure 10. I_{OP} vs. P_{OUT} Across Temp

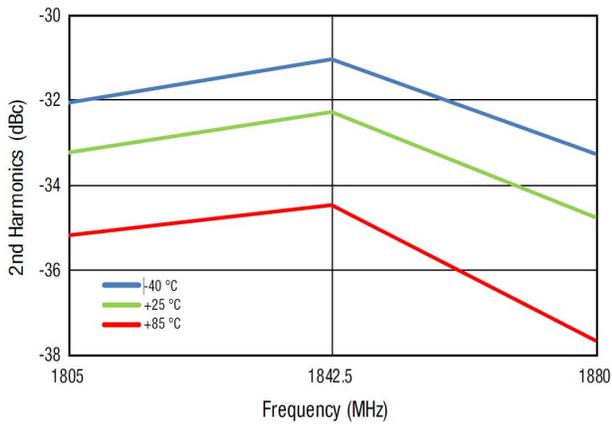


Figure 11. 2nd Harmonic, +28 dBm (CW) vs. Freq Across Temp

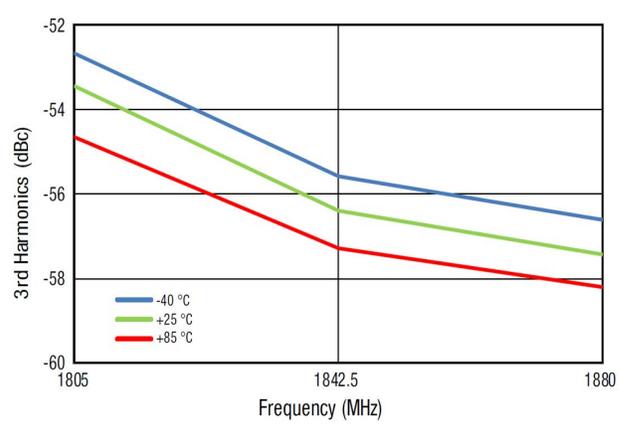


Figure 12. 3rd Harmonic, +28 dBm (CW) vs. Freq Across Temp

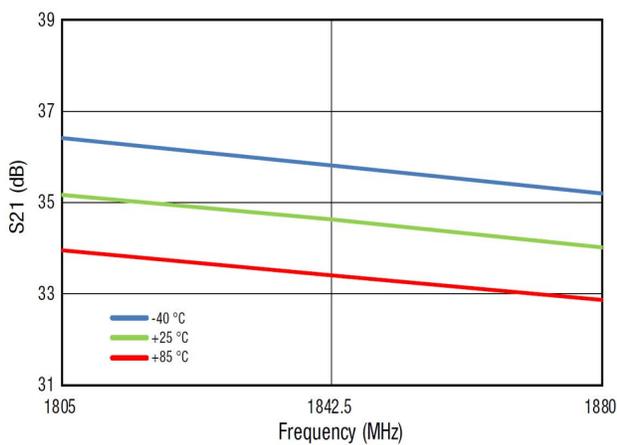


Figure 13. S_{21} vs Freq Across Temp, P_{IN} -20 dBm

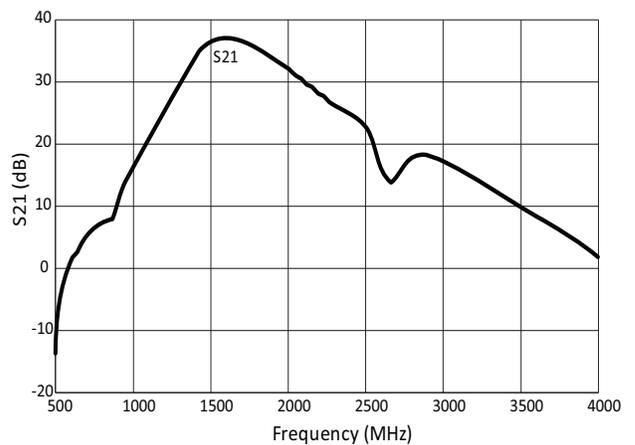


Figure 14. Wide-Band Small Signal Gain vs Freq

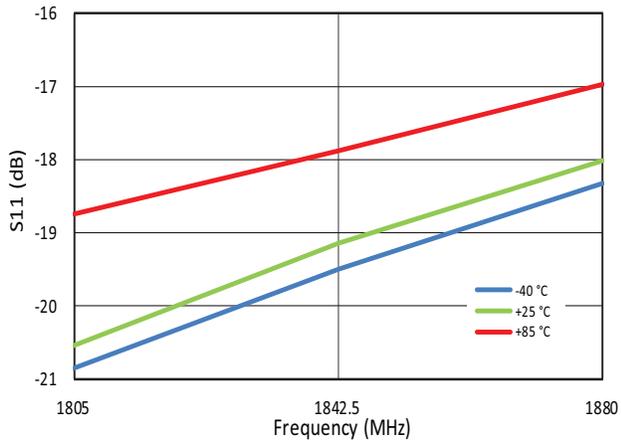


Figure 15. S11 vs. Freq Across Temp, P_{IN} -20 dBm

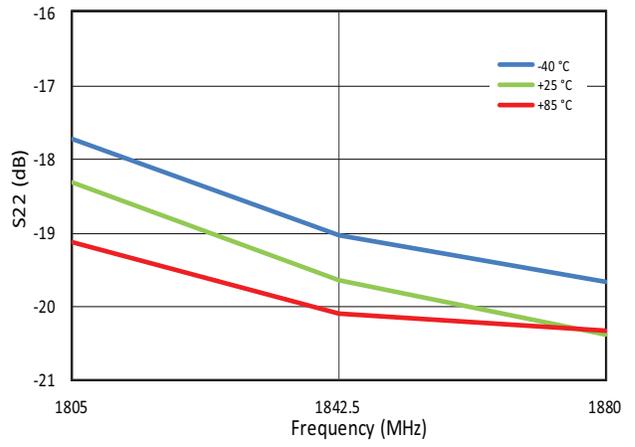


Figure 16. S22 vs. Freq Across Temp, P_{IN} -20 dBm

Evaluation Board

An evaluation board is used to test the performance of the SKY66391-12. A schematic is provided below.

An assembly drawing for the Evaluation Board is shown in Figure 18. Board layer details are shown in Figure 19. Layer detail physical characteristics are noted in Figure 20.

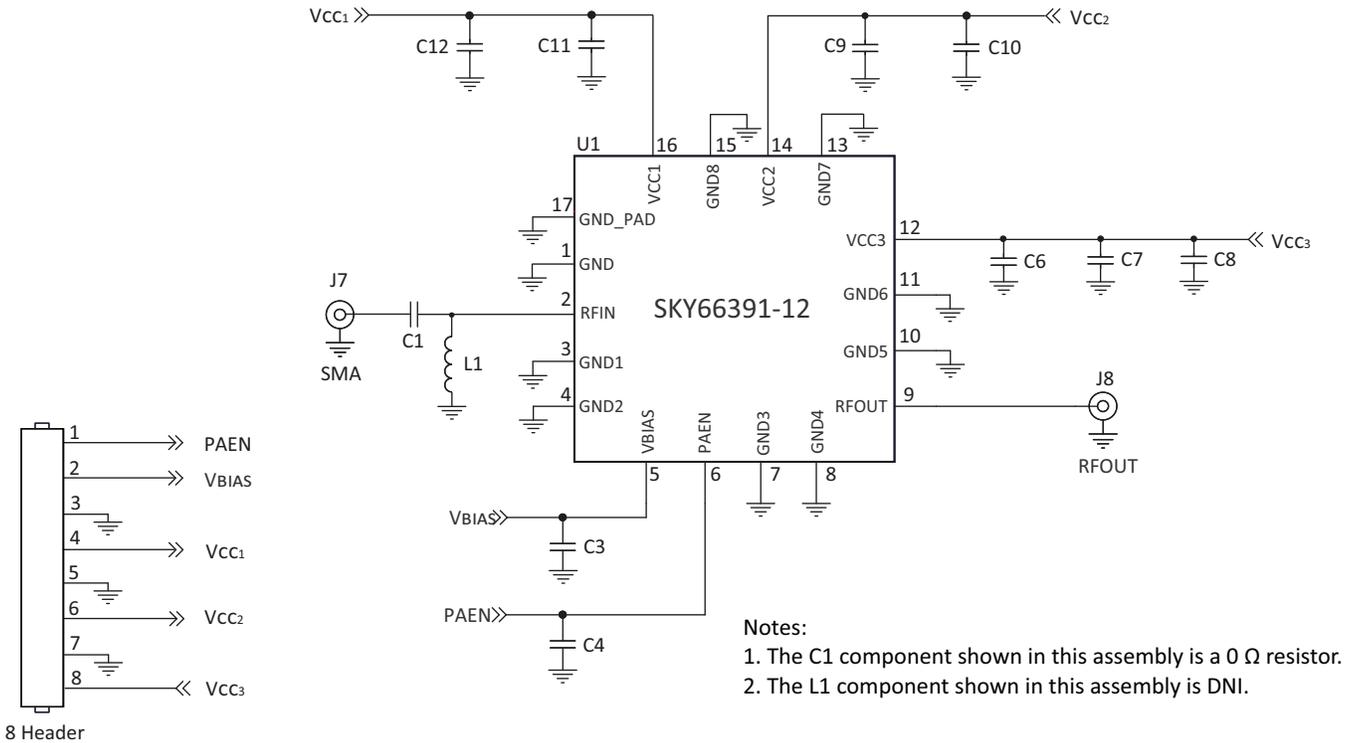


Figure 17. Evaluation Board Schematic

Table 6. Evaluation Board Bill of Materials

Component	Description	Size
C1	Resistor, 0 Ω , 0.063 W	0402
C3	Ceramic capacitor, 1 μ F, \pm 10%, 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, \pm 10%, 50 V	0402
C6, C9, C11	Ceramic capacitor, 0.47 μ F	0402
C8, C10, C12	Ceramic capacitor, 10 μ F, X7R, \pm 10%, 16 V	1206
L1	DNI	
SKY66391-12EK1	Evaluation board	

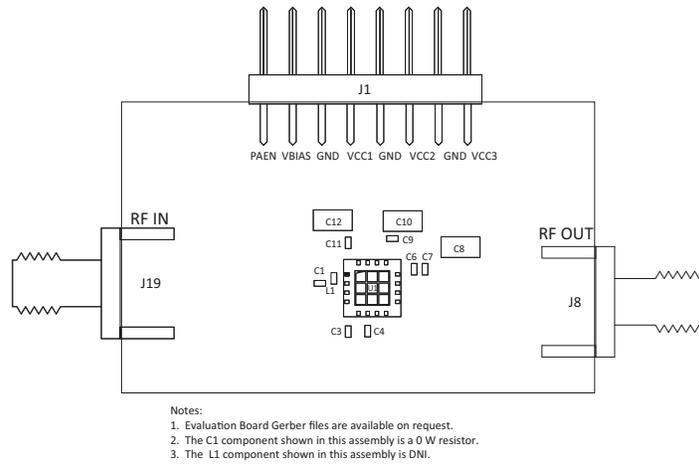


Figure 18. Evaluation Board Assembly Drawing

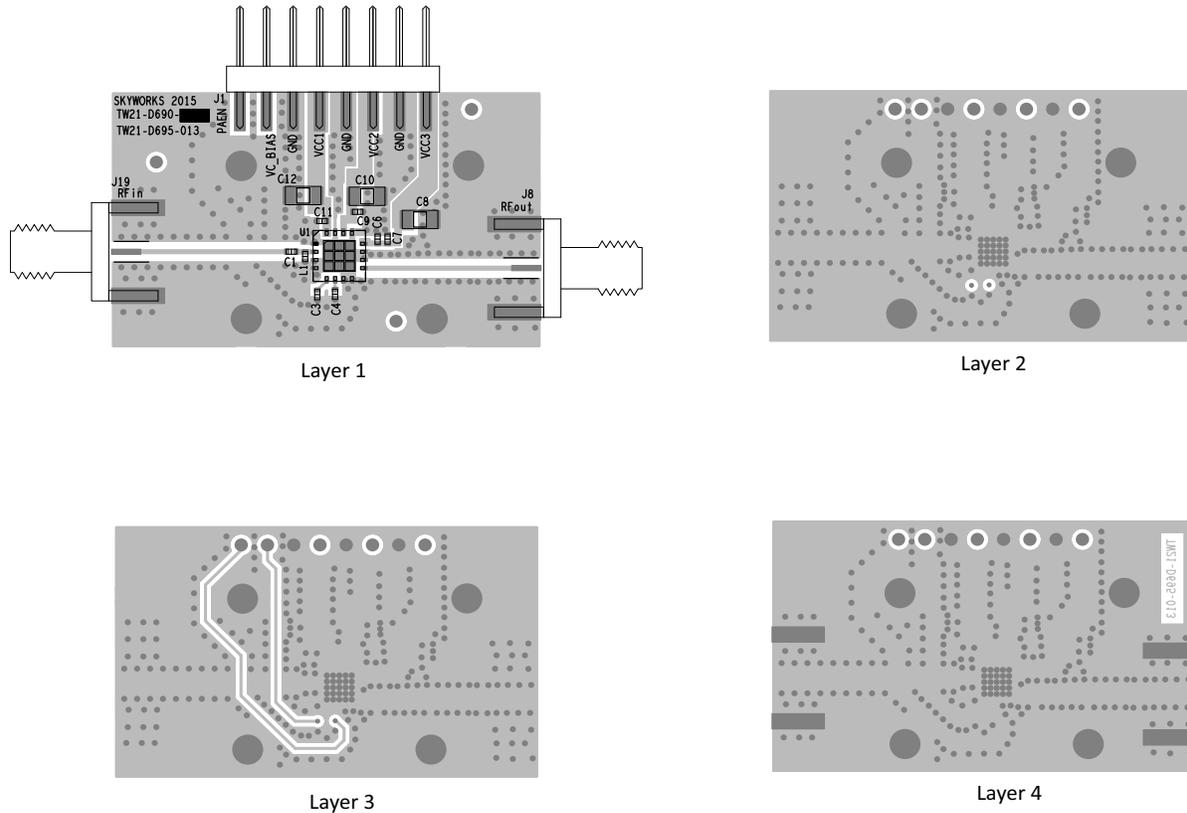


Figure 19. Board Layer Detail

50 Ω	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm 		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

Figure 20. Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for optimum thermal and stability performance. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

GND (pins 1, 3, 4, 7, 8, 10, 11, 13, 15). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via the layout allows. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

VCBIAS (pin 5). The bias supply voltage for each stage, nominally set to +5 V.

RFOUT (pin 9). Amplifier RF output pin ($Z_0 = 50 \Omega$). The module includes an internal dc blocking capacitor. All impedance matching is provided internal to the module.

VCC1, VCC2, and VCC3 (pin 16, 15, 12). Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders, and should be populated with 0Ω resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RFIN (pin 2). Amplifier RF input pin ($Z_0 = 50 \Omega$). All impedance matching is provided internal to the module.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66391-12 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead- or lead-free soldering.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Product production quantities are shipped in a standard tape and reel format.

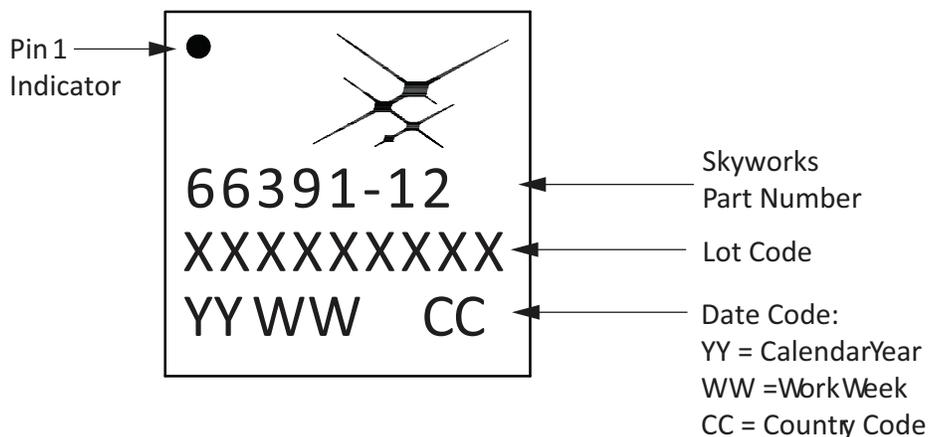


Figure 21. Typical Part Marking

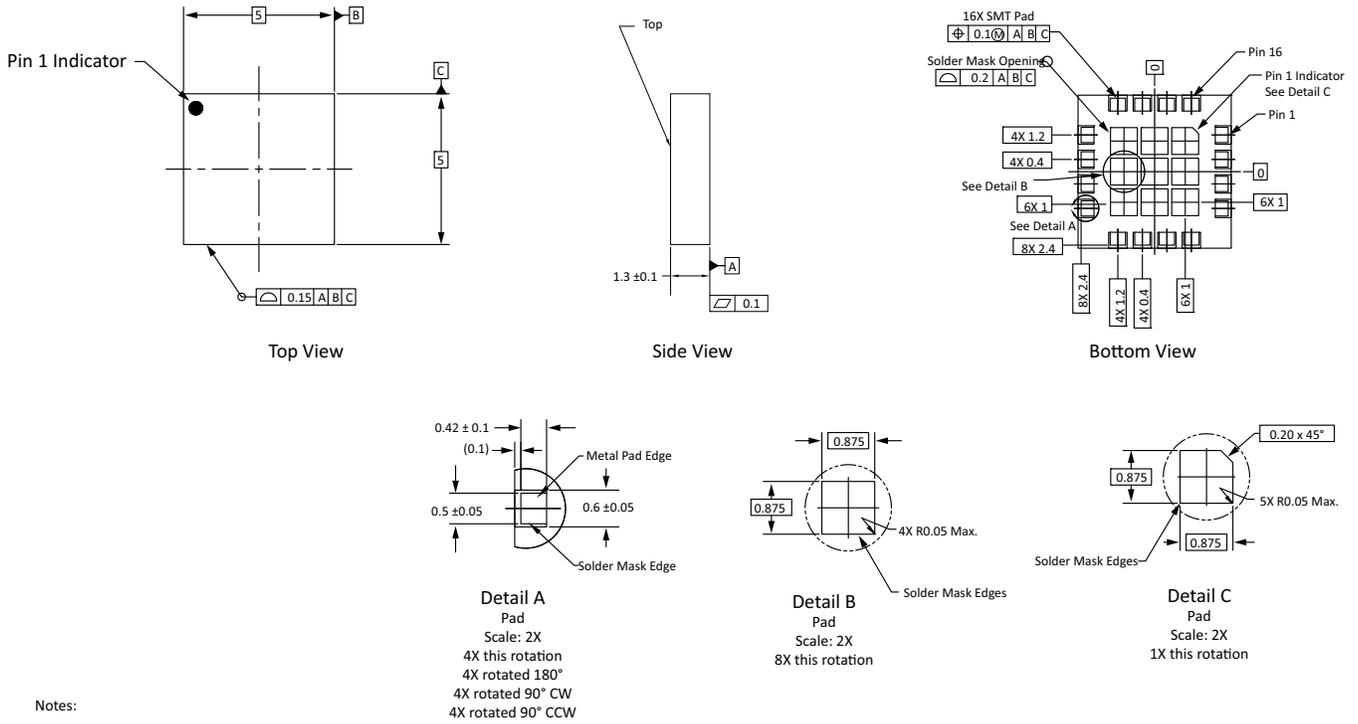
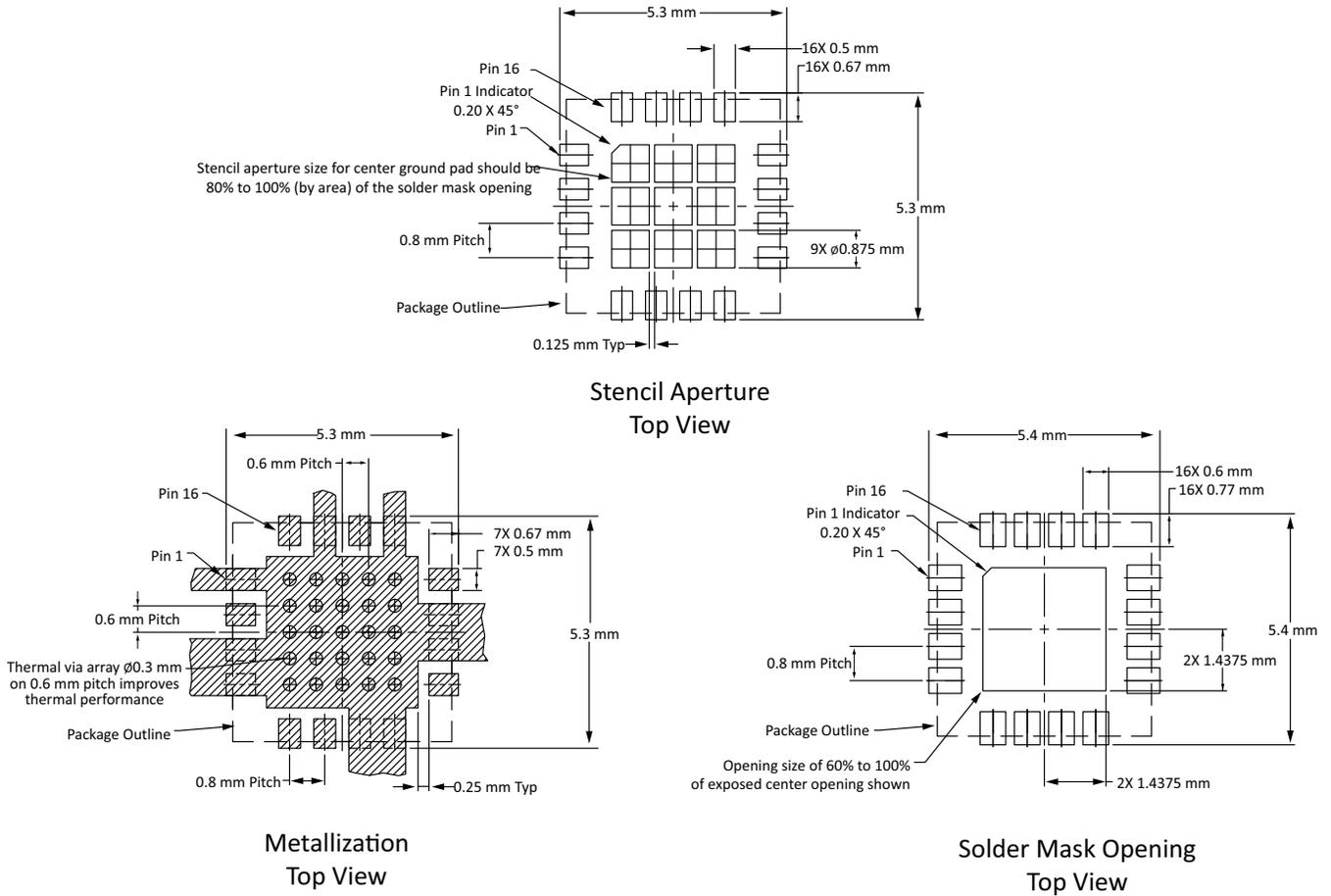


Figure 22. Package Dimensions



Notes:

1. Thermal vias should be resin filled and capped in accordance with IPC-4761 type VII vias.
2. Recommended Cu thickness is 30 to 35 μm.

Figure 23. PCB Layout Footprint

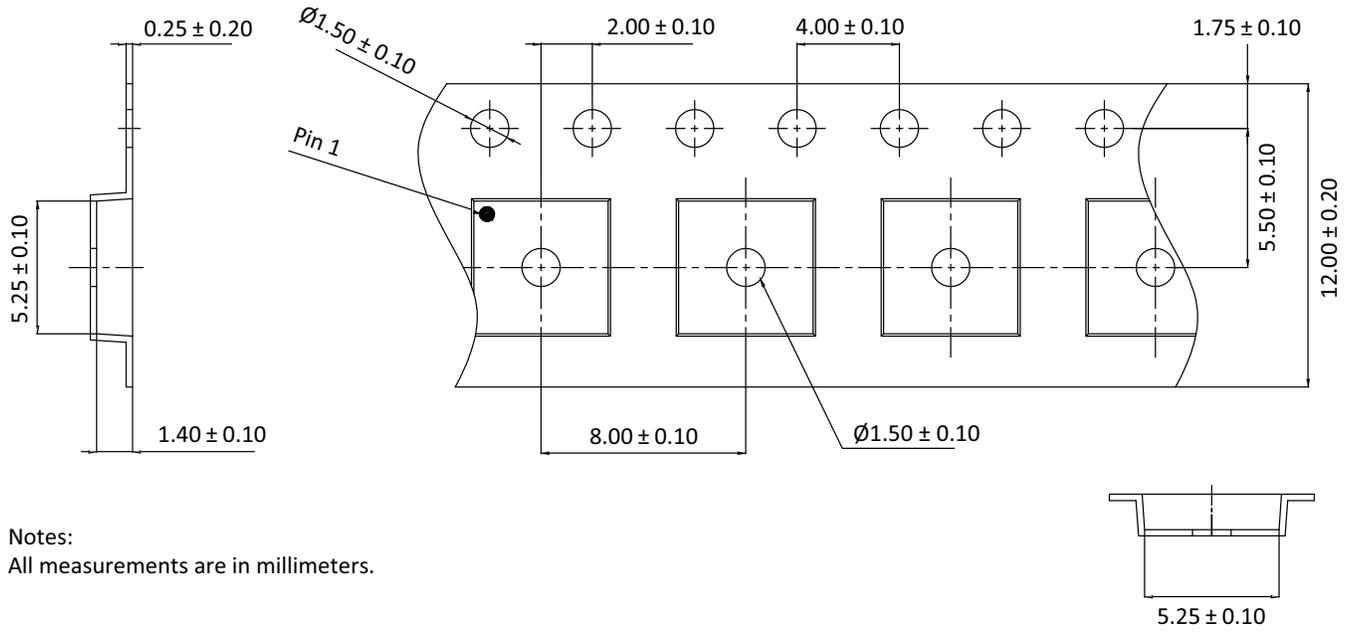


Figure 24. Tape and Reel Information

Ordering Information

Part Number	Description	Evaluation Board Part Number
SKY66391-12	1800 to 1900 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier	SKY66391-12EK1

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