APPLICATION NOTE

# A Wideband CATV Attenuator

## Introduction

In cable TV line amplifiers and set-top applications, a variable attenuator is used in front of an LNA as an AGC. Figure 1 shows a block diagram of a typical transceiver used in a set-top box. The attenuator's purpose is to normalize the level of the high dynamic range multichannel TV signal. The input signal level may vary from 0 to 20 dBmV (-49 to -29 dBm) depending on the local cable network layout and standards. Thus, the attenuator should provide at least 20 dB of low distortion attenuation.

Application note APN1003, *A Wideband General-Purpose PIN Diode Attenuator*, describes a PI attenuator design using four individually packaged SMP1307-011 PIN diodes with coverage from 10 MHz to 3 GHz. This application note describes a four-diode PI-type attenuator specifically designed for CATV applications with coverage to 1 GHz. The benefits of this design are the cost and space savings resulting from the SMP1320-027, a single package, four PIN diode array configured as a PI attenuator in a SOT-5 plastic package.

## PI Attenuator Fundamentals

PIN diode designs are commonly used for matched broadband applications, especially those covering low RF frequencies (to 5 MHz) through frequencies greater than 1 GHz. The most popular circuits are the TEE, bridged TEE and PI configurations. These designs use PIN diodes as current controlled RF resistors whose resistance values are set by a DC control established by an AGC loop.

Figure 2 shows a basic PI attenuator that uses three PIN diodes. It also shows the expressions that determine the resistor values for each PIN diode as a function of attenuation.

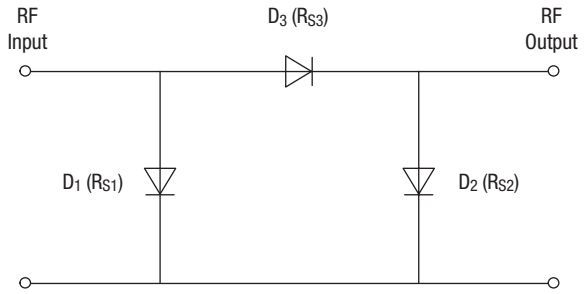



**Figure 2. PI Attenuator**

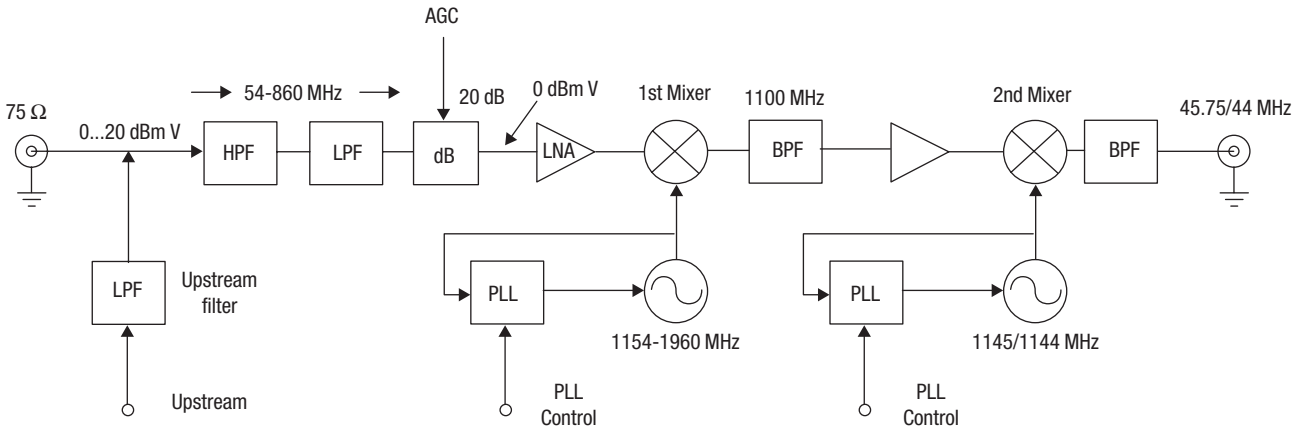



**Figure 1. Block Diagram of Typical Dual-Conversion Cable Transceiver**

Figure 3 displays the value of PIN diode resistance for a 50 Ω PI attenuator. Note that the minimum value for the shunt diodes, $R_1$ and $R_2$, is 50 Ω.

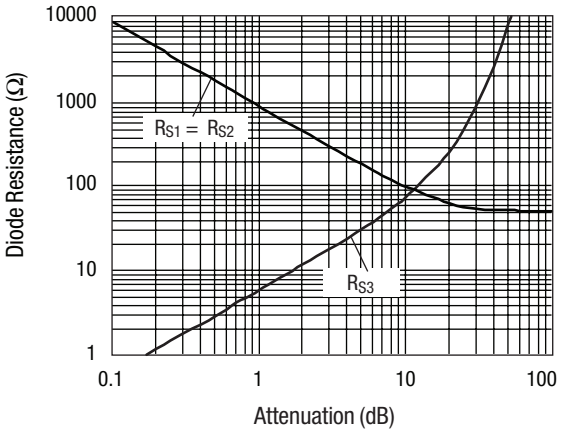



**Figure 3. Attenuation of PI Attenuators**

Figure 4 shows a PI attenuator that uses four PIN diodes and is the subject of this application note. The benefit of the four-diode circuit is that its symmetry allows for a simpler bias network and a reduction of distortion due to cancellation of harmonic signals resulting from the back-to-back configuration of the series connected diodes.

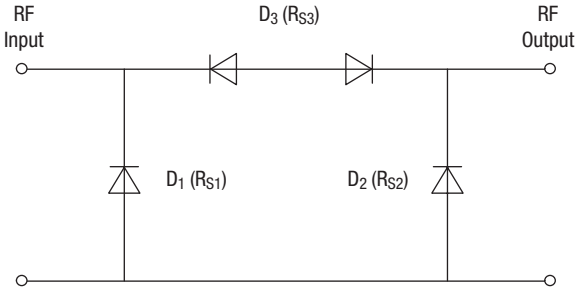



**Figure 4. Four Diode PI Attenuator**

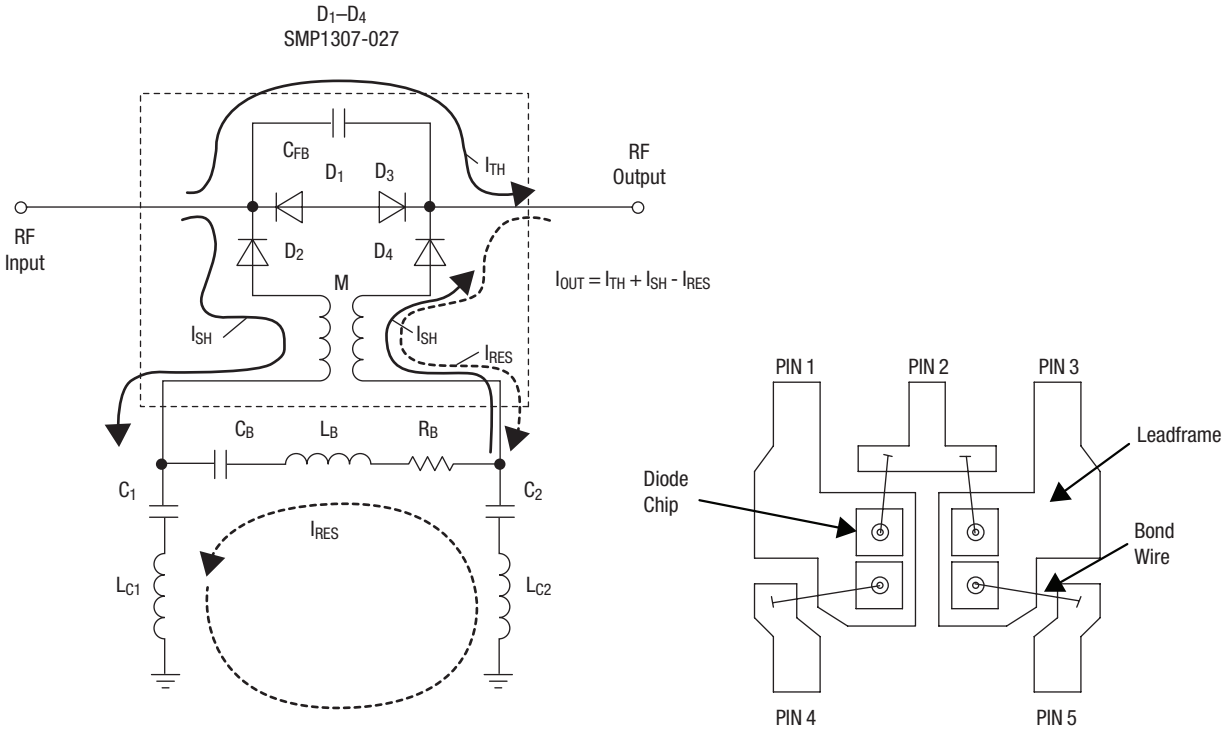



**Figure 5. SOT-5 Package Assembly Couplings**

## SOT-5 Package Assembly Model and Feedthrough Compensation Circuitry

Figure 5 shows the model for the RF couplings that exist within the fourdiode SOT-5 package. The effect of these couplings is most noticeable at high attenuation where the series diodes, $D_1$ and $D_3$, are in a high impedance state, and shunt diodes, $D_2$ and $D_4$, are in a low impedance state. The capacitive coupling between the RF input and output, designated as $C_{FB}$, is the result of the diode junction capacitance (about 0.3 pF) and the inter-terminal package capacitance (about 0.1–0.15 pF). This results in a capacitance of approximately 0.4–0.45 pF. There is also magnetic coupling between the shunt connected diodes, caused by the proximity of bond wires and package leadframe pads, shown as the transformer M. This provides a circulating feed-through current path ($I_{SH}$). Without compensating for these internal couplings, the maximum isolation at 1 GHz was less than 25 dB, compared to greater than 40 dB achieved using separate packaged diodes demonstrated in APN1003.

To improve the high-frequency isolation, a simple and robust compensation circuit was developed, as shown in Figure 5. The compensation circuit requires only one or possibly two additional components and uses existing parasitic components of a PI attenuator. The series connected $C_1$–$L_{C1}$ and $C_2$–$L_{C2}$ are the existing RF ground capacitors with their respective parasitic inductors, $L_{C1}$ and $L_{C2}$. Since the values of $C_1$ and $C_2$ are usually very large at the high-frequency end of the CATV band, they may be neglected. Capacitor $C_B$, a necessary addition for the compensation circuit to work, is represented with its parasitic inductance $L_B$. Resistor $R_B$ represents the loss of capacitors $C_1$, $C_2$, $C_B$ (about 0.6 Ω) which may be added to the compensation circuit if more flatness at the high-frequency response is desired.

Compensation occurs when capacitors $C_1$, $C_2$, $C_B$ resonate with $L_{C1}$ and $L_{C2}$ at a frequency near or above the highest frequency of the band. As shown in Figure 5, a portion of the resonating current component, $I_{RES}$, flows in the opposite direction of the feedthrough currents, $I_{TH} + I_{SH}$, resulting in cancellation when balanced. Resistor $R_B$ may be used to regulate the depth and flatness of the cancellation across the frequency range.

## Attenuator Circuit Model

In the circuit in Figure 6, the PIN diode pairs $X_2/X_4$ and $X_1/X_3$ are symmetrically biased from two DC sources. The reference DC voltage source (5 V) provides adequate biasing to keep shunting diodes $X_3$ and $X_4$ at approximately 75 Ω (for the 75 Ω system analyzed in the case below) during “shut-down” of series diodes $X_1$ and $X_2$. The values of biasing resistors SRL1, SRL2, SRL3, $R_1$, SRL5 and SRL4 were selected to provide minimum VSWR for the whole range of the attenuation changes. Attenuation is controlled by the control voltage source, $V_{CTL}$, which ranges from 1 to 5 V. This source supplies control current to the series diodes $X_1$ and $X_2$ through the wideband high impedance ferrite inductor $X_5$ (FBM H4525, Taiyoyuden) and resistors SRL4, SRL5, and SRL6.

Capacitors SRLC5 and SRLC7 provide RF grounding for the shunt diodes. The separation of the biasing path into two branches, SRL1 and SRL2, reduces RF coupling between input and output. This will affect maximum attenuation, especially at high frequencies, due to the parasitic series inductances.

Capacitors $C_6$ and $C_7$ reflect the total effect of the 50 Ω SMA coaxial connectors used on the test board.

The values of all biasing resistors were optimized for the best SWR performance over the attenuation range. The values of SRL5 and SRL4 were kept as small as possible to ensure maximum forward current for the series diodes $X_1$ and $X_2$ and high enough not to affect insertion loss of the whole attenuator.

Capacitors $C_4$ and $C_5$ reflect the interterminal parasitic capacitive interactions. The effect of magnetic coupling between shunting branches was modeled with coupled microstrip lines CLIN1. Its parameters were established empirically.

The compensation circuitry, consisting of capacitor $C_{BAL}$ (2 pF), was optimized for the highest attenuation at the high end of the band, while keeping frequency response reasonably smooth. Lower values of $C_{BAL}$ improve flatness at the cost of less attenuation at the high-frequency range.

## SMP1307 SPICE Model

The SMP1307-027 is a four-diode assembly specifically designed for PI-type attenuator applications based on the SMP1307 die.

The SMP1307 is a silicon PIN diode with a thick I region (175 μm) and a long carrier lifetime (TL = 1.5 μs). This results in a variable resistance device capable of attenuating frequencies below 10 MHz with low distortion while providing high dynamic range of resistance variation.

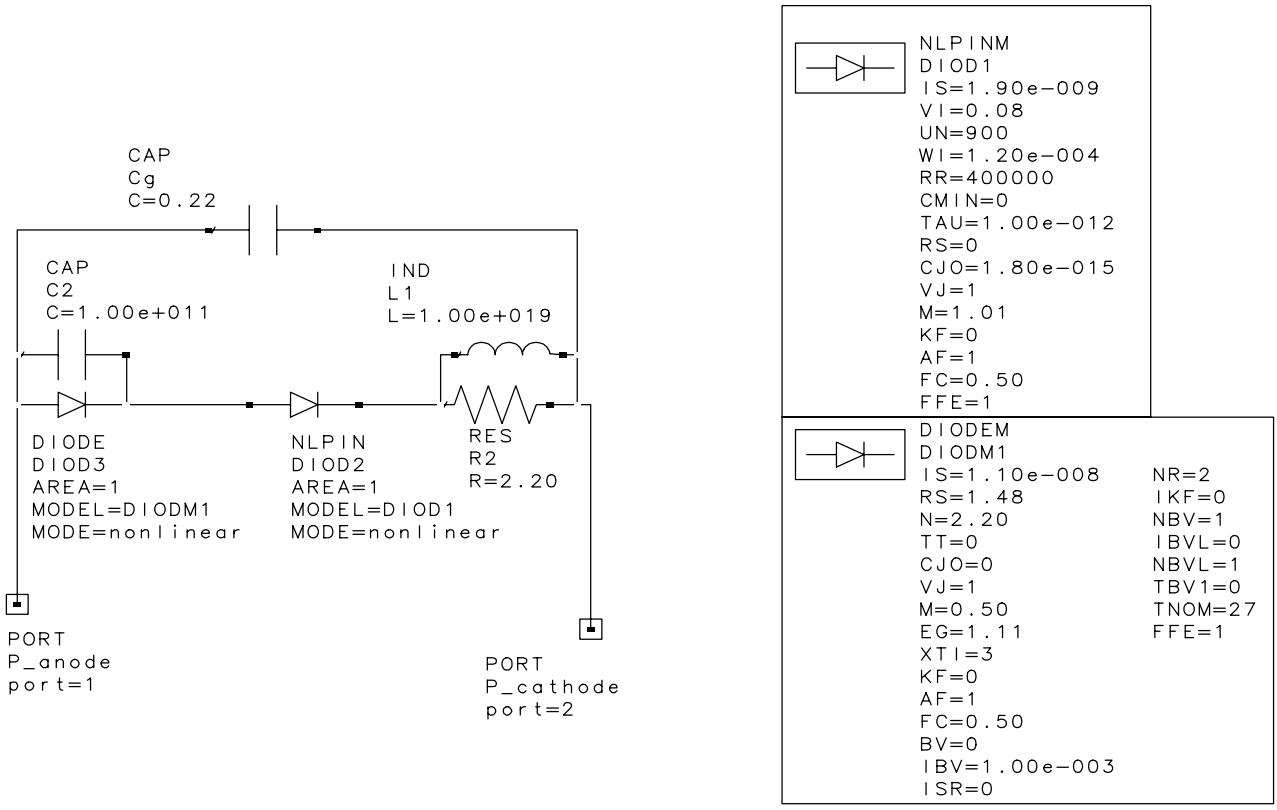



**Figure 6. SMP1307 Model for Libra IV**

The SPICE model for the SMP1307-011 varactor diode defined for the Libra IV environment is shown in Figure 7, with a description of the parameters employed. In this model, two diodes were used to fit both the DC and RF properties of the PIN diode. The built-in PIN diode model of Libra IV was used to model behavior of RF resistance vs. DC current. The P-N junction diode model was used to model DC voltage-current response. Both diodes were connected in series to ensure the same current flow, while the PN-junction diode was effectively RF short-circuited with capacitor $C_2$ = 1E11 pF. The portion of the RF resistance, reflecting residual series resistance, was modeled with $R_2$ = 2.2 Ω, which was shunted with the ideal inductor $L_1$ = 1E19 nH to avoid affecting DC performance. Capacitors $C_G$, $C_P$ and inductor $L_2$ reflect junction and mounting properties of the SMP1307 die.

This is a linear model emulating the DC and RF properties of the PIN diode when the signal frequency is higher than 0.0425 MHz. For more details on the properties of the PIN diode, see Reference 1.

Tables 1 and 2 describe the model parameters. Default values are shown that are appropriate for silicon PIN diodes that may be used by the Libra IV simulator. Some built-in Libra IV PIN diode values were not used. They are marked “not used” in the tables.

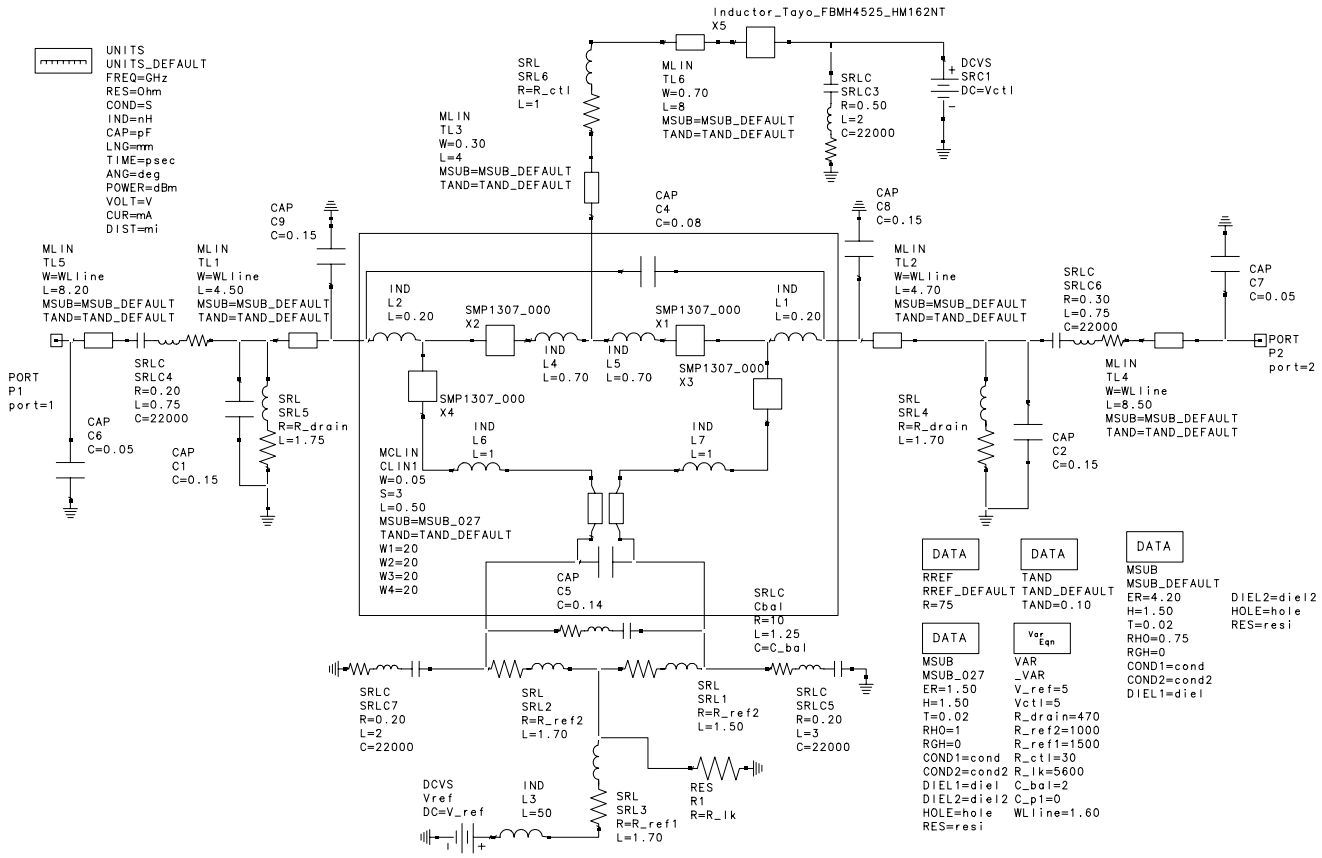



**Figure 7. Libra IV CATV/Modem PIN Attenuator Model**

| Parameter | Description | Unit | Default |
|---|---|---|---|
| $I_S$ | Saturation current (not used) | A | 1.9E-9 |
| $V_I$ | I region forward bias voltage drop | V | 0.08 |
| UN | Electron mobility cm**2/(V*S) (not used) | cm**2/(V*S) | 900 |
| WI | I region width (not used) | M | 1.2e-4 |
| $R_R$ | I region reverse bias resistance | Ω | 4E5 |
| $C_{MIN}$ | PIN punchthrough capacitance | F | 0 |
| TAU | Ambipolar lifetime within I region (not used) | S | 1E-12 |
| $R_S$ | Ohmic resistance | Ω | 0 |
| $C_{J0}$ | Zero-bias junction capacitance | F | 1.8E-15 |
| $V_J$ | Junction potential | V | 1 |
| M | Grading coefficient | - | 1.01 |
| KF | Flicker noise coefficient (Not used) | - | 0 |
| AF | Flicker noise exponent (Not used) | - | 1 |
| FC | Coefficient for forward-bias depletion capacitance (not used) | - | 0.5 |
| FFE | Flicker noise frequency exponent (not used) | - | 1 |

**Table 1. Silicon PIN Diode Values in Libra IV (Assumed for SMP1307 Model)**

| Parameter | Description | Unit | Default |
|---|---|---|---|
| $I_S$ | Saturation current | A | 1.1E-8 |
| $R_S$ | Series resistance | Ω | 1.48 |
| N | Emission coefficient (not used) | - | 2.2 |
| TT | Transit time (not used) | S | 0 |
| $C_{JO}$ | Zero-bias junction capacitance (not used) | F | 0 |
| $V_J$ | Junction potential (not used) | V | 1 |
| M | Grading coefficient (not used) | - | 0.5 |
| EG | Energy gap (with XTI, helps define the dependence of IS on temperature) | EV | 1.11 |
| XTI | Saturation current temperature exponent (with EG, helps define the dependence of IS on temperature) | - | 3 |
| KF | Flicker noise coefficient (not used) | - | 0 |
| AF | Flicker noise exponent (not used) | - | 1 |
| FC | Forward bias depletion capacitance coefficient (not used) | - | 0.5 |
| $B_V$ | Reverse breakdown voltage (not used) | V | Infinity |
| $I_{BV}$ | Current at reverse breakdown voltage (not used) | A | 1e-3 |
| ISR | Recombination current parameter (not used) | A | 0 |
| NR | Emission coefficient for ISR (not used) | - | 0 |
| IKF | High injection knee current (not used) | A | Infinity |
| NBV | Reverse breakdown ideality factor (not used) | - | 1 |
| IBVL | Low-level reverse breakdown knee current (not used) | A | 0 |
| NBVL | Low-level reverse breakdown ideality factor (not used) | - | 1 |
| $T_{NOM}$ | Nominal ambient temperature at which these model parameters were derived | ÞC | 27 |
| $F_{FE}$ | Flicker noise frequency exponent (not used) | | 1 |

**Table 2. Silicon Diode Values in Libra IV (Assumed for SMP1307 Model)**

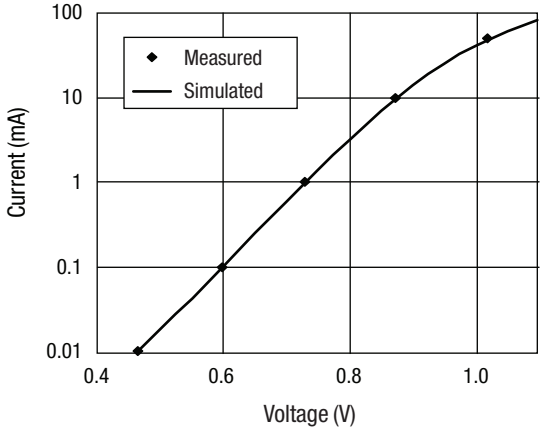



**Figure 8a. DC Current-Voltage Response of SMP1307**

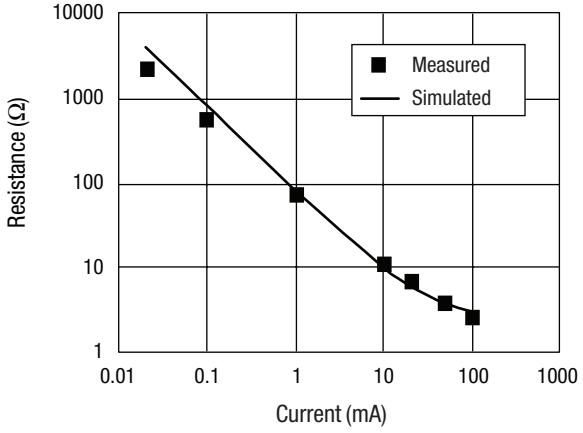



**Figure 8b. RF Resistance vs. Current for SMP1307**

The model DC voltage-current response calculated by Libra IV is shown in Figure 8a, with the measured data. It shows very good compliance of our model's DC properties with measured results. Figure 8b shows internal RF resistance with the parasitic capacitors $C_G$, $C_P$ and inductor $L_2$ unembedded.

## Attenuator Design, Materials, Layout and Performance

Both 50 and 75 Ω versions of the four-diode PIN attenuator were designed and tested. The schematic diagram is shown in Figure 9 with values for the 75 Ω design; the 50 Ω design schematic differs only by the value of $R_5$ (= 560 Ω).

The 50 Ω PCB layout shown in Figure 10a was designed for the 0402 size components, and the 75 Ω PCB layout shown in Figure 10b was designed for the 0805 size components. The boards are made of standard FR4 material, 62 mil thick for both the 50 Ω and 75 Ω versions.

Table 3 lists the bill of materials based on the 0402 size components.

The major difference between the 50 Ω and 75 Ω PCB design is the width of the main throughline. A remarkable fact about this design is that to minimize return loss of the attenuator at the higher frequencies of the CATV band (especially in the lowest attenuation modes), the width of the main throughline is made smaller than required for the matching characteristic impedance of the input/output system. Thus, the optimum width for the 50 Ω version is about 1.5 mm (60 mils), and about 0.8 mm (32 mils) for the 75 Ω version. The thinner lines introduce some inductance, which help compensate for the miscellaneous parasitic capacitance resulting from the numerous pads and discontinuities.

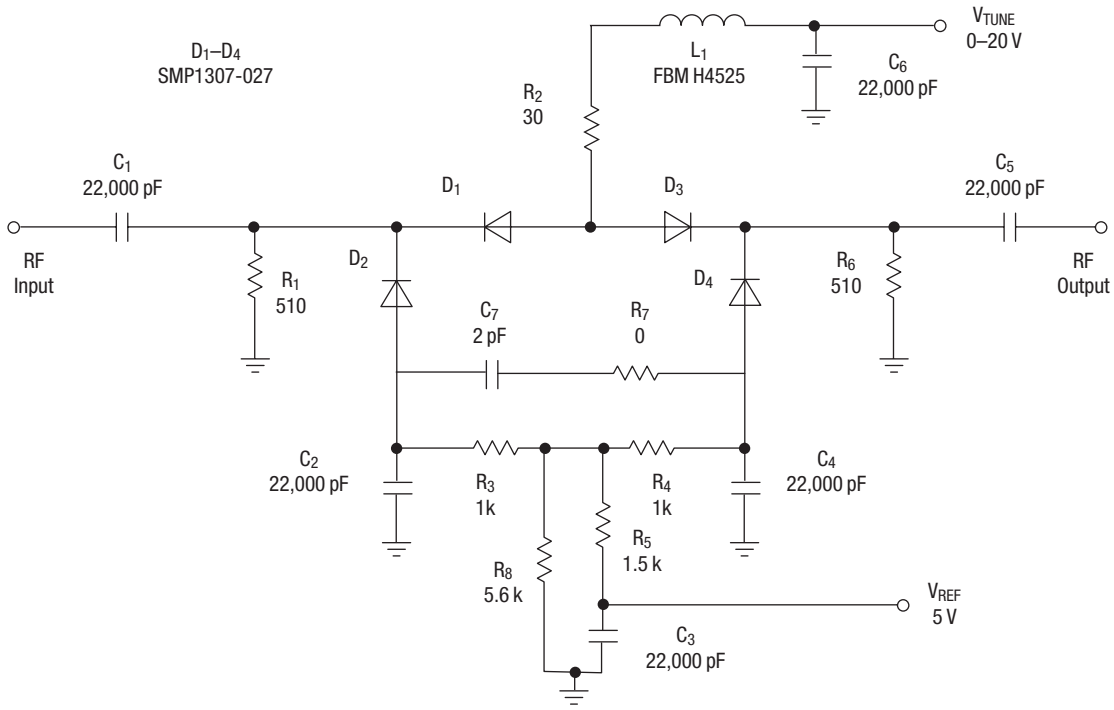
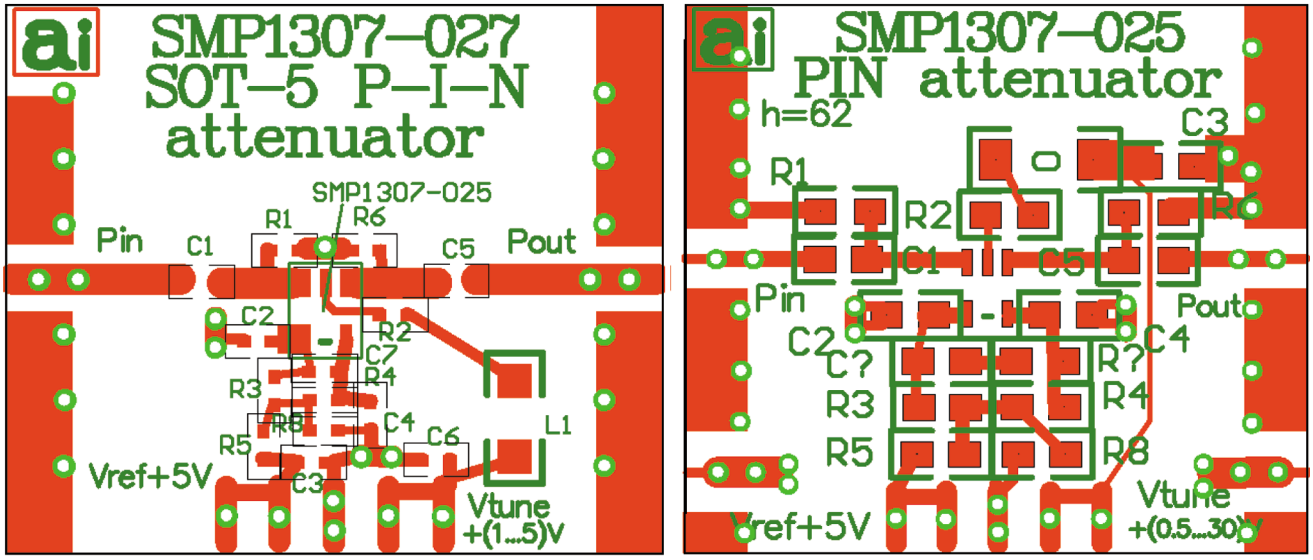



**Figure 9. CATV/Modem PIN Attenuator Schematic Diagram (75 Ω Design)**

| Designator | Value | Part Number | Footprint | Manufacturer |
|---|---|---|---|---|
| $C_1$ | 22,000 p | CM05CG223K10AB | 0402 | AVX/KYOCERA |
| $C_2$ | 22,000 p | CM05CG223K10AB | 0402 | AVX/KYOCERA |
| $C_3$ | 22,000 p | CM05CG223K10AB | 0402 | AVX/KYOCERA |
| $C_4$ | 22,000 p | CM05CG223K10AB | 0402 | AVX/KYOCERA |
| $C_5$ | 22,000 p | CM05CG223K10AB | 0402 | AVX/KYOCERA |
| $C_6$ | 22,000 p | CM05CG223K10AB | 0402 | AVX/KYOCERA |
| $C_7$ | 2 p | CM05CG2R0K10AB | 0402 | AVX/KYOCERA |
| $D_1$–$D_4$ | SMP1307-027 | SMP1307-027 | SOT-5 | Skyworks Solutions |
| $L_1$ | FBMH4525 | FBMH4525_HM162NT | 1810 | TAIYO-YUDEN |
| $R_1$ | 510 | CR05-511J-T | 0402 | AVX |
| $R_2$ | 30 | CR05-300J-T | 0402 | AVX |
| $R_3$ | 1 k | CR05-102J-T | 0402 | AVX |
| $R_4$ | 1 k | CR05-102J-T | 0402 | AVX |
| $R_5$ | 1.5 k | CR05-102J-T | 0402 | AVX |
| $R_6$ | 510 | CR05-511J-T | 0402 | AVX |
| $R_7$ | Optional | Optional | 0402 | AVX |
| $R_8$ | 5.6 k | CR05-562J-T | 0402 | AVX |

**Table 3. Attenuator Bill of Materials**




**10a** **10b**

**Figures 10a and 10b. PCB Layouts for 50 and 75 Ω CATV/Modem PIN Attenuator**

The measured and simulated results are shown in Figures 11 through 13. Figures 11 and 12 show measured results and simulated performances for the 50 Ω attenuator using 0402 size components. Figure 13 shows measured results for the 75 Ω attenuator using 0805 size components.

For attenuation less than 15 dB, shown in Figure 11, flatness of ±1 dB up to 900 MHz was demonstrated. Attenuation starts to increase faster at higher frequencies as the control voltage drops below 1.5 V. This occurs partially due to the effect of the correction circuit.

The correction circuit ($C_7/R_7$) for the 50 Ω design consisted of $C_7$ = 2 pF and $R_7$ = 20 Ω. For the 75 Ω design, where $C_7$ = 1.6 pF and $R_7$ = 50 Ω, the effect was substantially subdued to improve the frequency response smoothness. As a result, the high-frequency insertion loss response in Figure 13 doesn't show the characteristic "dip" observed in Figures 11 and 12, where the compensation circuit effect is much stronger. As a result, the attenuation flatness stays within ±2 dB to the 30 dB range.

The input SWR shown in Figures 11 and 12 show some deterioration in the low-frequency area, which is the result of optimization to benefit the higher frequency end. However, that balance could be easily changed by trimming either the reference voltage or the value of the resistor $R_5$. In Figure 11, the SWR for the 50 Ω attenuator was kept well below 1.6. The SWR for the 75 Ω attenuator was higher, but still below 2. The cause for the 75 Ω system degradation was the integrated effect of multiple parasitic capacitances from the component's pad placement, biasing lines, etc. Also, reducing the overall transmission line width to 0.8 mm would significantly improve the return loss performance.

A comparison of the simulated and measured curves shows that the model is able to accurately predict attenuator performance. There is a discrepancy of approximately 0.1 V in the vicinity of 1 V control voltages. However, this uncertainty may be neglected because in most CATV/modem set-top applications, the attenuator is part of a closed loop level control.

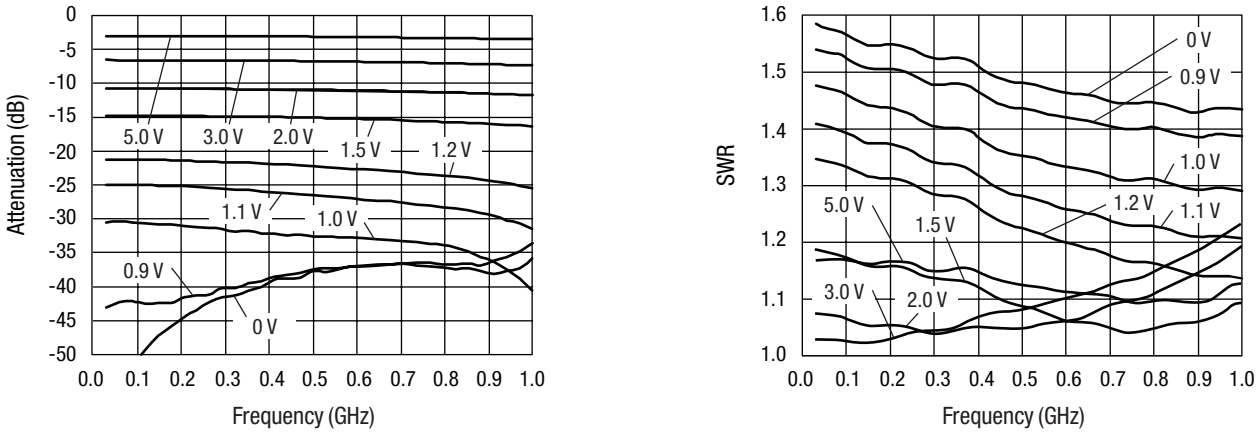



**Figure 11. Measured Insertion Loss and SWR for 50 Ω Attenuator**

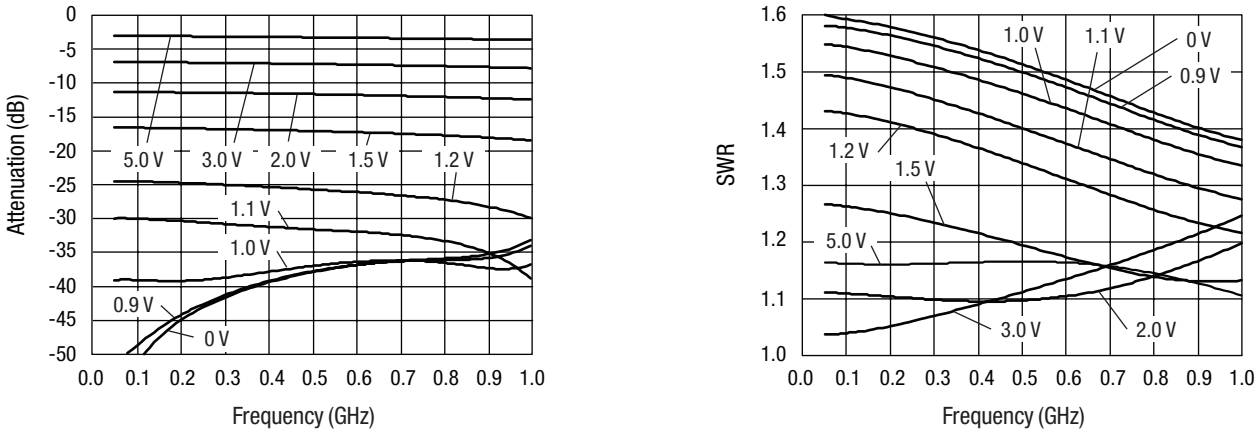



**Figure 12. Simulated Insertion Loss and SWR for 50 Ω Attenuator**

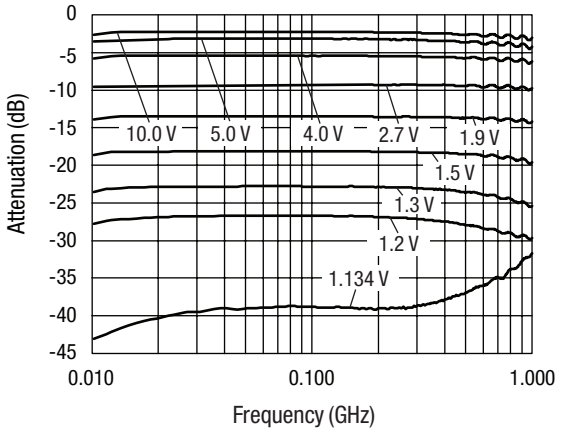



**Figure 13. Measured Insertion Loss for 75 Ω Attenuator**

## Conclusions

A four-diode PI attenuator was designed and constructed in both 50 Ω and 75 Ω environments suitable for CATV service using a single package, SMP1307-27 PIN diode array. The attenuator performed with an attenuation range of greater than 25 dB and with an insertion loss of below 3 dB. The measurements show that for attenuation levels lower than 15 dB, a flatness of better than ±1 dB to 900 MHz was recorded. This performance appears to be consistent with most CATV set-top system requirements.

## References

1. Gerald Hiller, “Design with PIN Diodes,” Application Note, Skyworks Solutions, Inc.
2. Gerald Hiller, “Predict Intercept Points in PIN Diode Switches,” Microwaves & RF, Dec. 1985.
3. Robert Caverly and Gerald Hiller, “Distortion in PIN Diode Control Circuits,” IEEE Trans. Microwave Theory Tech., May 1987.
4. Gerald Hiller and Peter Shveshkeyev, “A Wideband General Purpose PIN Diode Attenuator,” Application Note, Skyworks Solutions, Inc., 1999.
5. Gerald Hiller and Peter Shveshkeyev “5.8 GHz Switch Using Plastic Package PIN Diodes,” Application Note, Skyworks Solutions, Inc., 1999.

## List of Available Documents

1. CATV/Modem PIN Attenuator Simulation Project Files for Libra IV.
2. CATV/Modem PIN Attenuator Circuit Schematic and PCB Layout for Protel, EDA Client, 1998 Version.
3. CATV/Modem PIN Attenuator PCB Gerber Photo-plot Files.

Copyright © 2002, 2003, 2004, 2005, 2006, 2007, 2008, Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of stated published specifications or parameters.

Skyworks, the Skyworks symbol, and "Breakthrough Simplicity" are trademarks or registered trademarks of Skyworks Solutions, Inc., in the United States and other countries. Third-party brands and names are for identification purposes only, and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.