APPLICATION NOTE

AN1452: Si829x ProVCD™ Double-Pulse Test Report

1. Introduction

The rapid electrification of the automotive industry has placed stringent demands on the performance, efficiency, and reliability of EV traction inverters. As a core component in electric powertrains, the traction inverter must operate at high switching frequencies and power levels while maintaining minimal losses and ensuring robust operation under harsh electrical and thermal conditions. Both silicon carbide (SiC) MOSFET and advanced IGBT modules are widely used in this space; SiC devices are used for high-efficiency, high-frequency operation, and IGBTs for are used for cost-effective, high-current applications.

2. Background and Context

While wide bandgap SiC devices offer significant advantages such as lower switching losses and higher temperature capability, they also present challenges due to their extremely fast switching speeds.
High dv/dt and di/dt can lead to voltage overshoot, ringing, EMI, and device stress, particularly in the parasitic-rich environment of traction inverter layouts. Similarly, IGBT modules, though slower, require careful gate control to balance switching loss and transient behavior, especially in high-current automotive applications.

In both cases, the gate driver plays a critical role in achieving optimal system performance. Traditional gate driving approaches typically rely on voltage-mode control, where a fixed gate voltage is applied through an external resistor. While simple, this method provides limited flexibility in shaping the switching transition. Designers are often forced into trade-offs: reducing switching losses by lowering gate resistance can increase overshoot and EMI, while increasing resistance improves robustness at the expense of efficiency, an undesirable compromise in EV systems where both performance and reliability are critical.

To address these challenges, the Skyworks Si829x ProVCD™ (programmable variable current drive) introduces a current-mode gate driving architecture that enables advanced dynamic gate waveform shaping. Unlike conventional voltage-mode drivers, ProVCD™ provides three independently programmable current stages for both turn-on and turn-off transitions, allowing precise control of gate current throughout the entire switching event.
This multi-stage capability enables designers to tailor the gate drive profile to specific operating conditions and device characteristics, optimizing switching performance for both SiC MOSFET and IGBT modules.
In addition, the Si829x ProVCD™ features a high-current output capability of up to 15 A source and sink, providing strong gate driving strength required for high-power traction inverter applications.
Each current stage is independently adjustable from 0 A to 15 A with fine resolution, enabling flexible and granular control of switching behavior. This level of programmability allows designers to effectively balance switching loss, voltage overshoot, and EMI performance without relying on extensive external tuning components. For detailed device specifications and configuration options, refer to the “Si829xx Isolated Safety Gate Drivers” data sheet.

In the context of EV traction inverters, this dynamic gate control offers several important advantages by enabling optimized switching behavior. It helps reduce switching losses, improving overall drivetrain efficiency and contributing to extended driving range. The ability to precisely control dv/dt and di/dt further minimizes electromagnetic interference (EMI) and limits insulation stress within the system. Additionally, the programmable nature of the gate drive provides the flexibility to optimize performance across a wide range of load and temperature conditions, allowing designers to maintain robust and efficient operation under varying real-world scenarios.

3. Report Objective

The objective of this report is to evaluate the impact of the Si829x ProVCD™ compared to conventional voltage-mode gate driving in an EV traction inverter environment. A double-pulse test (DPT) is employed to characterize switching performance under representative operating conditions for both SiC and IGBT modules. The study focuses on a comparative analysis between ProVCD™ and traditional voltage-mode driving (TVMD), with an emphasis on SiC module performance. Key performance metrics include switching energy (E_{ON} and E_{OFF}), voltage overshoot, and waveform ringing.

To provide a comprehensive evaluation, the test results presented in this report are organized into three key areas. First, the impact of ProVCD™ under varying load current conditions (I_{DS}) is examined, highlighting how dynamic gate waveform shaping improves SiC module performance across different current levels compared to TVMD benchmarks. Second, the performance benefits of ProVCD™ are analyzed under varying junction temperature conditions, demonstrating its effectiveness in maintaining optimized switching behavior across a wide temperature range relative to traditional driving methods. Finally, the report evaluates ProVCD™ performance across different SiC modules, illustrating how variations in internal gate resistance influence switching behavior and how ProVCD™ adapts to these differences, as evidenced by comparative DPT results.

By comparing measured results, this report demonstrates how multi-phase dynamic gate control enables improved optimization of switching behavior beyond what is achievable with traditional methods. The findings highlight the value of programmable current-drive techniques in advancing the efficiency, reliability, and robustness of next-generation EV traction inverter systems.

4. Double-Pulse Test Setup

The Wolfspeed® clamped inductive load (CIL) platforms were used to perform the Si829x ProVCD™ versus traditional voltage-mode driving (TVMD) double-pulse tests, enabling evaluation across different SiC module packages. A Skyworks Si829x Gate Driver Board (GDB), which is fully compatible with Wolfspeed CIL platforms, was utilized to drive the SiC modules, specifically targeting a single half-bridge leg during testing. This setup ensures consistent and repeatable switching conditions for accurate performance comparison. The available Wolfspeed CIL platforms and their corresponding power modules used in this study are listed in Table 1 below. Refer to "UG551: Si829x Gate Driver Board (GDB) User Guide" for additional details on the gate driver hardware.

Table 1. Wolfspeed CIL Platforms List

Wolfspeed CIL Platform	Compatible SiC Power Module Family	Tested Power Module P/N
KIT-CRD-CIL12N-XM3	Wolfspeed® XM3	EAB450M12XM3
KIT-CRD-CIL12N-YMC	Wolfspeed® YM3, Infineon® HybridPACK™	ECB2R1M12YM3
KIT-CRD-CIL12N-BM	Wolfspeed® BM3	WAS530M12BM3T
KIT-CRD-CIL12N-FMA	Wolfspeed® FM3	CBB021M12FM3

In this report, the test setup and results are based on the Wolfspeed® XM3 EAB450M12XM3 SiC module in conjunction with the Si829x gate driver (Option 1 package configuration).

Figure 1 below illustrates the overall architecture of the Si829x double-pulse test (DPT) system, including the power stage, gate driver board, control interface, and measurement instrumentation used to capture switching waveforms and key performance parameters. The Si82900CEA-WA-KIT, comprising the Si829x-EAWA-GDB gate driver board, Si829x-CTLR-DC controller card, and user GUI, is used to drive the XM3 half-bridge module. A low-voltage (LV) power supply provides 12 V to the gate driver board. The test PC, running the user GUI, connects to the controller board via a USB interface, enabling communication with the Si829x device and real-time configuration of ProVCD™ parameters.

The Wolfspeed® XM3 module (EAB450M12XM3) is mounted on the CIL platform (KIT-CRD-CIL12N-XM3), which provides the high-voltage and high-current interface. An external high-voltage (HV) DC power supply delivers the dc-link voltage required for the test. An external air-core inductor is included in the power loop to control di/dt during the double-pulse test.

For accurate measurement, two Tektronix® IsoVu™ optically isolated probes are used to monitor the low-side device gate current and gate-source voltage (V_{GS}). A Tektronix THDP0200 high-voltage differential probe is used to measure the drain-source voltage (V_{DS}) of the low-side device. The drain current (I_{DS}) is obtained by measuring the voltage across a current shunt using a high-bandwidth BNC connection.

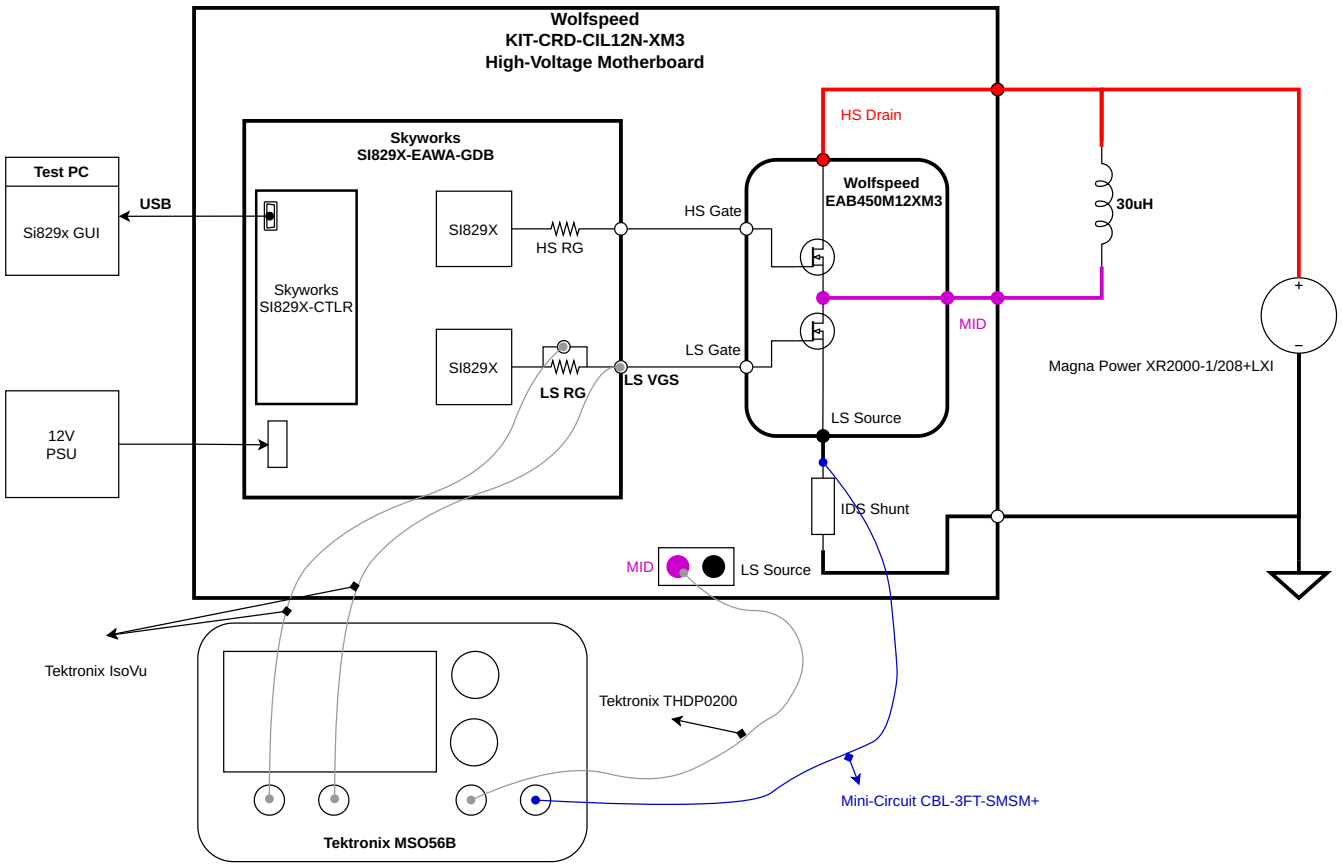


Figure 1. Si829x Double-Pulse Test System Block Diagram

The completed test setup is shown in Figure 2.

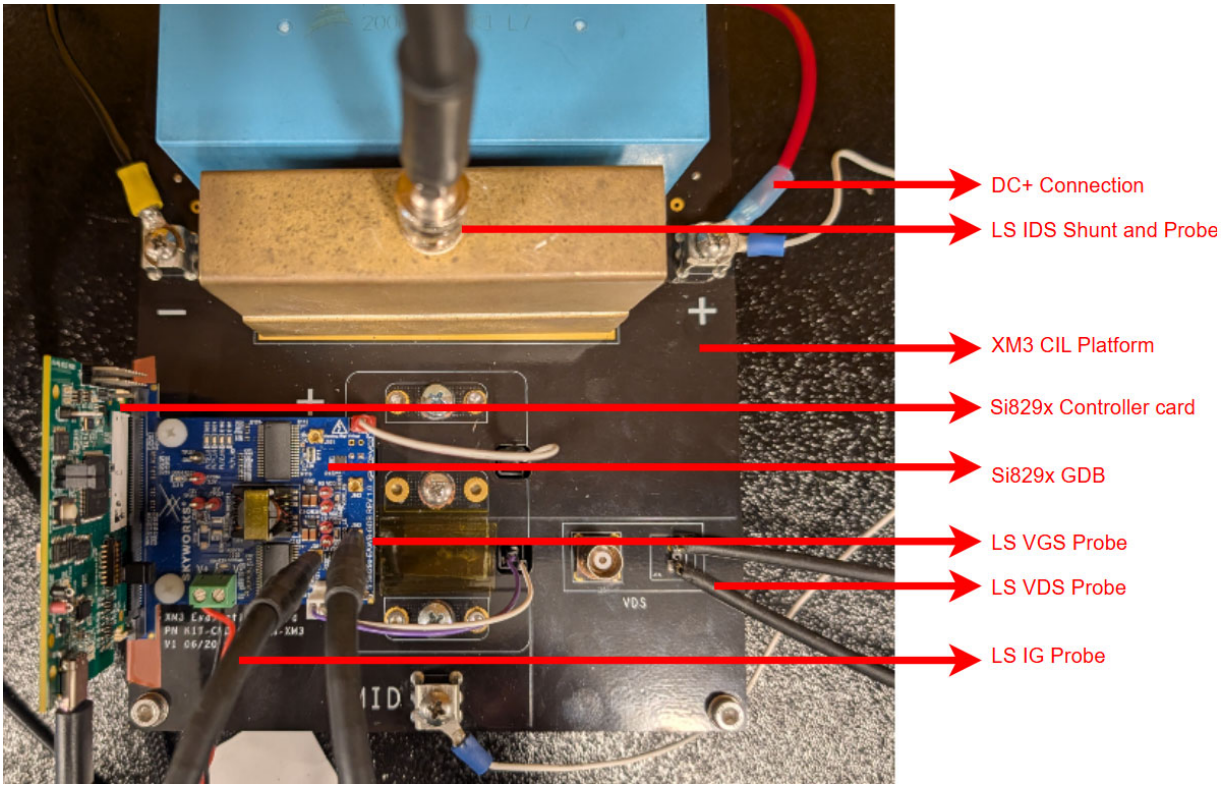


Figure 2. Si829x Double-Pulse Test Setup Top View

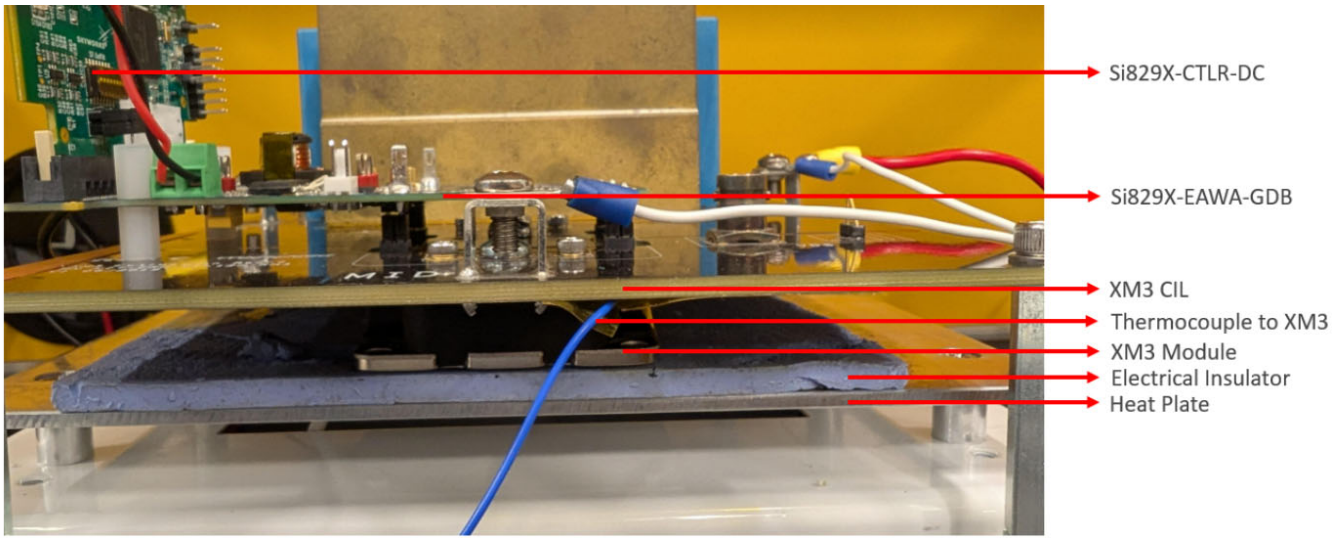


Figure 3. Si829x Double-Pulse Test Setup Front View[1,2]

1.Soak system for three hours to achieve equilibrium temperature condition before DPT data collection.
2.Capture DPT data under 20 °C, 55 °C, 85 °C, 125 °C of the SiC module.

5. Traditional Voltage Mode (TVMD) Benchmark Setup and Test Result

To ensure a fair comparison of Si829x ProVCD™ performance to traditional voltage-mode drive (TVMD) performance, optimized TVMD results are established as the benchmark. This requires careful selection of the turn-on and turn-off gate resistances under worst-case operating conditions to achieve the best possible trade-off between switching loss and transient behavior.

The Si829x device can be readily configured to operate in a TVMD mode, allowing the same hardware platform, including board parasitics and system interconnections, to be maintained across both test conditions. This approach ensures a consistent test environment and enables an accurate, like-for-like comparison between ProVCD™ and TVMD.

In this section, the method for configuring the Si829x into traditional voltage-mode operation is introduced. In addition, the selection criteria for turn-on and turn-off gate resistances used in TVMD are discussed, with a focus on achieving optimal performance under the defined test conditions.

5.1. Configuring the Si829x for TVMD Mode

The Si829x device supports configuration in a TVMD mode, enabling controlled, like-for-like comparisons while maintaining identical test conditions and hardware setup.

To configure the Si829x for voltage-mode operation, the following modifications are applied:

- Short the VOLF pin to the VGREG pin
- Short the VOHF pin to the VDREG pin
- Place external turn-on and turn-off gate resistors ($R_{G(ON)}$ and $R_{G(OFF)}$) between the VO pin and the gate of the power transistor to optimize switching performance under worst-case conditions. For details, see 5.2. “Turn-On Resistor Selection” and 5.3. “Turn-Off Resistor Selection”.

Additionally, the internal drive parameters are set to emulate a constant voltage drive by configuring:

$$I_{ON1} = I_{ON2} = I_{ON3} = I_{OFF1} = I_{OFF2} = I_{OFF3} \text{ to their maximum values}$$

$$T_{ON1} = T_{ON2} = T_{ON3} = T_{OFF1} = T_{OFF2} = T_{OFF3} \text{ to their maximum durations}$$

These settings effectively disable the multistage current-shaping behavior of ProVCD™, allowing the device to operate as a conventional voltage-mode driver while preserving the same system parasitics and layout conditions for accurate performance benchmarking.

5.2. Turn-On Resistor Selection

When optimizing the turn-on gate resistor ($R_{G(ON)}$), the primary limiting factors are typically body diode reverse recovery-induced voltage overshoot and the drain current (I_{DS}) safe operating area (SOA) of the device. It is important to note that the double-pulse test (DPT) is a device-level evaluation method rather than a full system-level test; therefore, EMI-related optimization is not considered in this context.

5.2.1. Body Diode Reverse-Recovery Voltage Overshoot

During fast MOSFET turn-on (i.e., with small $R_{G(ON)}$), the opposing device’s body diode undergoes abrupt reverse recovery, generating a high di/dt transient. This rapid current change excites the parasitic LC network formed by the device junction capacitances and PCB stray inductances, resulting in voltage overshoot and ringing. If the overshoot exceeds the breakdown voltage of the MOSFET or diode, device damage or failure may occur. Increasing $R_{G(ON)}$ reduces the di/dt, thereby mitigating voltage overshoot and improving device robustness.

5.2.2. I_{DS} Safe Operating Area (SOA)

During turn-on, the MOSFET conducts both the load current and the reverse recovery current from the opposing body diode. If $R_{G(ON)}$ is too small, the resulting high di/dt can produce a significant current spike. This peak current may exceed the device's pulsed drain current rating, leading to localized thermal stress and potential violation of the safe operating area (SOA). Sustained operation under such conditions can result in device degradation or failure.

The optimal selection of $R_{G(ON)}$ therefore involves choosing a value that limits both the reverse-recovery-induced voltage overshoot and the peak drain current (I_{DS}) to acceptable levels, ensuring safe operation within the electrical and thermal limits of the device. In practice, the following criteria are typically applied:

- $V_{DS(peak)} < 80\%$ to $90\% \times V_{DS(max)}$
- $I_{DS(peak)} < I_{SOA}$

5.2.3. Benchmark Result

In this XM3 module evaluation, the Wolfspeed EAB450M12XM3 power module is rated for 1200 V blocking voltage and 1100 A pulsed drain current (I_{DS}). The defined worst-case test conditions for this study are V_{DS} = 900 V, I_{DS} = 850 A, and a junction temperature range of 25 °C to 125 °C, representing typical and extreme operating conditions encountered in EV traction inverter applications.

Based on these constraints, the target criteria for tuning the turn-on and turn-off gate resistors ($R_{G(ON)}$) are defined as follows:

- $V_{DS(peak)} < 960$ V to 1080 V
- $I_{DS(peak)} < 1100$ A (within pulsed current and SOA limits)

Through iterative tuning, it was determined that using a gate resistance of 2 Ω for turn-on satisfies these criteria. This configuration effectively balances switching speed and transient control, limiting both voltage overshoot and current spikes while maintaining safe operation within the device's electrical and thermal limits.

The TVMD turn-on benchmark test result are shown in Figure 4 and Figure 5.

- The high-side (HS) V_{DS} overshoot due to the body diode reverse recovery is approximately 934 V. Figure 4 on page 8 shows a turn-on HS body diode voltage overshoot with $R_{G(ON)}$ = 2 Ω.

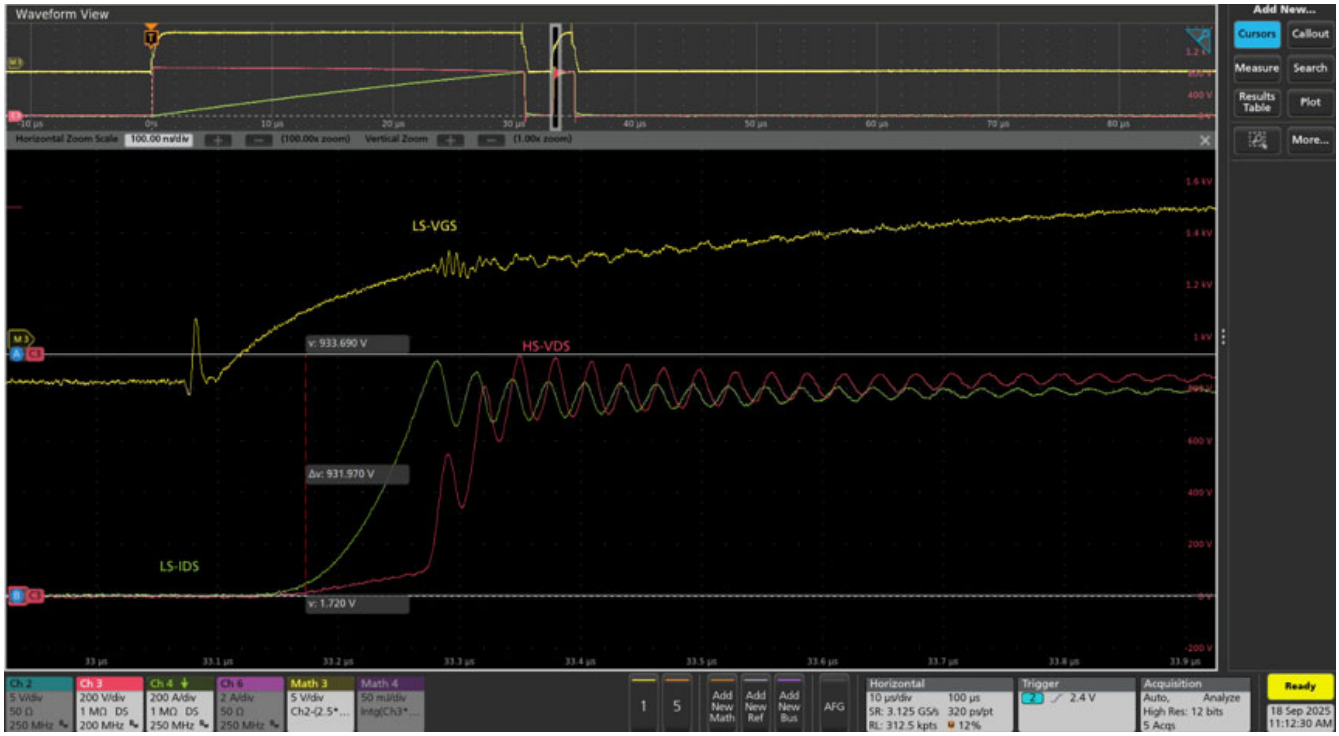


Figure 4. TVMD Turn-On HS V_{DS} Overshoot

- The low-side (LS) I_{DS} current overshot due to the body diode reverse recovery is approximately 1050 A. Figure 5 shows a turn-on switching waveform with $R_{G(ON)}$ = 2 Ω.

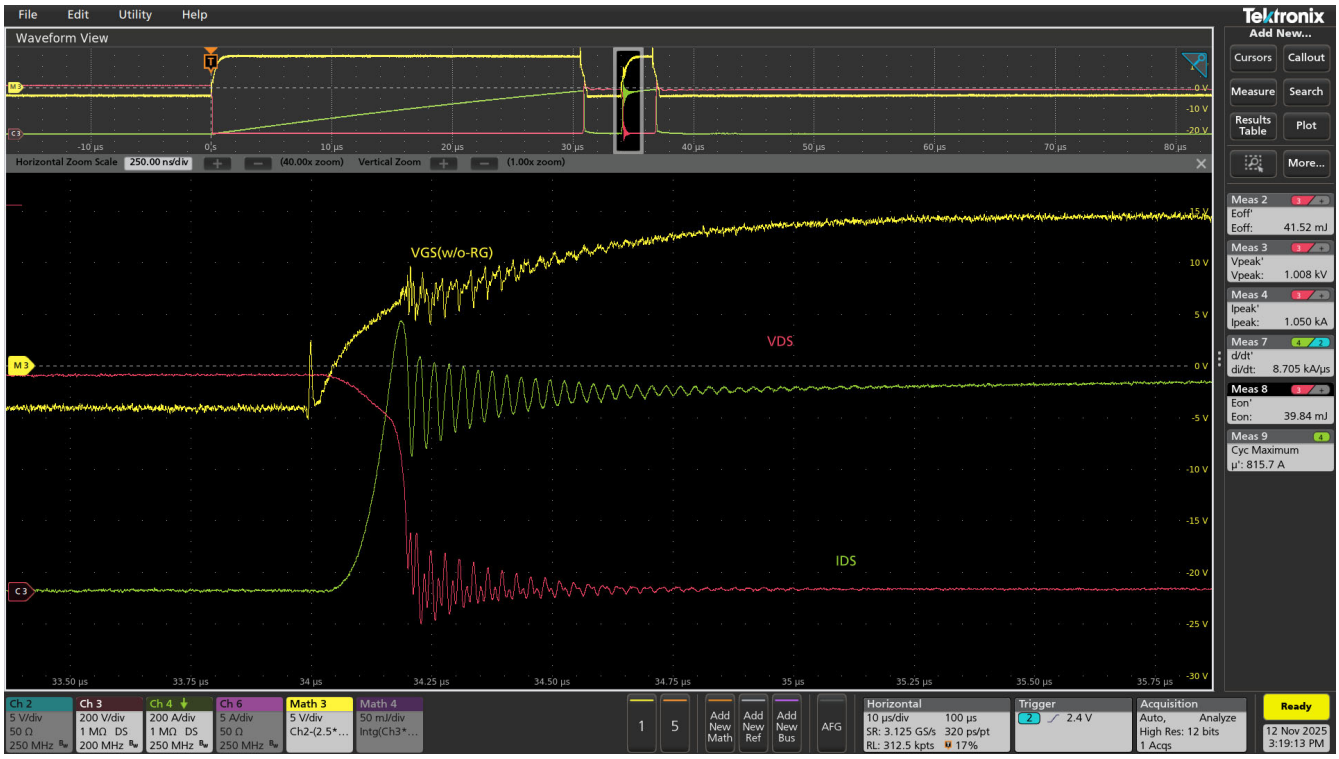


Figure 5. TVMD Turn-On LS I_{DS} Overshoot

Note: *The VGS waveforms in all DPT results are mathematically derived by using:*

$V_{GS(w/o\ RG)} = V_{GS,measured} - I_{G,measured} \times R_{G,internal}$ *(2.5 Ω in this case).*

This equation is used to reflect true V_{GS} voltage at the actual MOSFET gate. The internal parasitic inductance impact is not considered here.

5.3. Turn-Off Resistor Selection

When optimizing the turn-off gate resistor ($R_{G(OFF)}$), the primary limiting factor is typically the drain-source voltage (V_{DS}) overshoot resulting from high di/dt interacting with parasitic inductances in the power loop.

During fast MOSFET turn-off (i.e., with small $R_{G(OFF)}$), the rapid decrease in drain current produces a high di/dt. This transient current, when coupled with stray inductances in the module package and PCB layout, generates a significant V_{DS} overshoot. If this overshoot exceeds the MOSFET rated breakdown voltage, it can lead to device degradation or catastrophic failure.

Therefore, $R_{G(OFF)}$ must be carefully optimized under worst-case operating conditions to control the turn-off slew rate and limit voltage stress. In practice, the selected resistor value should ensure that the peak drain-source voltage remains within a safe margin, typically:

- $V_{DS(peak)} < 80\% – 90\% \times V_{DS(max)}$

This optimization achieves a balance between minimizing switching losses and maintaining safe, reliable operation by preventing excessive voltage overshoot.

5.3.1. Benchmark Result

Based on these constraints that discussed above, the target criteria for tuning turn-off gate resistors ($R_{G(OFF)}$) are defined as follows:

- $V_{DS(peak)} < 960$ V to 1080 V

Through iterative tuning, it was determined that using a gate resistance of 2 Ω for both turn-off satisfies these criteria. This configuration effectively balances switching speed and transient control, limiting both voltage overshoot while maintaining safe operation within the device's electrical and thermal limits.

The TVMD turn-off benchmark test result are shown in Figure 6:

- The low-side (HS) V_{DS} overshoot is approximately 934 V.
  Figure 6 on page 11 shows a turn-off switching waveform with $R_{G(OFF)} = 2$ Ω.

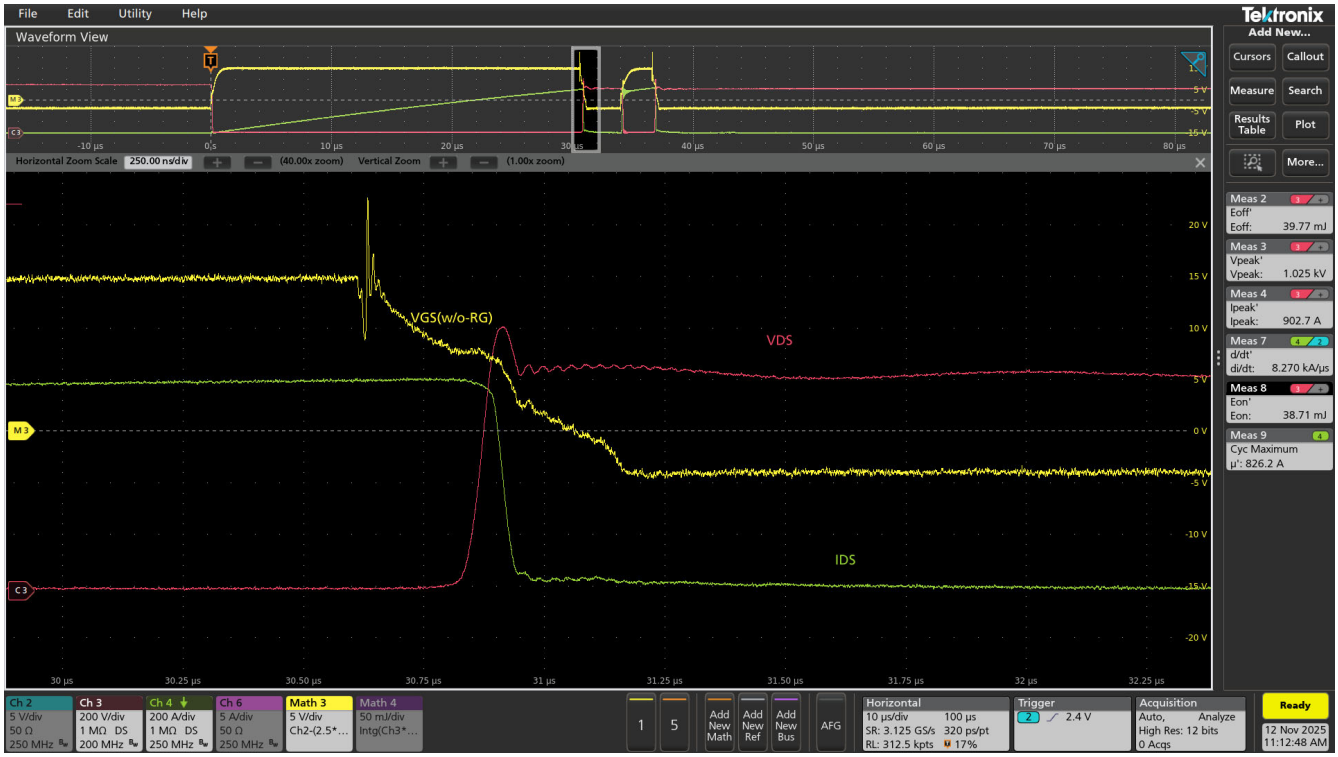


Figure 6. TVMD Turn-Off LS V_{DS} Overshoot

Note: *The VGS waveforms in all DPT results are mathematically derived by using:*

$V_{GS(w/o\ RG)} = V_{GS,measured} - I_{G,measured} \times R_{G,internal}$ *(2.5 Ω in this case).*

This equation is used to reflect true V_{GS} voltage at the actual MOSFET gate. The internal parasitic inductance impact is not considered here.

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6. ProVCD™ Tuning Method

During the Si829x double-pulse test (DPT), the ProVCD™ parameters were tuned at each test condition to optimize either switching loss or overshoot, depending on the evaluation objective. This adaptive tuning enables the gate drive profile to be tailored for specific operating points, demonstrating the flexibility of dynamic gate control.

For detailed information on the ProVCD™ optimization methodology, refer to “AN1453: Si829x ProVCD™ Optimization for Switching Loss Reduction”.

7. ProVCD™ vs. TVMD DPT Test Result under Varied Load

In this section, the double-pulse test (DPT) results are presented to demonstrate how the Si829x ProVCD™ enables reduction of switching loss or voltage overshoot without requiring the typical trade-off between the two. The evaluation is performed under varying load current (I_{DS}) conditions, while maintaining a constant ambient temperature of 25 °C. This approach highlights the effectiveness of dynamic gate waveform shaping in optimizing switching performance across different operating points.

The results presented in this section are based on the Wolfspeed XM3 SiC module, which incorporates a relatively high internal gate resistance of 2.5 Ω. This internal gate resistance limits the maximum gate current delivered to the device and reduces the effectiveness of dynamic gate shaping, thereby limiting the achievable reduction in switching loss and overshoot. Modules with lower internal gate resistance allow the programmable current stages of ProVCD™ to exert greater control over the switching transition, potentially enabling further performance improvements. For test results and comparisons on additional SiC modules with lower internal gate resistance, refer to the ProVCD™ vs. TVMD DPT Test Results on Varied Modules section.

7.1. Reduce Switching Loss by Using ProVCD™

To demonstrate that the Si829x ProVCD™ reduces switching loss without compromising overshoot, the comparison results are presented in two sections: analysis at a single test current point and evaluation across varied test current conditions.

7.1.1. Turn-On Switching Loss Test Result

7.1.1.1. Single Current DPT Result

Table 2 summarizes key results on the XM3 module. Detailed waveform comparisons and discussion are provided in subsequent sections.

Table 2. Turn-On ProVCD™ vs. TVMD EON results at 900 V and 500 A

Mode	E_{ON} (mJ)	I_{DS_PEAK} (A)	Turn-On dI/dt (A/ns)	Turn-On dV/dt (V/ns)
TVMD (R_G = 2 Ω)	26.2	587.1	6.0	9.8
2-stage ProVCD™[1]	23.3 (down 11%)	583.5	8.3	12.1
3-stage ProVCD™[1]	21.0 (down 20%)	587.1	8.3	15.3

1. Refer to “AN1453: Si829x ProVCD™ Optimization for Switching Loss Reduction” for further explanations of 2-stage and 3-stage turn-on ProVCD™ profiles.

1. The TVMD DPT results are obtained and used as the benchmark, as shown in the waveform capture below. The corresponding dI/dt and dV/dt are annotated for reference. Under these conditions, the measured baseline performance is E_{ON} = 26.2 mJ and I_{PEAK} = 587.1 A, establishing the reference point for comparison with ProVCD™ operation.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}



Figure 7. TVMD Turn-On DPT Waveforms under 900 V, 500 A (RG = 2 Ω)

2. By optimizing ProVCD™ with a two-stage turn-on profile (I_{ON1} = 15 A, T_{ON1} = 68.75 ns; I_{ON2} = 2.48 A), the resulting waveforms are shown below. This configuration achieves a reduced E_{ON} of 23.3 mJ, corresponding to an 11% reduction compared to the TVMD benchmark, without any increase in peak current (I_{PEAK}).The optimized profile also results in increased dI/dt and dV/dt, as observed in the waveform, indicating a faster switching transition while maintaining controlled current behavior.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}



Figure 8. Two-Stage ProVCD™ Turn-On DPT Waveforms under 900 V, 500 A (R_G = 0.2 Ω)

3. By optimizing ProVCD™ with a three-stage turn-on profile (I_{ON1} = 15 A, T_{ON1} = 68.75 ns; I_{ON2} = 2.48 A, T_{ON2} = 37.5 ns; I_{ON3} = 15 A), the resulting waveforms are shown below. This configuration achieves a reduced E_{ON} of 21.0 mJ, corresponding to a 20% reduction compared to TVMD without any increase in peak current (I_{PEAK}).

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}



Figure 9. Three-Stage ProVCD™ Turn-On DPT Waveforms Under 900 V, 500 A (R_G = 0.2 Ω)

7.1.1.2. Varied Test Current DPT Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, I_{DS} ranging from 50 A to 850 A, and room temperature (25 °C).

In the high-current range (200 A to 850 A), two-stage ProVCD™ demonstrates a relatively consistent E_{ON} reduction of approximately 10% on XM3 module compared to the TVMD benchmark. In contrast, within the low-current range (< 100 A), the E_{ON} reduction decreases to approximately 4%, reflecting the reduced impact of dynamic gate waveform shaping under lighter load conditions.

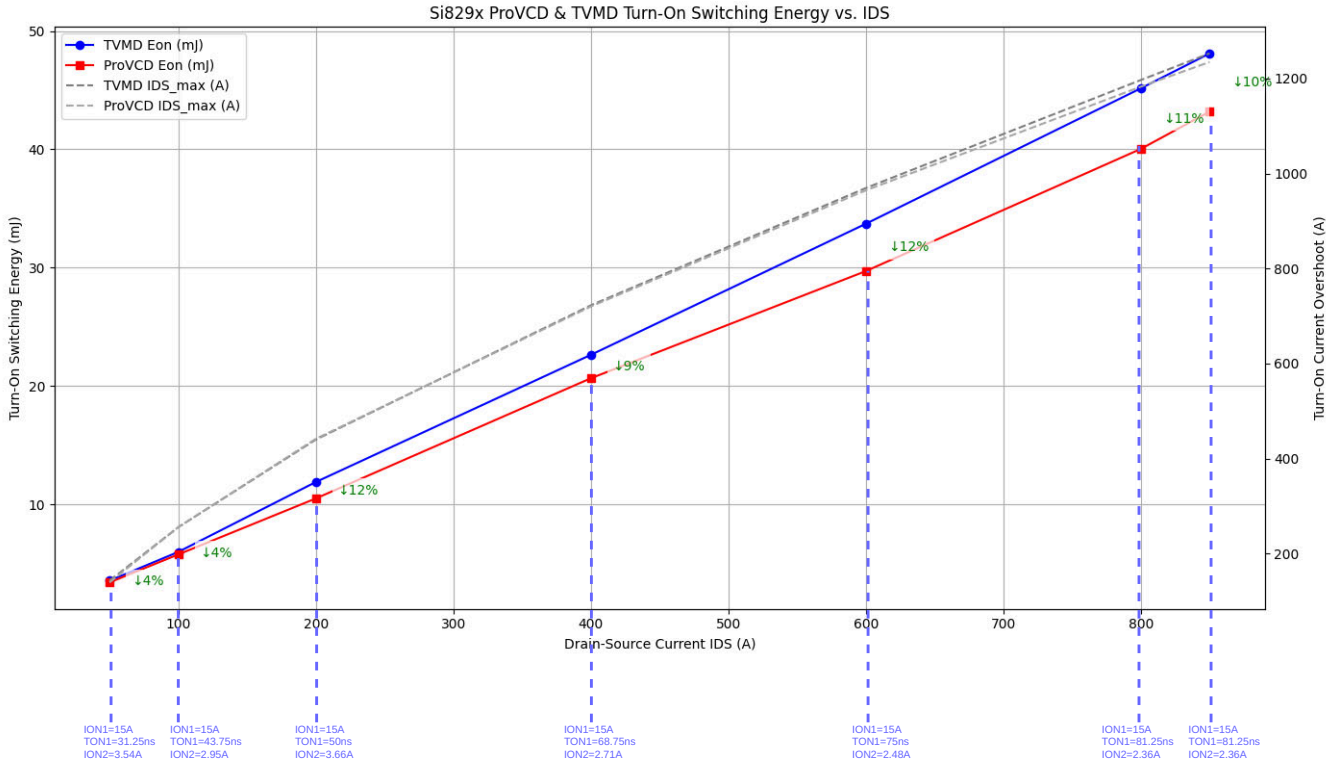


Figure 10. Si829x ProVCD™ vs. TVMD E_{ON} Comparison under Varied I_{DS} (Fixed 900 V and 25 °C)

7.1.2. Turn-Off Switching Loss Test Result

7.1.2.1. Single-Current DPT Result

A summary table of the key results on XM3 module is shown below. Detailed waveform comparisons and discussion are provided in the subsequent sections.

Table 3. Turn-Off ProVCD™ vs. TVMD E_{OFF} results at 900 V and 500 A

	E_{OFF} (mJ)	V_{DS_PEAK} (V)	Turn-Off dI/dt (A/ns)	Turn-Off dV/dt (V/ns)
TVMD (RG=2O)	22.3	1041.0	11.6	14.7
ProVCD™ Turn-Off	20.1 (down 10%)	1041.0	13.2	18.7

1. The TVMD DPT results are obtained and used as the benchmark, as shown in the waveform capture below. The corresponding dI/dt and dV/dt are annotated for reference. Under these conditions, the measured baseline performance is E_{OFF} = 22.3 mJ and V_{PEAK} = 1041.0 V, establishing the reference for comparison with ProVCD™-based turn-off performance.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}

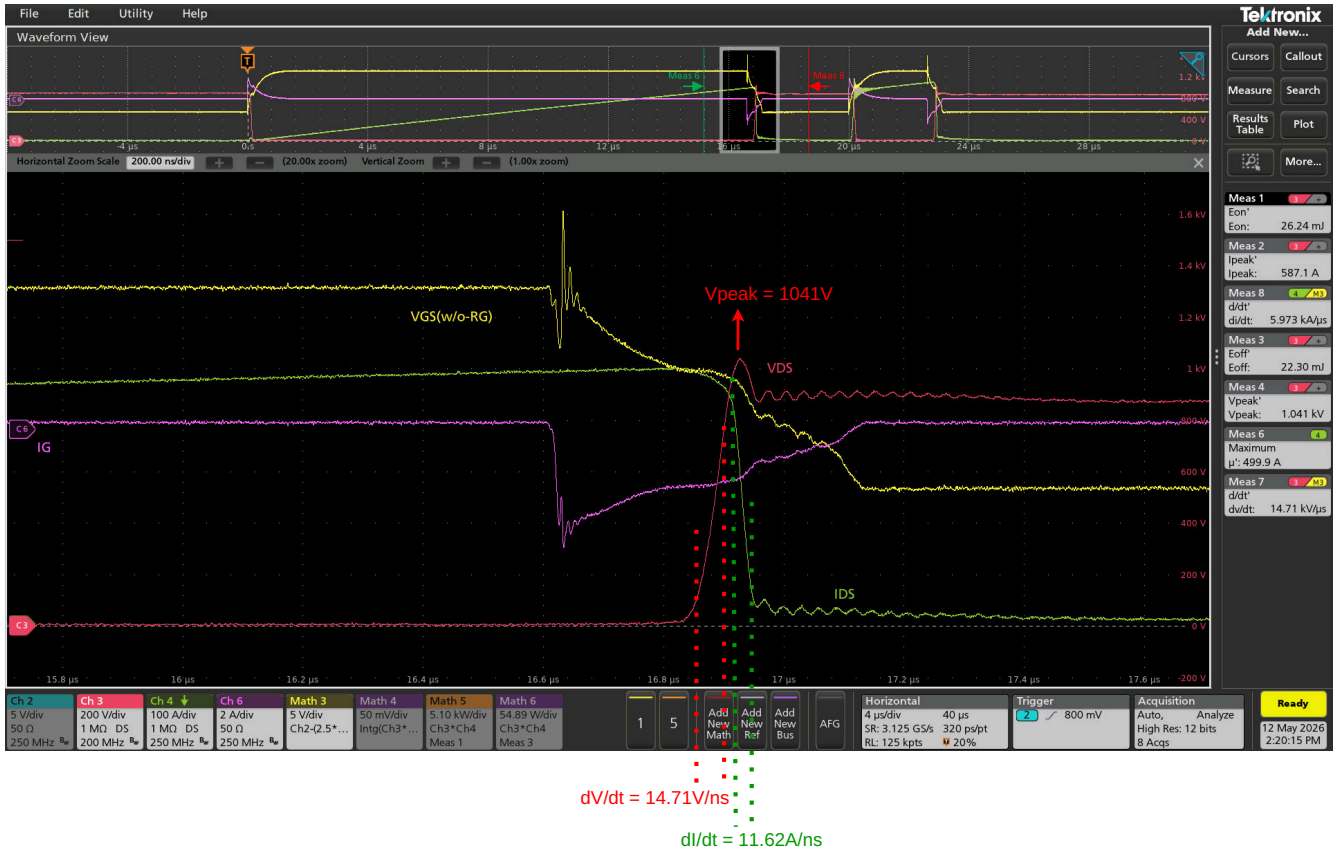


Figure 11. TVMD Turn-Off DPT Waveforms Under 900 V, 500 A (R_G = 2 Ω)

2. By optimizing ProVCD™ with a turn-off profile (I_{OFF1} = 15 A, T_{OFF1} = 137.5 ns; I_{OFF2} = 2.12 A; I_{MC} = 15 A), the resulting waveforms are shown below. This configuration achieves a reduced EOFF of 20.1 mJ, corresponding to a 10% reduction compared to the TVMD benchmark, without any increase in peak voltage (V_{PEAK}). The optimized turn-off profile also results in increased dI/dt and dV/dt, as observed in the waveform, indicating a faster transition while maintaining controlled voltage stress within the defined limits.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}

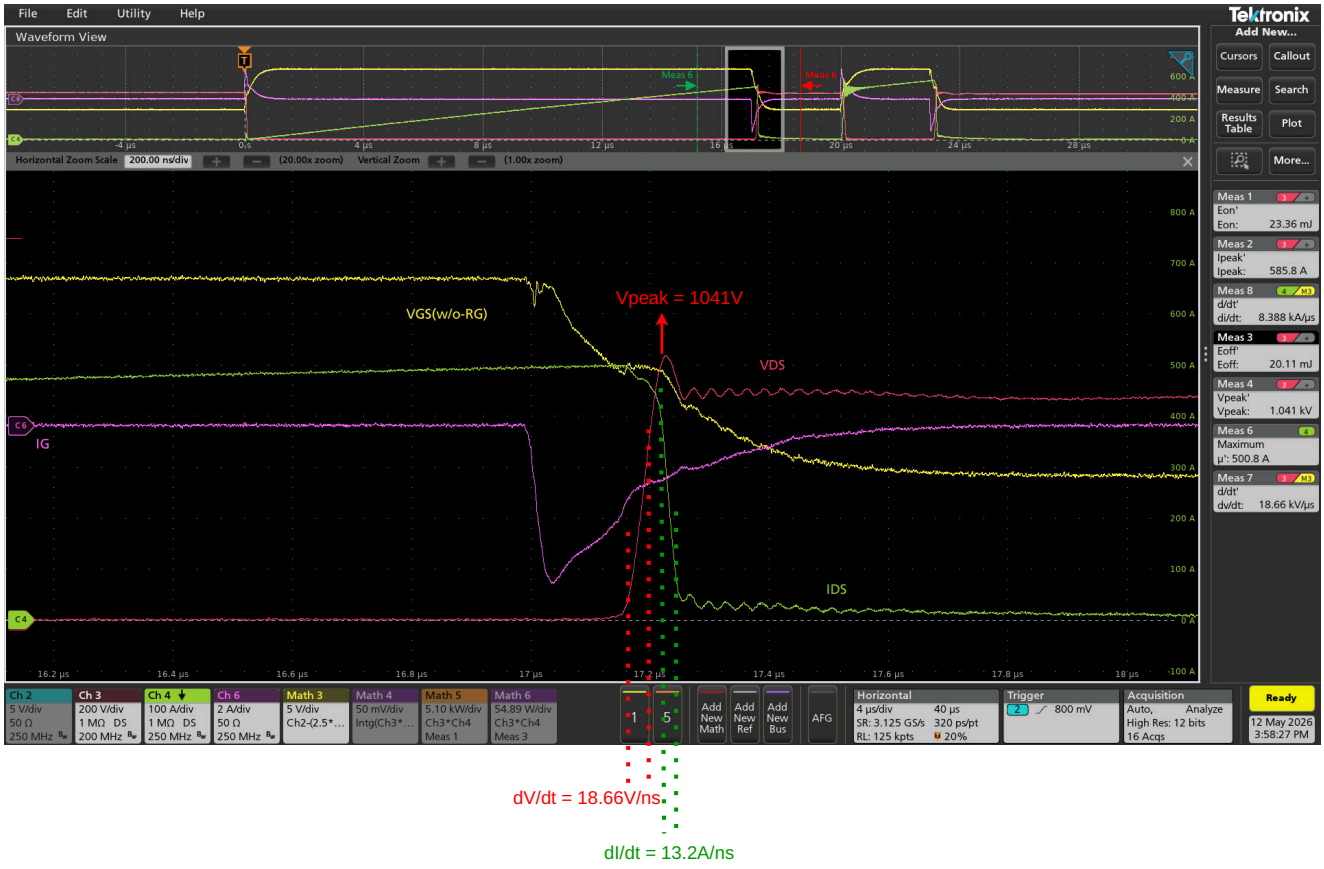


Figure 12. Two-Stage ProVCD™ Turn-Off DPT Waveforms Under 900 V, 500 A (R_G = 0.2 Ω)

7.1.2.2. Varied Test Current DPT Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, I_{DS} ranging from 50 A to 850 A, and room temperature (25 °C).

In the high-current range (200 A to 850 A), ProVCD™ demonstrates a relatively consistent E_{OFF} reduction of approximately 15% to 20% compared to the TVMD benchmark. In the low-current range (< 100 A), the E_{OFF} reduction decreases, reflecting the reduced influence of dynamic gate waveform shaping under lighter load conditions.

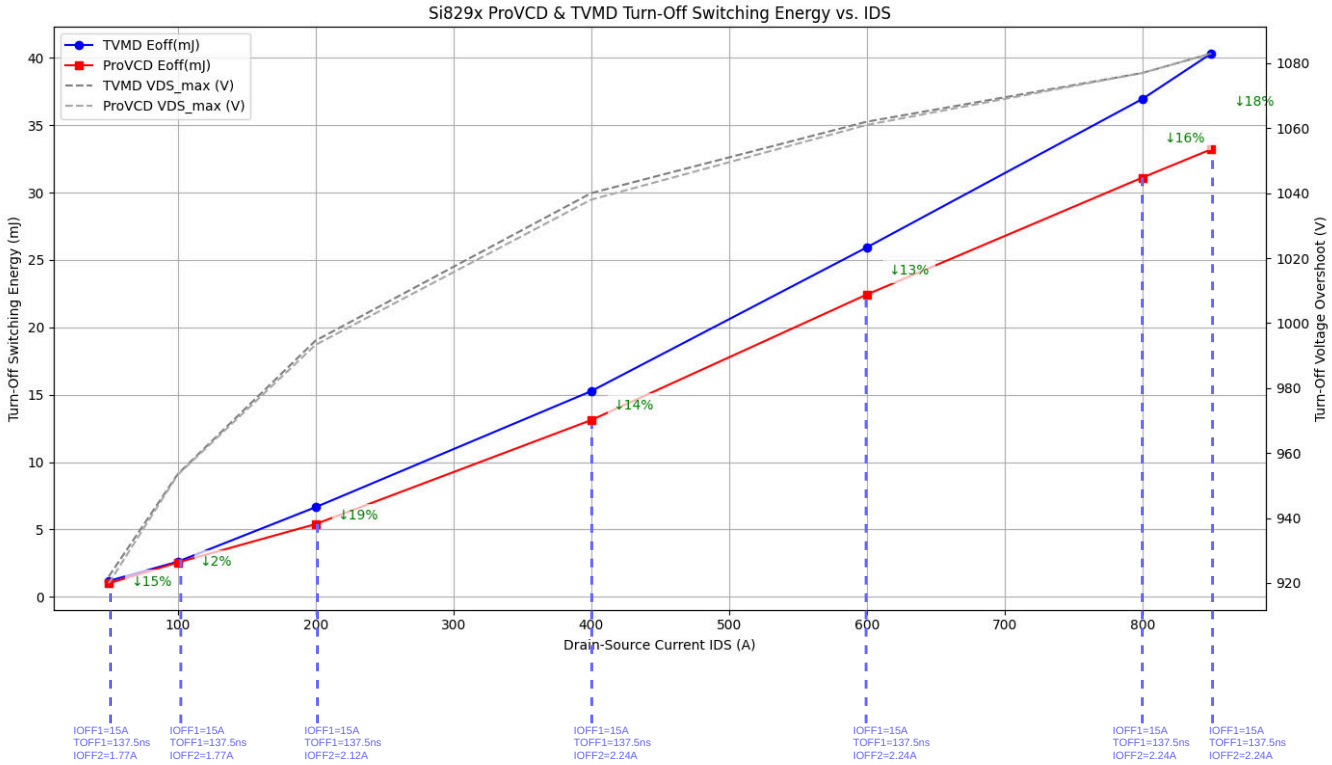


Figure 13. Si829x ProVCD™ vs. TVMD E_{OFF} Comparison under Varied I_{DS}, Fixed 900 V and 25 °C

7.2. Reduce Overshoot by Using ProVCD™

To demonstrate that the Si829x ProVCD™ reduces overshoot without compromising switching loss, the comparison results are presented in two sections: analysis at a single test current point and evaluation across varied test current conditions.

7.2.1. Turn-On Overshoot Loss Test Result

7.2.1.1. Single Current DPT Result

A summary table of the key results on XM3 module is shown below. Detailed waveform comparisons and discussion are provided in the subsequent sections.

Table 4. ProVCD™ Turn-On ProVCD vs. TVMD I_{PEAK} Results at 900 V and 850 A

	E_{ON} (mJ)	I_{DS_PEAK} (A)	Turn-On dI/dt (A/ns)
TVMD (R_G = 2 Ω)	42.8	927.6	8.1
Two-stage ProVCD™ Turn-On	41.7	907.1 (down 26%)	10.4

1. The TVMD DPT results are obtained and used as the benchmark, as shown in the waveform capture below. The corresponding dI/dt and dV/dt are annotated for reference. Under these conditions, the measured baseline performance is E_{ON} = 42.8 mJ and I_{PEAK} = 927.6 A, establishing the reference for comparison with ProVCD™-based turn-on performance.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}

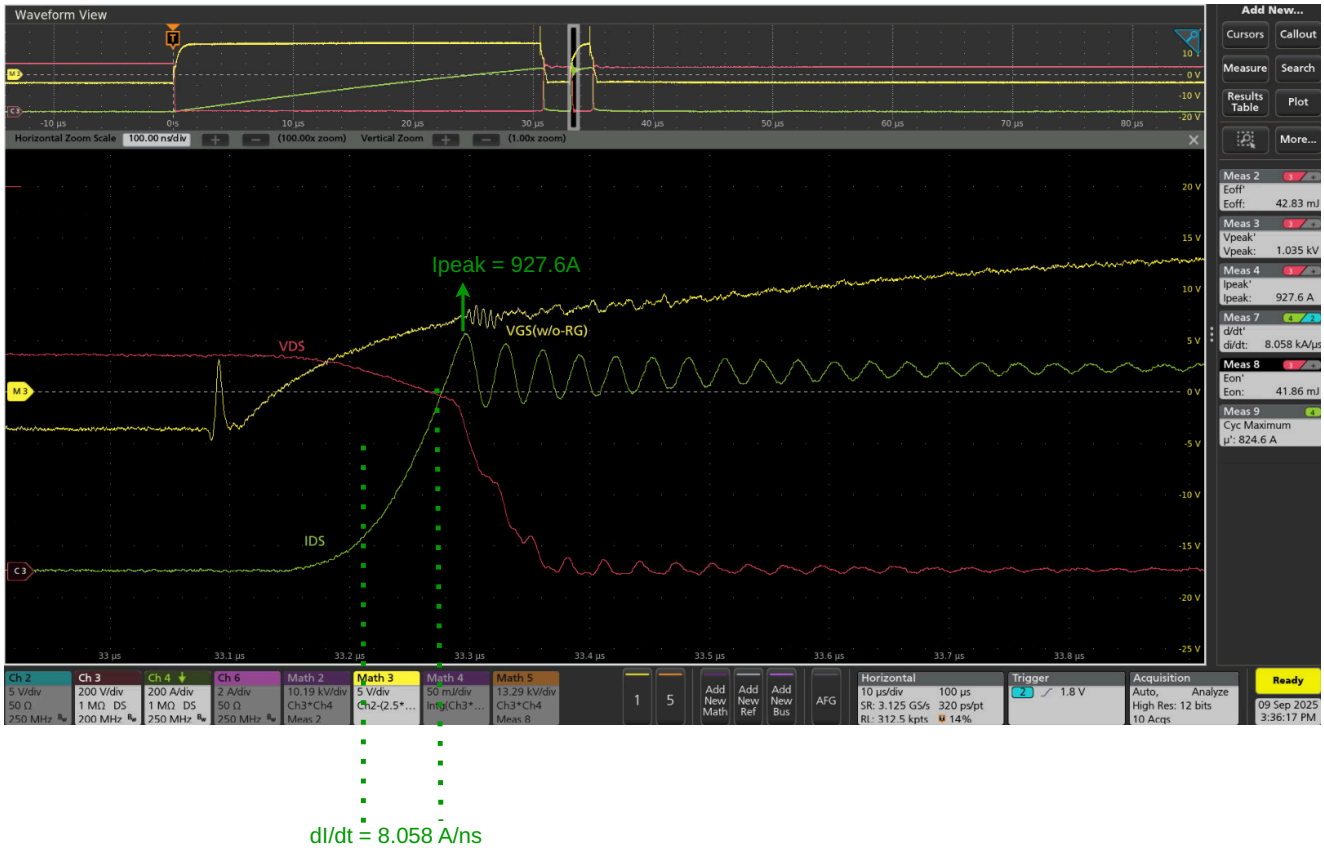


Figure 14. TVMD Turn-On DPT Waveforms Under 900 V, 850 A (R_G = 2 Ω)

2. By optimizing ProVCD™ with a two-stage turn-on profile (I_{ON1} = *15 A,* T_{ON1} = *75 ns;* I_{ON2} = *2.12 A*), the resulting waveforms are shown below. This configuration results in a measured peak current (I_{PEAK}) of 907.1 A. Based on a dc load current of 850 A, this corresponds to a 26% reduction in current overshoot compared to the TVMD benchmark. The optimized profile leads to an increased dI/dt, as observed in the waveform, indicating a faster current transition while maintaining controlled overshoot.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}

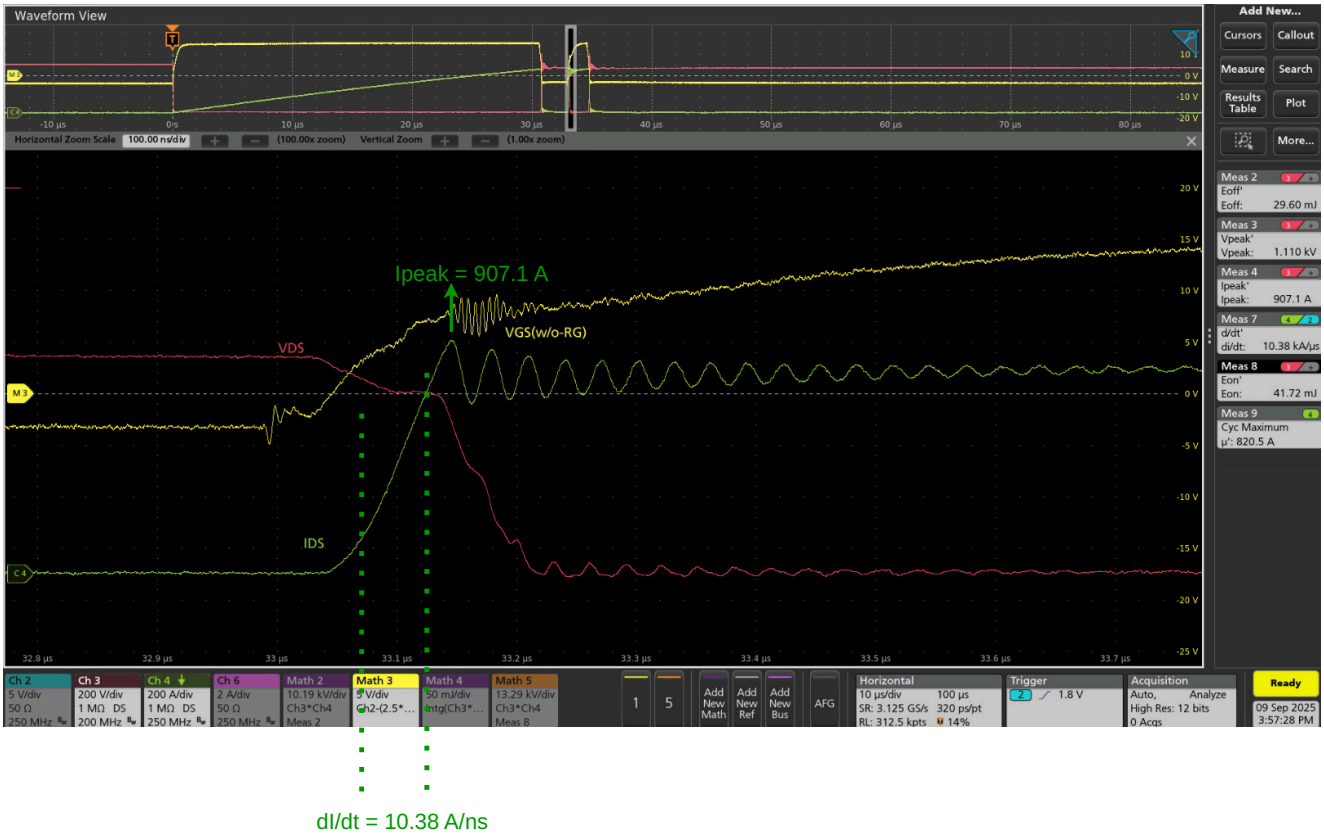
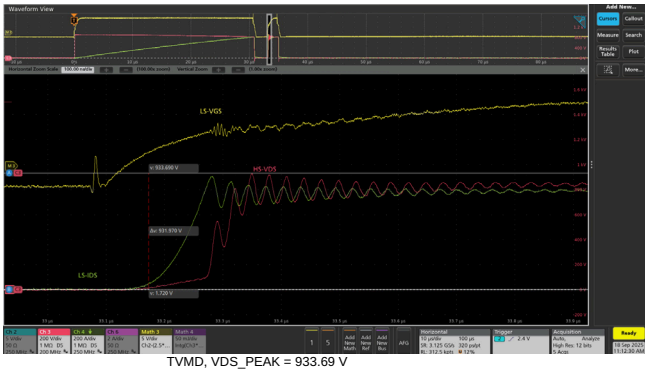


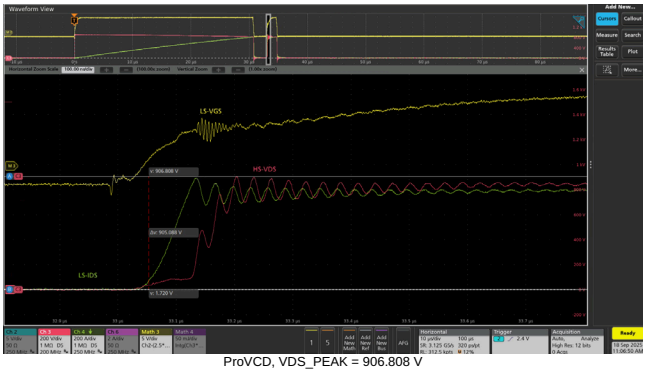
Figure 15. Two-Stage ProVCD™ Turn-On DPT Waveforms Under 900 V, 850 A (R_G = 0.2 Ω)

3. Additionally, the high-side (HS) body diode reverse recovery voltage overshoot is compared between ProVCD™ and TVMD operation. Using the same optimized ProVCD™ turn-on profile, the measured voltage overshoot is reduced from 933.7 V (TVMD) to 906.8 V, demonstrating the effectiveness of dynamic gate shaping in mitigating reverse recovery-induced transients.

CH3 (Red) – HS V_{DS}, CH4 (Green) – I_{DS}, CH6 (Pink) – I_G, Math3 (Yellow) – V_{GS}



TVMD, VDS_PEAK = 933.69 V



ProVCD, VDS_PEAK = 906.808 V

Figure 16. Two-Stage ProVCD™ Turn-On DPT Waveforms Under 900 V, 850 A (R_G = 0.2 Ω)

7.2.1.2. Varied Test Current DPT Result

To evaluate ProVCD™ performance under varying load conditions, the comparisons presented in the previous section were conducted across multiple IDS levels ranging from 200 A to 850 A. At each test point, the ProVCD™ current profile was individually optimized to match the current and voltage overshoot observed in the corresponding TVMD results. This approach ensures a fair comparison by maintaining equivalent transient stress levels while highlighting the achievable improvements in switching performance with dynamic gate shaping.

The graph below is derived from DPT results measured at V_{DS} = 900 V, with I_{DS} ranging from 200 A to 850 A, at room temperature (25 °C).

In the high-current range (200 A to 850 A), ProVCD™ demonstrates a consistent reduction in peak current (I_{PEAK}), ranging from approximately 4% to 24% compared to the TVMD benchmark. Furthermore, the reduction in I_{PEAK} increases with load current, indicating that ProVCD™ provides greater benefit in limiting current overshoot under higher-power operating conditions.

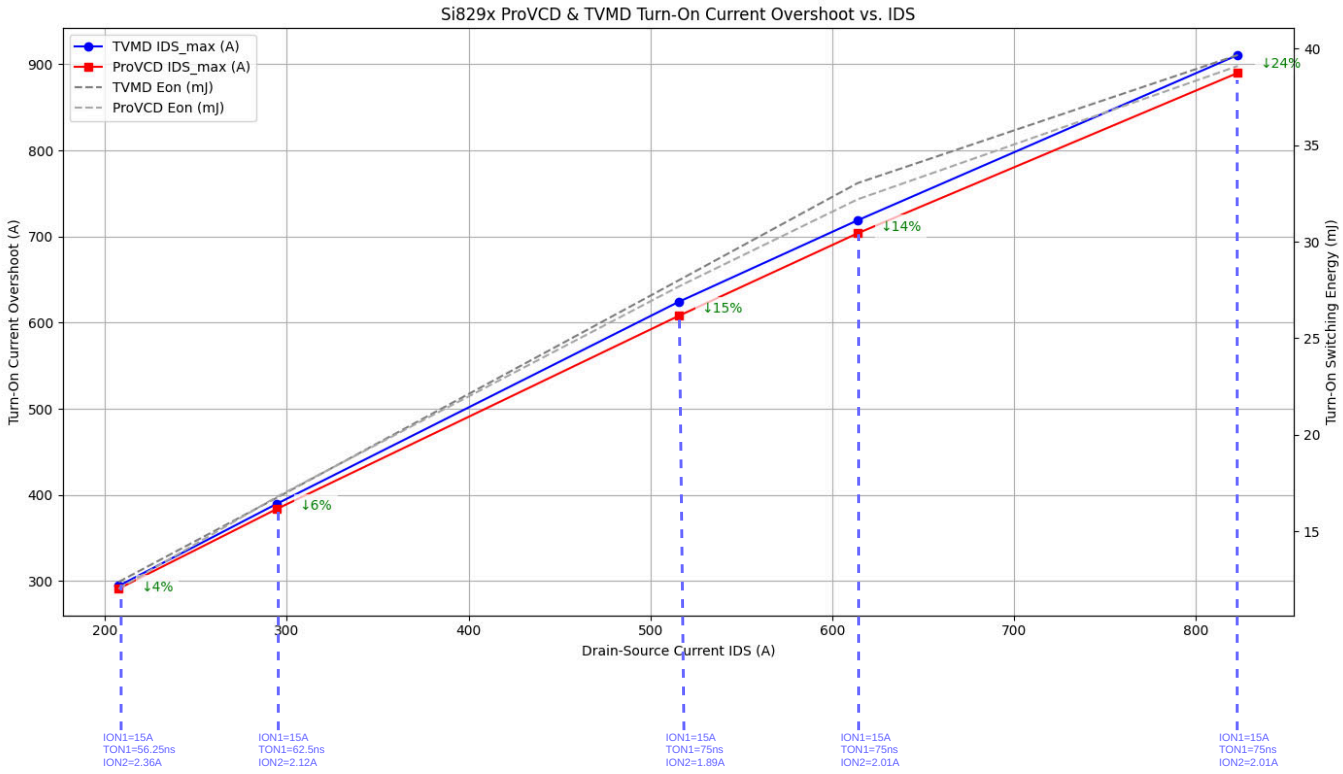


Figure 17. Si829x ProVCD™ vs. TVMD I_{DS_PEAK} Comparison Under Varied I_{DS}, Fixed 900 V and 25 °C

7.2.2. Turn-Off Overshoot Loss Test Result

7.2.2.1. Single Current DPT Result

A summary table of the key results on XM3 module is shown below. Detailed waveform comparisons and discussion are provided in the subsequent sections.

Table 5. ProVCD™ Turn-Off ProVCD™ vs. TVMD Overshoot Results

	E_{OFF} (mJ)	V_{DS_PEAK} (V)
TVMD (R_G = 2 Ω)	43.7	1037.0
ProVCD™ Turn-Off	43.6	981.9 (down 40%)

1. The TVMD DPT results are obtained and used as the benchmark, as shown in the waveform capture below. Under these conditions, the measured baseline performance is E_{OFF} = 43.7 mJ and V_{PEAK} = 1037.0 V, establishing the reference for comparison with ProVCD™-based turn-off performance.

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, Math3 (Yellow) – V_{GS}

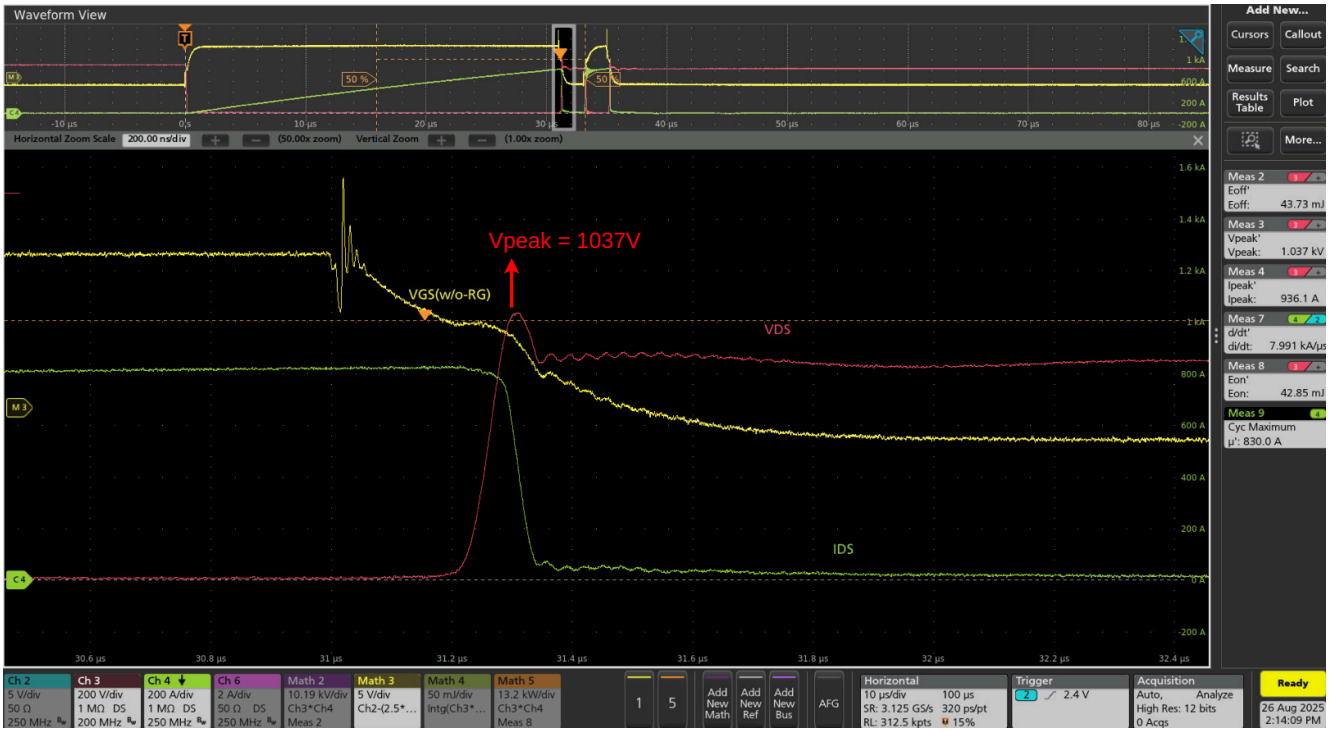


Figure 18. TVMD Turn-Off DPT Waveforms Under 900 V, 850 A (R_G = 2 Ω)

2. By optimizing ProVCD™ with an optimized turn-off profile (I_{OFF1} = 15 A, T_{OFF1} = 156.25 ns; I_{OFF2} = 0.83 A), the resulting waveforms are shown below. This configuration achieves a reduced peak voltage (V_{PEAK}) of 981.9 V, corresponding to a 40% reduction in voltage overshoot relative to the 900 V dc bus, without an increase in switching energy (E_{OFF}).

CH3 (Red) – V_{DS}, CH4 (Green) – I_{DS}, Math3 (Yellow) – V_{GS}

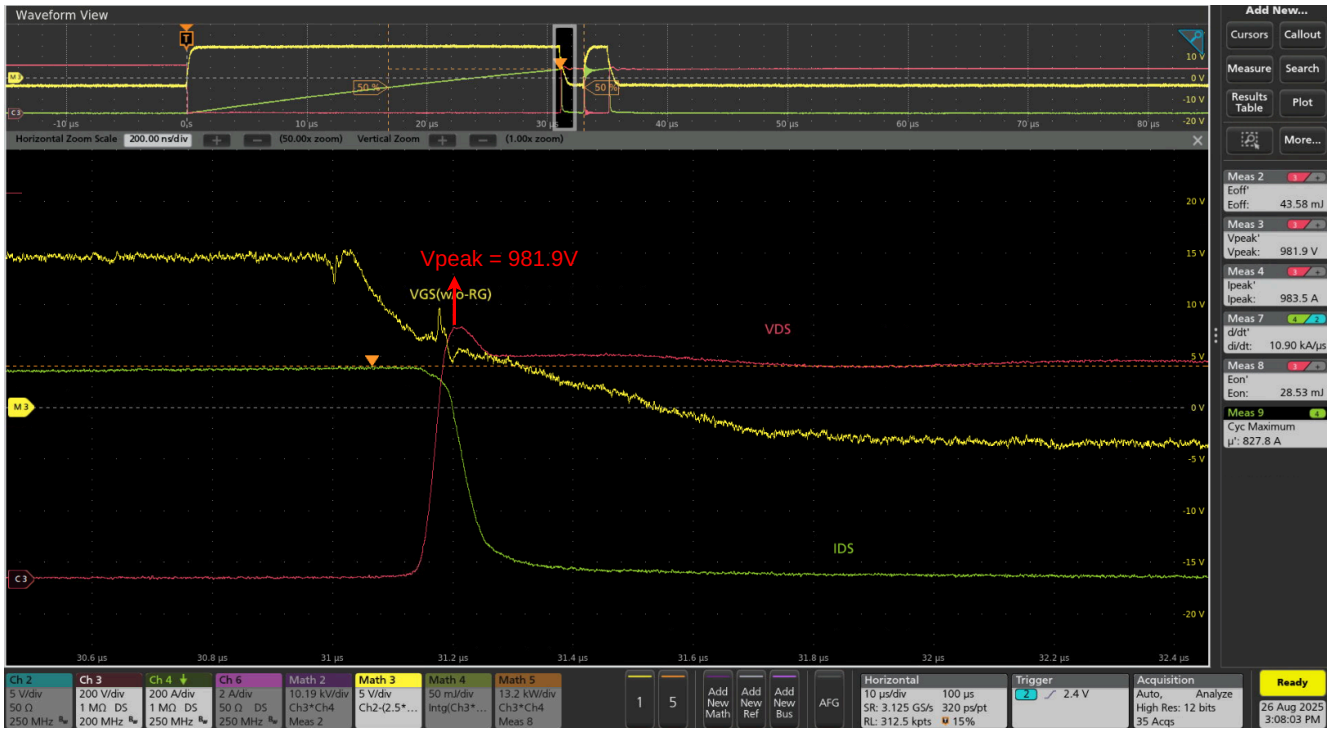


Figure 19. ProVCD™ Turn-Off DPT Waveforms Under 900 V, 850 A (R_G = 0.2 Ω)

7.2.2.2. Varied Test Current DPT Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, with I_{DS} ranging from 200 A to 850 A, at room temperature (25 °C).

In the high-current range (200 A to 850 A), ProVCD™ demonstrates a relatively consistent reduction in voltage overshoot ($V_{PEAK} – V_{DC}$), typically in the range of 30% to 40% compared to the TVMD benchmark. Furthermore, the overshoot reduction becomes more pronounced at higher load currents, indicating increased effectiveness of dynamic gate shaping under high-current operating conditions.

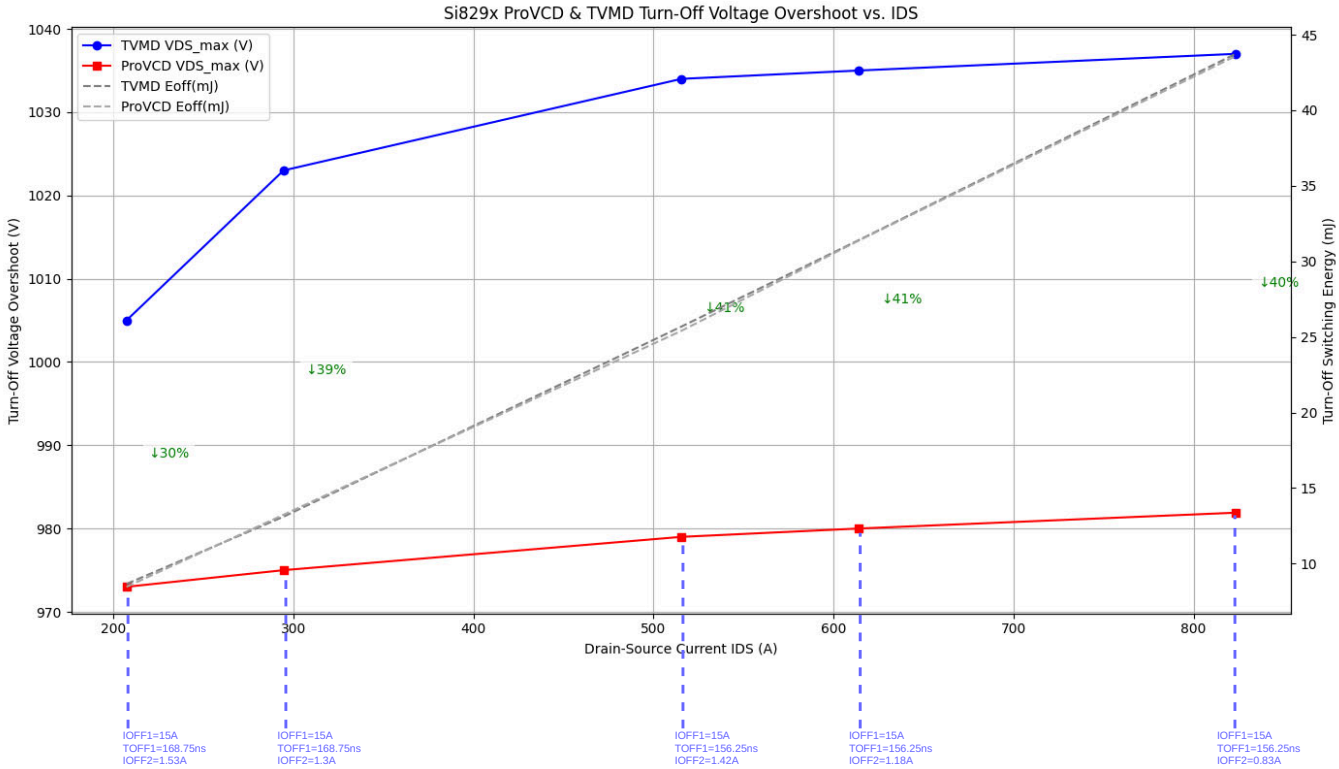


Figure 20. Si829x ProVCD™ vs. TVMD E_{OFF} Comparison Under Varied I_{DS}, fixed 900 V and 25 °C

8. ProVCD™ vs. TVMD DPT Test Result under Varied Temperatures

To evaluate ProVCD™ performance under varying operating conditions, the comparisons presented in the previous section were conducted across multiple SiC module junction temperatures ranging from 25 °C to 125 °C. At each temperature point, the ProVCD™ current profile was individually optimized to match either the switching energy or the overshoot characteristics of the corresponding TVMD results.

This methodology ensures a fair comparison by maintaining consistent switching loss or transient stress levels, while clearly demonstrating the effectiveness of dynamic gate waveform shaping across a wide temperature range.

The benefits of ProVCD™ in reducing turn-on switching energy (E_{ON}), turn-off switching energy (E_{OFF}), turn-on current overshoot, and turn-off voltage overshoot are demonstrated in the respective sections below.

8.1. Turn-On Switching Loss Temperature Test Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, I_{DS} = 850 A, and junction temperatures ranging from 25 °C to 125 °C.

Across this temperature range, ProVCD™ achieves a relatively consistent reduction in turn-on switching energy (E_{ON}) of approximately 10% compared to the TVMD benchmark, demonstrating stable performance and effectiveness of dynamic gate waveform shaping under varying thermal conditions.

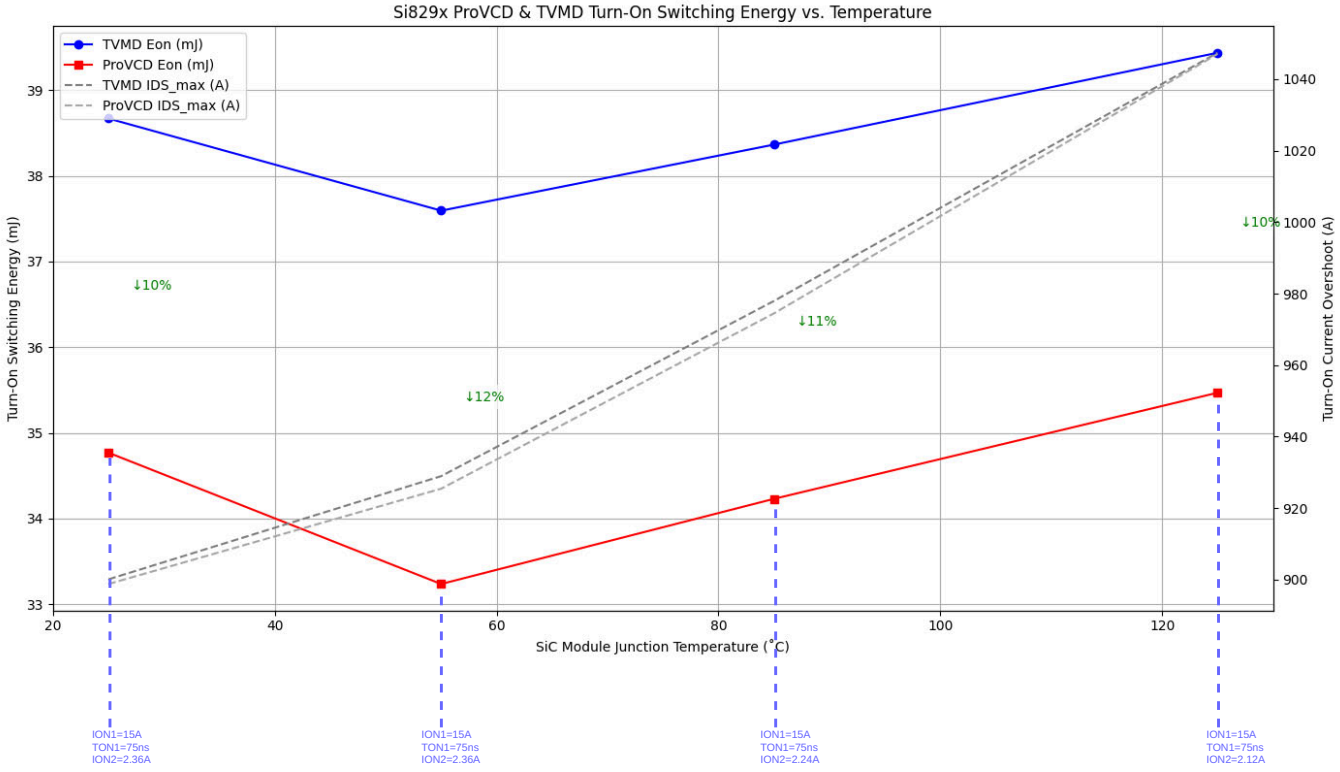


Figure 21. Si829x ProVCD™ vs. TVMD E_{ON} Comparison Under Varied Temperature, Fixed 900 V and 850 A

8.2. Turn-Off Switching Loss Temperature Test Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, I_{DS} = 850 A, and junction temperatures ranging from 25 °C to 125 °C.

ProVCD™ continues to achieve E_{OFF} improvement as junction temperature increases compared to TVMD.

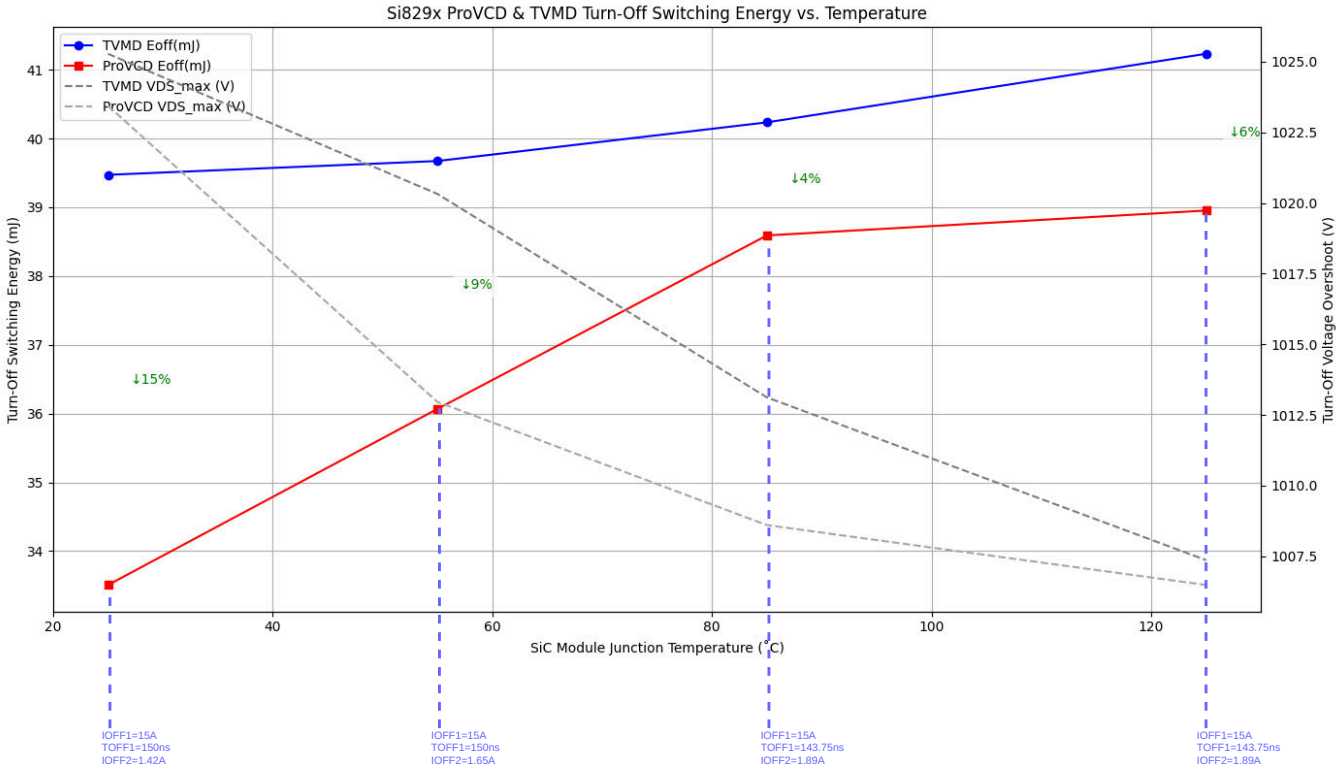


Figure 22. Si829x ProVCD™ vs. TVMD E_{OFF} Comparison Under Varied Temperature, Fixed 900 V and 850 A

8.3. Turn-On Current Overshoot Temperature Test Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, I_{DS} = 850 A, and junction temperatures ranging from 25 °C to 125 °C.

ProVCD™ achieves a relatively consistent reduction in peak current (I_{PEAK}) of approximately 7% to 31% across the evaluated temperature range compared with TVMD.

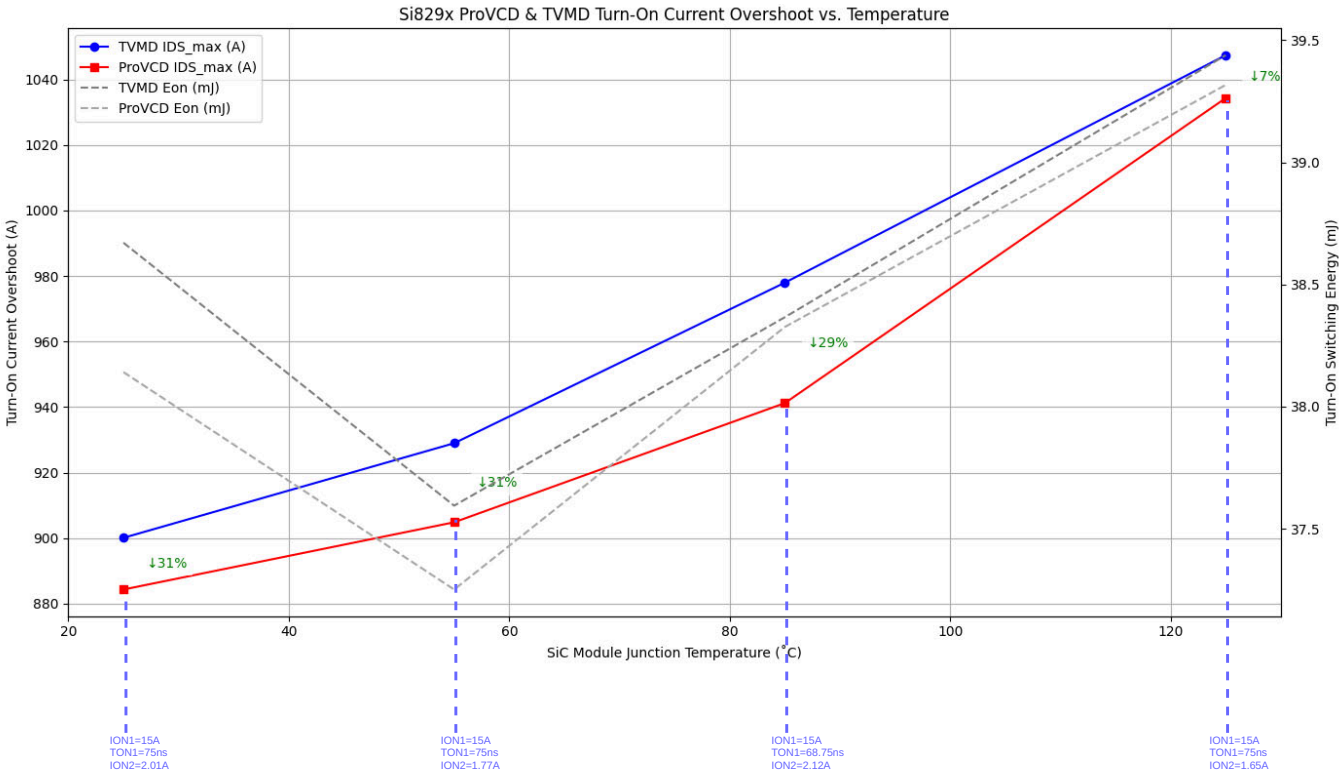


Figure 23. Si829x ProVCD™ vs. TVMD I_{PEAK} Comparison Under Varied Temperature, Fixed 900 V and 850 A

8.4. Turn-Off Voltage Overshoot Temperature Test Result

The graph below is derived from DPT results measured at V_{DS} = 900 V, I_{DS} = 850 A, and junction temperatures ranging from 25 °C to 125 °C.

ProVCD™ demonstrates a reduction in voltage overshoot ($V_{PEAK} – V_{DC}$) across the temperature range, compared with TVMD.

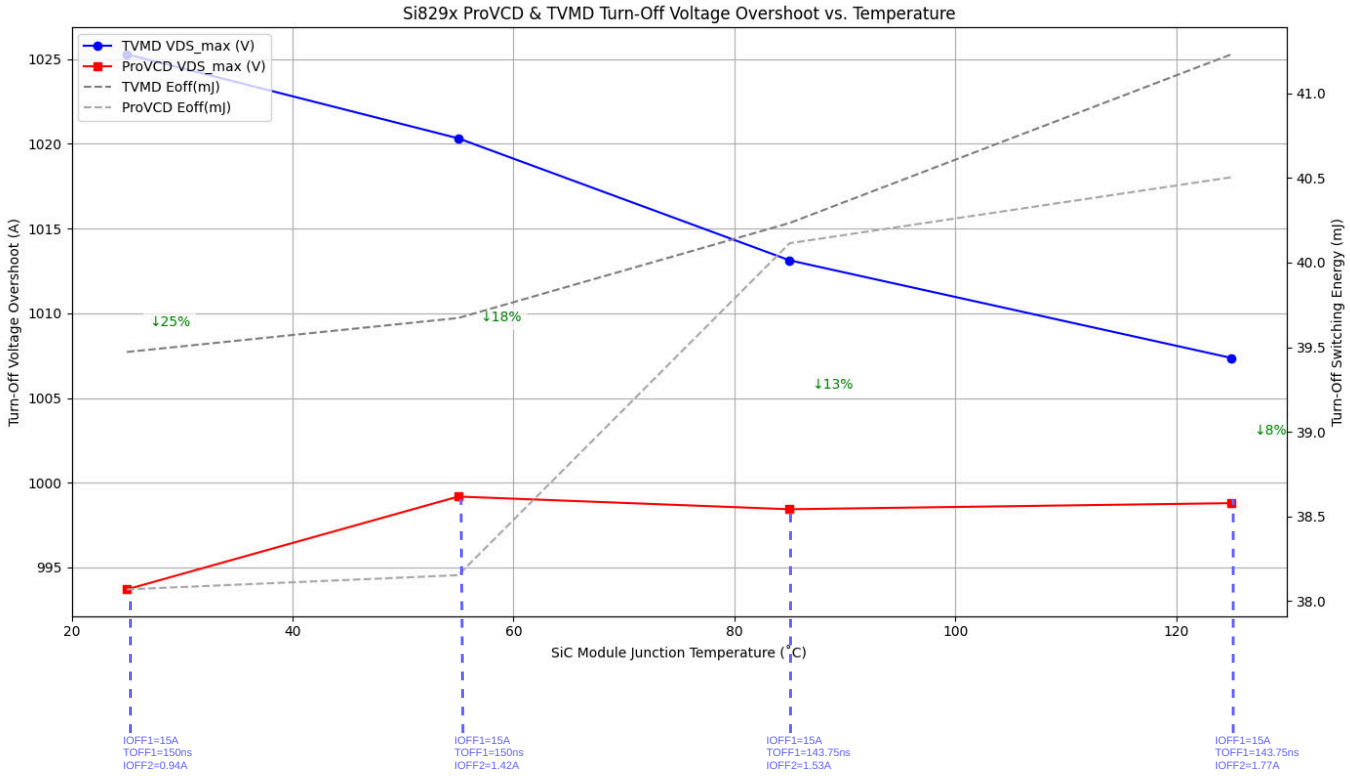


Figure 24. Si829x ProVCD™ vs. TVMD V_{PEAK} Comparison Under Varied Temperature, Fixed 900 V and 850 A

9. ProVCD™ vs. TVMD DPT Test Result on Varied Modules

The results presented in the previous sections are based on the Wolfspeed XM3 module, which features an internal gate resistance of approximately 2.5 Ω. This internal gate resistance plays a critical role in determining the achievable benefits of ProVCD™, as it directly influences the gate current profile, switching transition speed, and the effectiveness of dynamic gate waveform shaping.

In addition to internal gate resistance, other SiC module characteristics can also vary from module to module and impact switching behavior. Parameters, such as gate charge, Miller charge, input and reverse-transfer capacitance, threshold voltage, transconductance, on-state resistance, and internal parasitic inductance, may differ across module designs or device generations. These variations can influence turn-on and turn-off delay, dV/dt, dI/dt, voltage overshoot, ringing, switching loss, and dynamic current sharing. As a result, the effectiveness of ProVCD™ is influenced not only by the nominal internal gate resistance, but also by the broader set of electrical and parasitic characteristics of the SiC module. Note however, series gate resistance of the modules does have a first-order impact on switching loss, which is demonstrated in the data.

To further evaluate these effects, additional tests were conducted on multiple SiC modules with different internal gate resistance values and module characteristics using both ProVCD™ and traditional voltage-mode driving (TVMD). This section presents the comparative results, highlighting how the Si829x ProVCD™ reduction potential varies across different module implementations. The results demonstrate the adaptability of ProVCD™ and its ability to extend performance benefits across a range of SiC module characteristics.

9.1. YM3 SiC Module ProVCD™ Test Result

To demonstrate the performance of Si829x ProVCD™ on modules beyond the Wolfspeed XM3 platform, the Wolfspeed YM3 six-pack SiC module (ECB2R1M12YM3) was evaluated. To avoid duplicating the analysis presented in the previous sections, this section focuses solely on the ability of Si829x ProVCD™ to reduce turn-on switching energy (E_{ON}) and turn-off switching energy (E_{OFF}).

Similar to the XM3 evaluation, double-pulse testing was performed using the Wolfspeed YM3 CIL platform. The traditional voltage-mode driving (TVMD) benchmark was established by following the methodology described in 5. “Traditional Voltage Mode (TVMD) Benchmark Setup and Test Result”, including optimization of the turn-on and turn-off gate resistors under worst-case operating conditions.

The ECB2R1M12YM3 module differs significantly from the XM3 module, featuring a much lower internal gate resistance of 0.5 Ω and a total gate charge (Q_G) of 1696 nC. The lower internal gate resistance enables higher gate current and allows the programmable current stages of ProVCD™ to exert greater influence over the switching transition. As a result, the ProVCD™ current profiles must be configured differently to achieve optimal performance.

For this evaluation, the ProVCD™ parameters were tuned to maximize switching loss reduction while maintaining the same transient stress levels as the TVMD benchmark. Specifically, the optimization target was to minimize turn-on switching energy (E_{ON}) and turn-off switching energy (E_{OFF}) without increasing turn-on current overshoot ($I_{DS,peak}$) or turn-off voltage overshoot ($V_{DS,peak}$). This methodology provides a fair comparison and highlights the additional performance benefits that ProVCD™ can deliver on modules with lower internal gate resistance.

9.1.1. Turn-On Switching Loss Test Result

By optimizing ProVCD™ with a three-stage turn-on profile *(I_{ON1} = 15 A, T_{ON1} = 43.75 ns; I_{ON2} = 2.01 A, T_{ON2} = 68.75 ns; I_{ON3} = 15 A)*, the resulting waveforms are shown below. This configuration achieves a reduced E_{ON} of 27.42 mJ, corresponding to an 51% reduction compared to the TVMD benchmark (55.7 mJ), without any increase in peak current (I_{PEAK}).The optimized profile also results in increased dI/dt and dV/dt, as observed in the waveform, indicating a faster switching transition while maintaining controlled current behavior.

CH5 (Orange) – I_{DS}, CH2 (Blue) – I_{GS}, CH3 (Red) – VDS, Math1 (Purple) – E_{ON}, Ref1 (Gray) – TVMD V_{DS}, Ref2 – TVMD I_{DS}

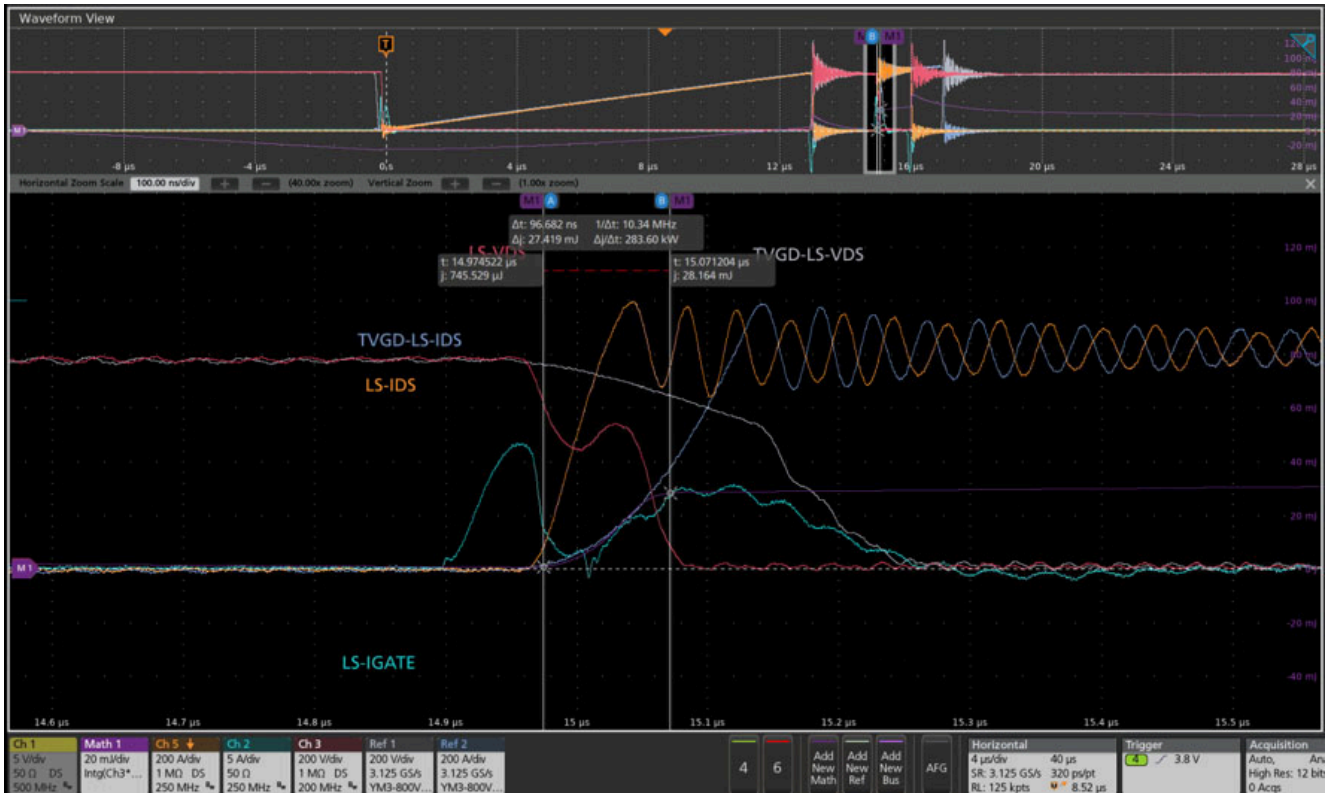


Figure 25. ProVCD™ Turn-On DPT Waveforms Under 800 V, 800 A

9.1.2. Turn-Off Switching Loss Test Result

By optimizing ProVCD™ with a turn-off profile *(I_{OFF1} = 15 A, T_{OFF1} = 81.25 ns; I_{OFF2} = 3.54 A)*, the resulting waveforms are shown below. This configuration achieves a reduced E_{OFF} of 15.47 mJ, corresponding to a 43% reduction compared to the TVMD benchmark (27.3 mJ), without any increase in peak voltage (V_{PEAK}).
The optimized turn-off profile also results in increased dI/dt and dV/dt, as observed in the waveform, indicating a faster transition while maintaining controlled voltage stress within the defined limits.

CH5 (Orange) – I_{DS}, CH2(Blue) – I_{GS}, CH3(Red) – V_{DS}, Math1 (Purple) – E_{ON}, Ref1 (Gray) – TVMD V_{DS}, Ref2 – TVMD I_{DS}

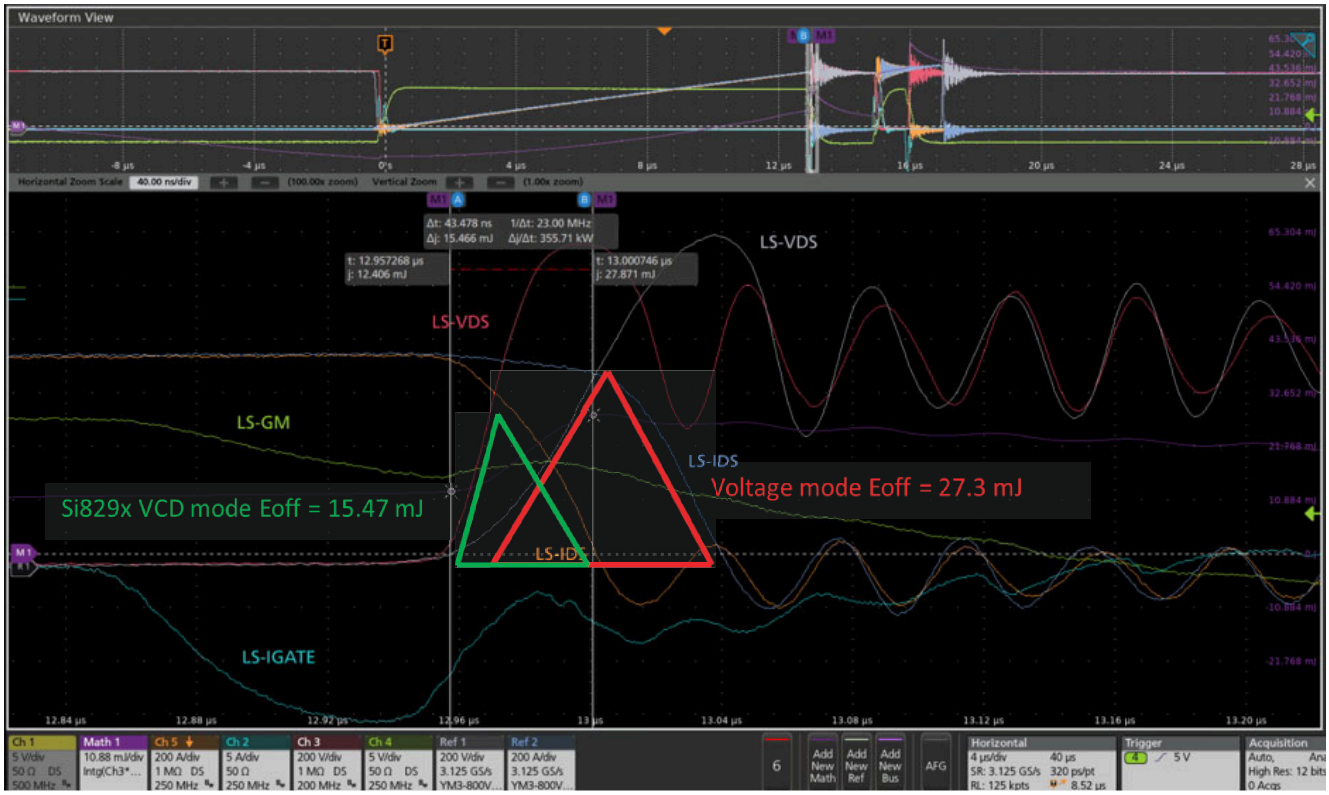


Figure 26. ProVCD™ Turn-Off DPT Waveforms Under 800 V, 800 A

9.2. SiC Module Variant ProVCD™ Test Result Summary

To further understand the performance of Si829x ProVCD™ across different SiC module platforms, the table below summarizes the achievable switching loss reduction on three representative modules: the Wolfspeed XM3, and Wolfspeed YM3. To ensure a fair comparison, all tests were performed under the same operating conditions of 800 V dc bus voltage and 800 A drain current (I_{DS}).

For each module, the traditional voltage-mode driving (TVMD) benchmark was established by optimizing the turn-on and turn-off gate resistors under worst-case operating conditions while maintaining compliance with the module's data sheet voltage, current, and safe operating area (SOA) limits. The reported ProVCD™ performance therefore reflects the additional optimization potential achievable through dynamic gate shaping beyond what can be obtained with a fully optimized conventional gate-drive solution.

Table 6. Si829x ProVCD™ DPT Test Result Summary Under V_{DS} = 800 V, I_{DS} = 800 A

Parameter	EAB450M12XM3	ECB2R1M12YM3
Internal gate resistance R_G (Ω)	2.5	0.5
Total gate charge Q_G (nQ)	1330	1696
Si829x ProVCD™ turn-on E_{ON} reduction	10%	51%
Si829x ProVCD™ turn-off E_{OFF} reduction	14%	43%

10. Observations and Conclusions

The Si829x ProVCD™ enables dynamic gate shaping to optimize switching performance across a wide range of SiC power modules. Double-pulse test results demonstrate measurable reductions in E_{ON}, E_{OFF}, turn-on current overshoot, and turn-off voltage overshoot over varying load conditions, temperatures, and module platforms.

While the profiles in this report were optimized primarily for switching loss or overshoot reduction, resulting in higher dV/dt and dI/dt, ProVCD™ provides the flexibility to balance efficiency, overshoot, EMI, and system robustness through independently programmable multi-stage current levels and high-resolution timing control.

This capability makes Si829x ProVCD™ particularly well suited for EV traction inverter applications, where maximizing efficiency and reliability while meeting EMI requirements is critical.

For more information, refer to the following documents:

- “AN1446: Si829x Technical Reference Manual”
- “AN1453: Si829x ProVCD™ Optimization for Switching Loss Reduction”
- “AN1455: Optimizing EMI Performance of Si829x ProVCD™: Analysis and Test Results”.

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