DATA SHEET

SKY66052-11: 3300 to 4200 MHz Wide Instantaneous Bandwidth High-Gain Linear Driver Amplifier

Applications

- 4G LTE and 5G NR TDD systems
- Supports 3GPP Bands B42, B43, n77, and n78
- Driver amplifier for massive MIMO, macro- and micro-base stations

Features

- Adjustable gain up to 37 dB
- Wide instantaneous signal bandwidth: 200 MHz
- High linearity: –40 dBc open loop ACLR at +10 dBm (100 MHz 5G, 8.5 dB PAR signal)
- High linear output power up to +19 dBm
- Fast turn-on time: 0.7 µs typical
- Internally matched input and output return loss to 50 Ω system
- Integrated active bias: performance compensated over temperature
- Integrated enable on/off function: PA_{EN} = 1.8 V logic
- Single supply voltage: 5.0 V
- Compact 16-pin, 3.0 x 3.0 x 0.85 mm package (MSL3, 260 °C per JEDEC-J-STD-020)
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Description

The SKY66052-11 is a wide instantaneous bandwidth, fully input/output matched power amplifier (PA) with high gain and linearity.

The compact PA is designed for 4G LTE and 5G NR TDD systems operating from 3300 to 4200 MHz. The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation. A block diagram is shown in Figure 1.

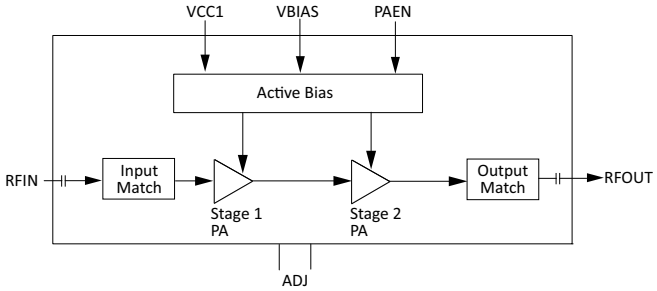


Figure 1. Functional Block Diagram

The SKY66052-11 is part of a pin-to-pin compatible family of driver PAs, refer to Table 1. The device package and pinout are shown in Figure 2. Signal pin assignments and functional pin descriptions are described in Table 2.

Table 1. Pin-to-Pin Compatible Driver PA Family

Part Number	Frequency (MHz)	3GPP / 5G Band	Gain
SKY66041-11	2300 to 2700	B7, B38, B40, B41, n41	30
SKY66051-11	2300 to 2700	B7, B38, B40, B41, n41	>35
SKY66042-11	3300 to 4100	B42, B43, n77, n78	30
SKY66052-11	3300 to 4200	B42, B43, n77, n78	>35

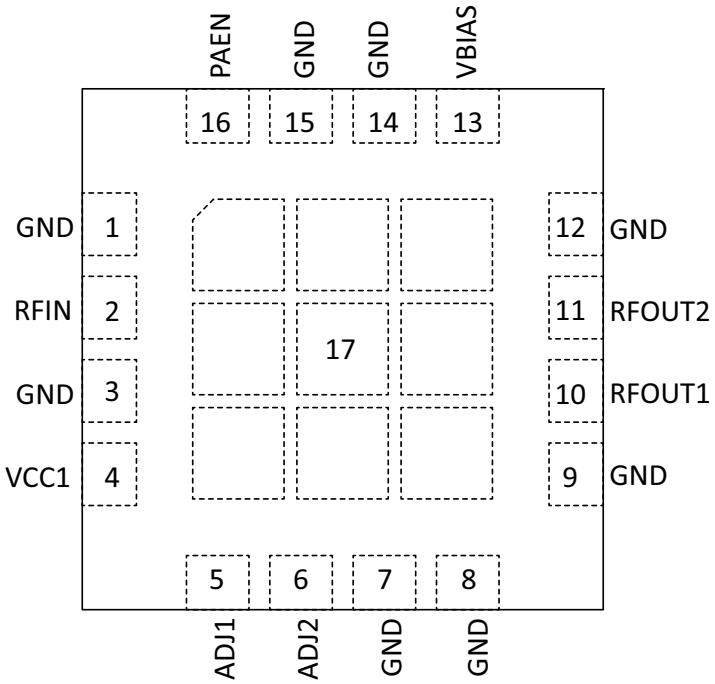


Figure 2. Pinout (Top View)

Table 2. Pin Descriptions[1]

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	10	RFOUT1	RF output port 1
2	RFIN	RF input port	11	RFOUT2	RF output port 2
3	GND	Ground	12	GND	Ground
4	VCC1	Stage 1 collector voltage	13	VBIAS	Bias voltage
5	ADJ1	Adjust 1	14	GND	Ground
6	ADJ2	Adjust 2	15	GND	Ground
7	GND	Ground	16	PAEN	PA enable
8	GND	Ground	17	GND	Center ground
9	GND	Ground			

1. The center ground pad must have a low inductance and low thermal resistance connection to the application printed circuit board ground plane.

Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included for both input and output stages, providing excellent gain tracking over temperature and voltage variations.

The SKY66052-11 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the V_{CC1} supply line (pin 4) and V_{BIAS} (pin 13).

Electrical and Mechanical Specifications

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Units
RF input power (CW)	P_{IN}		22	dBm
Supply voltage (V_{CC1} and V_{BIAS})	V_{CC}		6	V
PA enable	V_{EN}		3.6	V
Operating temperature	T_C	–40	+125	°C
Storage temperature	T_{ST}	–55	+150	°C
Junction temperature (For 106 hours MTTF)	T_J		+175	°C
Electrostatic discharge Charged device model (CDM), Class C3 Human body model (HBM), Class 2	ESD		 1000 2000	V

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (V_{CC1} and V_{BIAS})	V_{CC1}, V_{BIAS}	4.75	5	5.25	V
PA enable: ON OFF	PA_{EN}	 1.17 –0.3	 1.8 0	 3.3 0.63	V
PA enable current	I_{ENABLE}		5	10	µA
Operating frequency	f	3300		4200	MHz
Operating temperature	T_C	–40	+25	+105	°C

Table 5. Electrical Specifications[1]

(V_{CC1} = V_{BIAS} = 5 V, PA_{EN} = 1.8 V, f = 3750 MHz, T_C = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		3300		4200	MHz
Small signal gain	|S21|	P_{IN} = –30 dBm	38	39.5		dB
Gain @ +15 dBm	|S21|@+15 dBm	P_{OUT} = +15 dBm	38	39.5		dB
Input return loss	|S11|	P_{IN} = –20 dBm	11	15		dB
Output return loss	|S22|	P_{IN} = –20 dBm	7.5	11		dB
Reverse isolation[2]	|S12|	P_{IN} = –30 dBm		45		dB
ACLR @ +15 dBm	ACLR	P_{OUT} = +15 dBm (100 MHz LTE, 8.5 dB PAR signal)		–35	–34	dBc
ACLR @ +10 dBm	ACLR	P_{OUT} = +10 dBm (100 MHz LTE, 8.5 dB PAR signal)		–45		dBc
Output power at 1 dB gain compression	P1dB	CW, reference to small signal gain (P_{IN} = –30 dBm)	+28	+29		dBm
Output power at 3 dB gain compression[2]	P3dB	CW, reference to small signal gain (P_{IN} = –30 dBm)		+30		dBm
Second harmonic	2fO	CW, P_{OUT} = +15 dBm		–52	–47.5	dBc
Third harmonic	3fO	CW, P_{OUT} = +15 dBm		–52		dBc
Quiescent current	Icq	No RF signal		88	100	mA
Turn-on time[3]	tON	Measured from 50% PA enable voltage level to 90% of RF amplitude		0.7	0.95	µs
Power dissipation (T_{CASE} = 105 °C, P_{OUT} = +15 dBm)[2]	P_D			0.6		W
Device thermal resistance (T_{CASE} = 105 °C, P_{OUT} = +15 dBm)[2]	q_{JC}			56.5		°C/W

1. Performance is assured only under the conditions listed in this table.
2. Not tested in production. Verified by design.
3. RF turn-on time is measured from the time the PA enable reaches 50% of PA enable “on” level to the time at which the RF output power achieves 90% of the average steady-state “on” level.

Evaluation Board Description

An evaluation board (EVB) is used to test the performance of the SKY66052-11 driver amplifier. An EVB schematic is provided in Figure 3. Table 6 provides the Bill of Materials list for components optimized for 3300 to 4200 MHz operation.

An EVB assembly drawing is shown in Figure 4. Board layer details are shown in Figure 5. Layer detail physical characteristics are noted in Figure 6.

Evaluation Board Test Procedure

Turn-On Sequence

1. Connect 50 Ω test equipment or load to the input and output RF ports of the evaluation board.
2. Connect the dc ground.
3. Connect all V_{CC1} and V_{BIAS} lines to a +5 V supply. Connect PA_{EN} to a 1.8 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 1.8 V PA_{EN}.
5. Apply RF signal data at –30 dBm and observe that the gain of the device is approximately 39.5 dB and begin measurements.

Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PA_{EN} (set to 0 V).
3. Turn off all V_{CC} and V_{BIAS} lines.

Note: It is important to adjust the V_{CC} voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

Circuit Design Considerations

The following considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66052-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.
- Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board.
- Multiple vias to the grounding layer are required.

Note: A poor connection between the ground pad and ground increases junction temperature (T_J), which reduces the life of the device.

Application Circuit Notes

Center Ground (Pin 17): It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

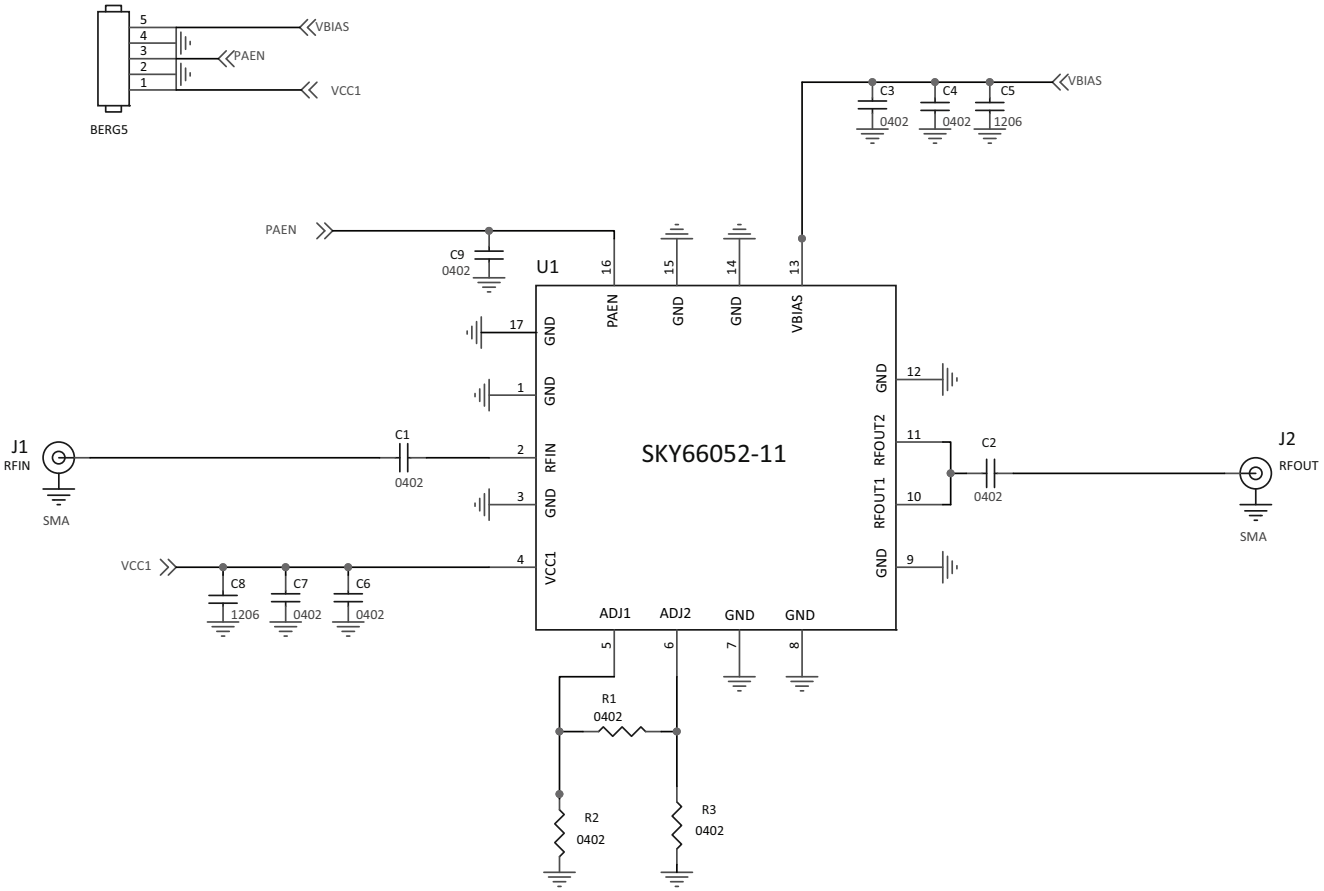
GND (Pins 1, 3, 7, 8, 9, 12, 14, 15): Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

V_{BIAS} (pin 13): The bias supply voltage for each stage, nominally set to +5 V.

RF_{OUT1}, RF_{OUT2} (pins 10, 11): Amplifier RF output pin (Z_O = 50 Ω). The module includes an internal dc blocking capacitor. All impedance matching is provided internal to the module.

V_{CC1} (pin 4): Supply voltage is nominally set to 5 V. Bypass and decoupling capacitors C3 through C8 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RF_{IN} (pin 2): Amplifier RF input pin (Z_O = 50 Ω). All impedance matching is provided internal to the module.



ADJ1, ADJ2 (pins 5 and 6) - Pi or T attenuator network can be added here to adjust the gain.

Figure 3. Evaluation Board Schematic

Table 6. Evaluation Board Bill of Materials

Component	Description	Size
C1, C2	Ceramic capacitor, 15 pF, ±5%, C0G, 50 V	0402
C3, C7, C9	Ceramic capacitor, 100 pF, ±5%, C0G, 50 V	0402
C4, C6	Ceramic capacitor, 1 µF, ±10%, X5R, 16 V	0402
C5, C8	Ceramic capacitor, 10 µF, ±10%, X7R, 16 V	1206
R1	Resistor, 0 Ω, 0.063 W	0402
R2	DNI	0402
R3	DNI	0402

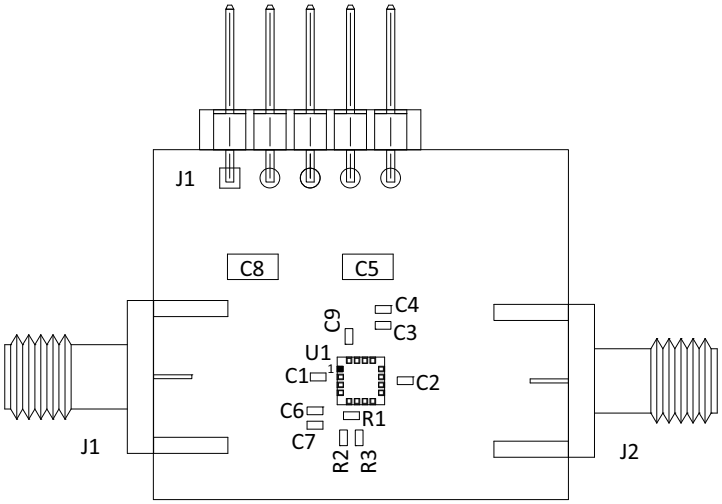


Figure 4. Evaluation Board Assembly Drawing

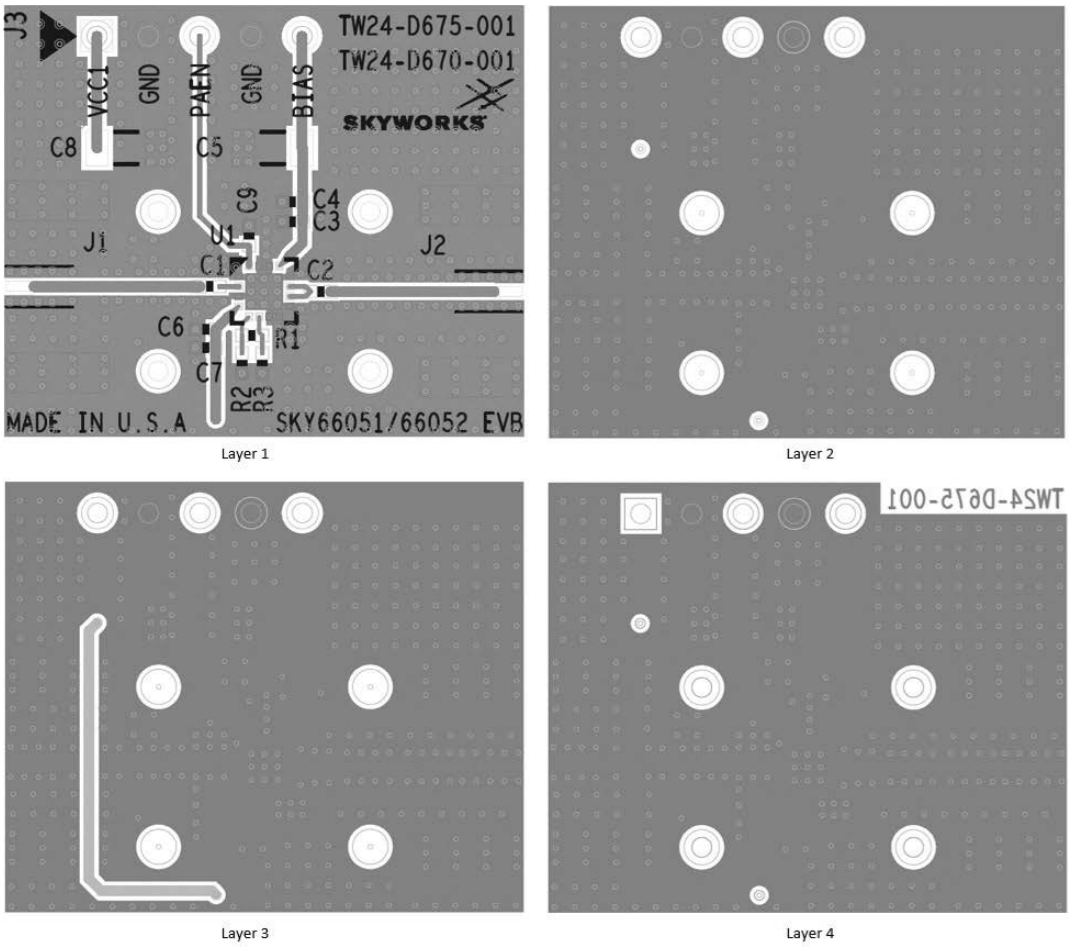


Figure 5. Board Layer Details

100-OHM TRACE	50-OHM TRACE	CROSS SECTION	NAME	THICKNESS	MATERIALS
	TOL: +/-5%				
W=N/A	W=0.520mm		TMASK	0.020mm	SOLDER RESIST
			L1	0.047mm	FINISHED Cu.
S=N/A	CPW = 0.200mm	CORE	DIELECTRIC	0.422mm	RO4350B
			L2	0.018mm	Cu-0.5oz.
		PREPREG	DIELECTRIC	0.528mm	FR4 (4.34)
			L3	0.018mm	Cu-0.5oz.
W=N/A	W=N/A	CORE	DIELECTRIC	0.422mm	FR4 (4.34)
			L4	0.047mm	FINISHED Cu.
S=N/A	CPW = N/A		BMASK	0.020mm	SOLDER RESIST
			TOTAL THICKNESS	1.542mm	TOL: +/- 10%

Figure 6. Layer Detail Physical Characteristics

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66052-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead- or lead-free soldering. For additional information, refer to the Skyworks Application Note, “PCB Design & SMT Assembly/ Rework Guidelines for MCM-L Packages,” document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

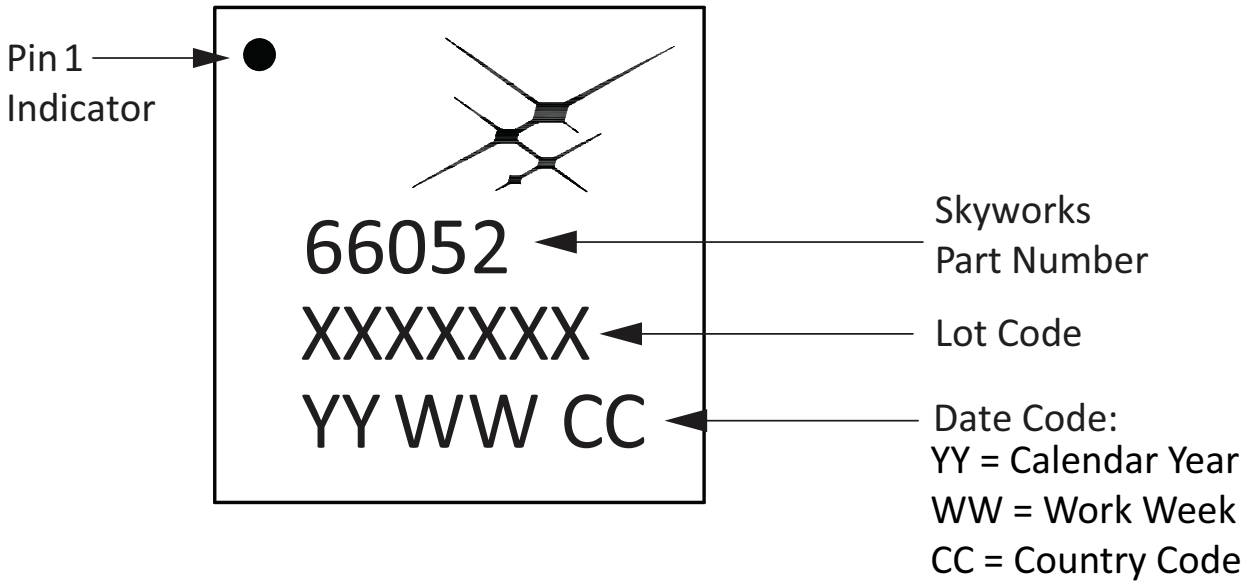
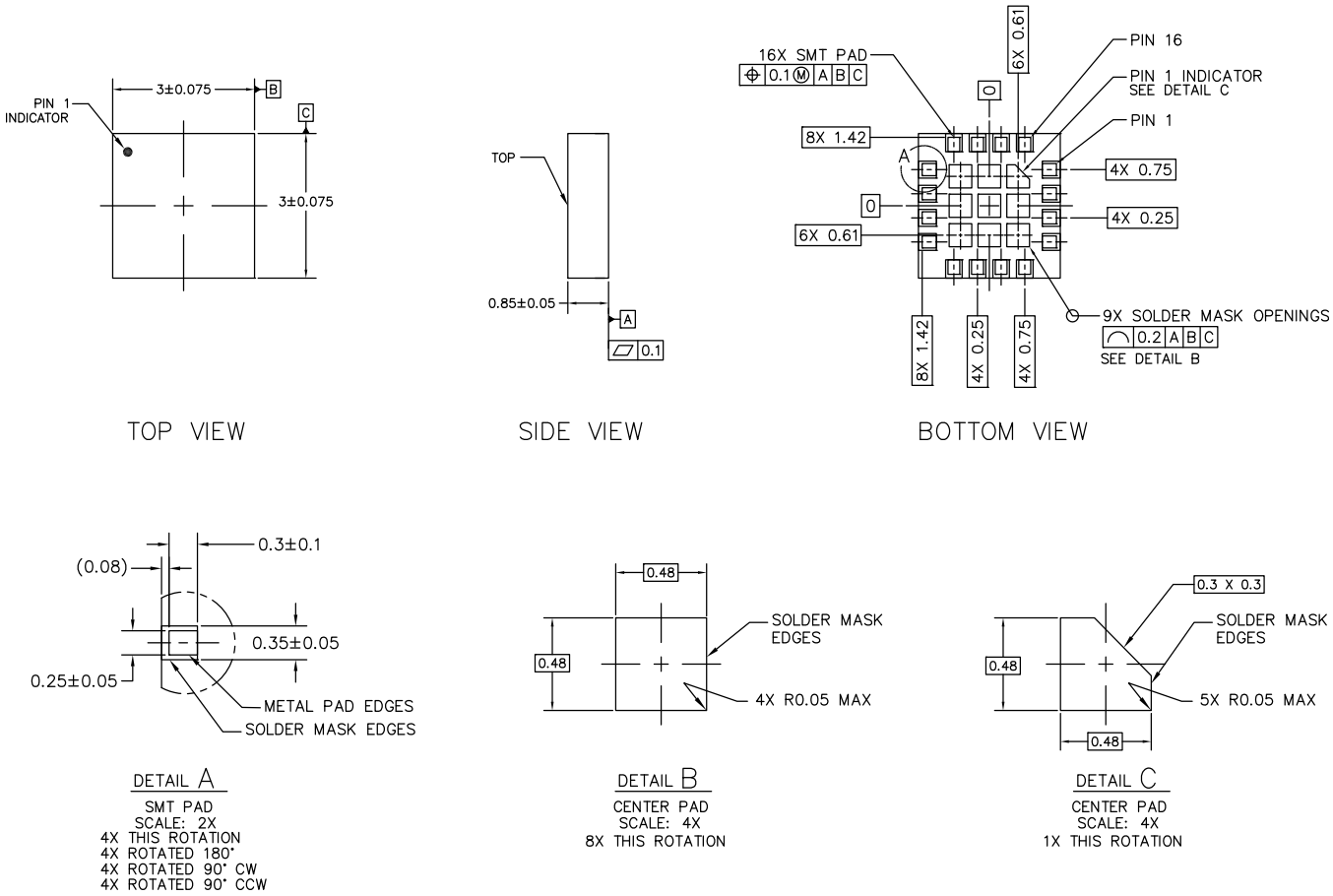


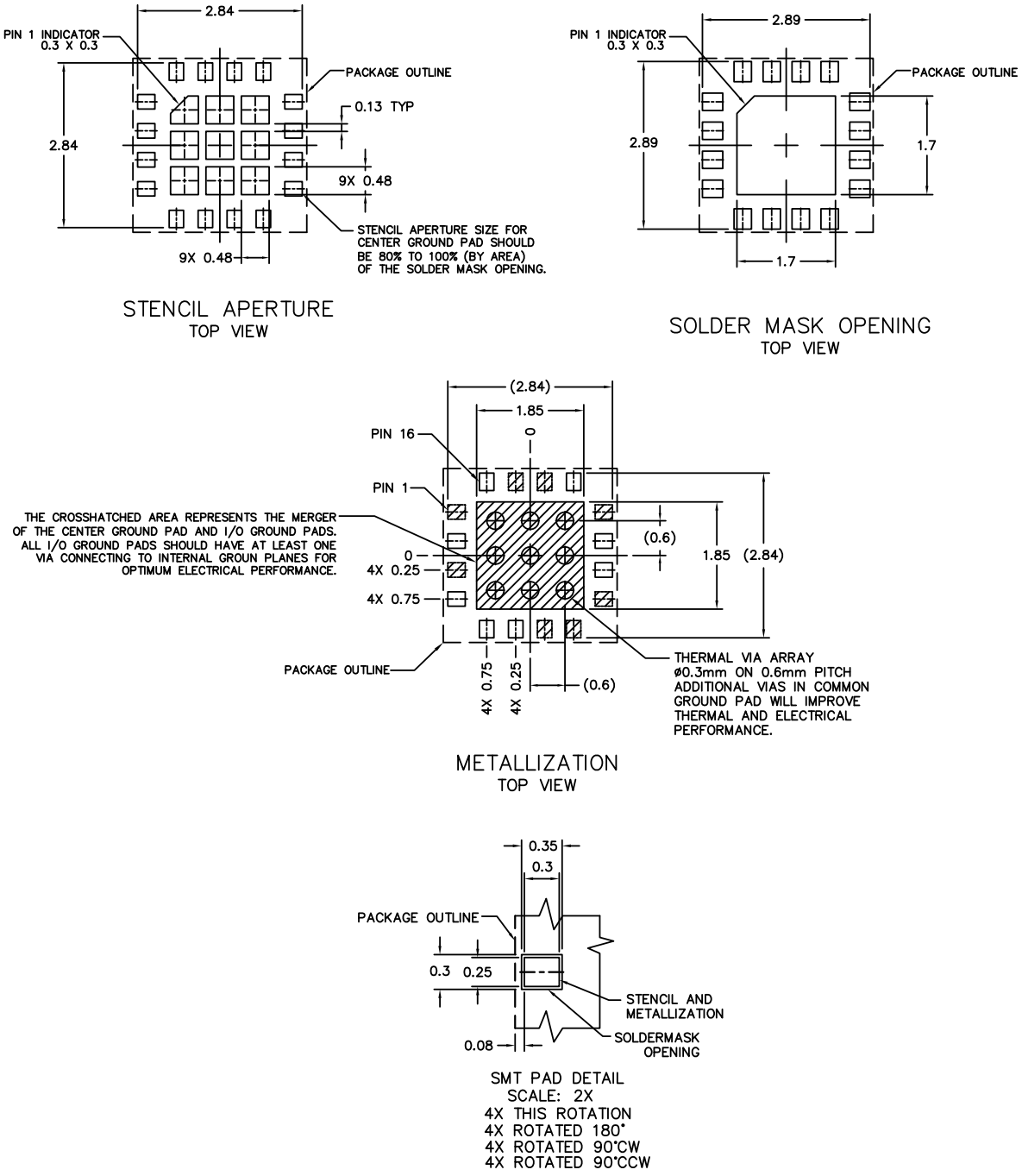
Figure 7. Typical Part Marking



NOTES: UNLESS OTHERWISE SPECIFIED.

1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DIMENSIONS ARE IN MILLIMETERS
3. PAD DEFINITIONS PER DETAILS ON DRAWING.

Figure 8. Package Dimensions



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC–4761 TYPE VII VIAS. 30–35UM Cu THICKNESS IS RECOMMENDED.

Figure 9. PCB Layout Footprint

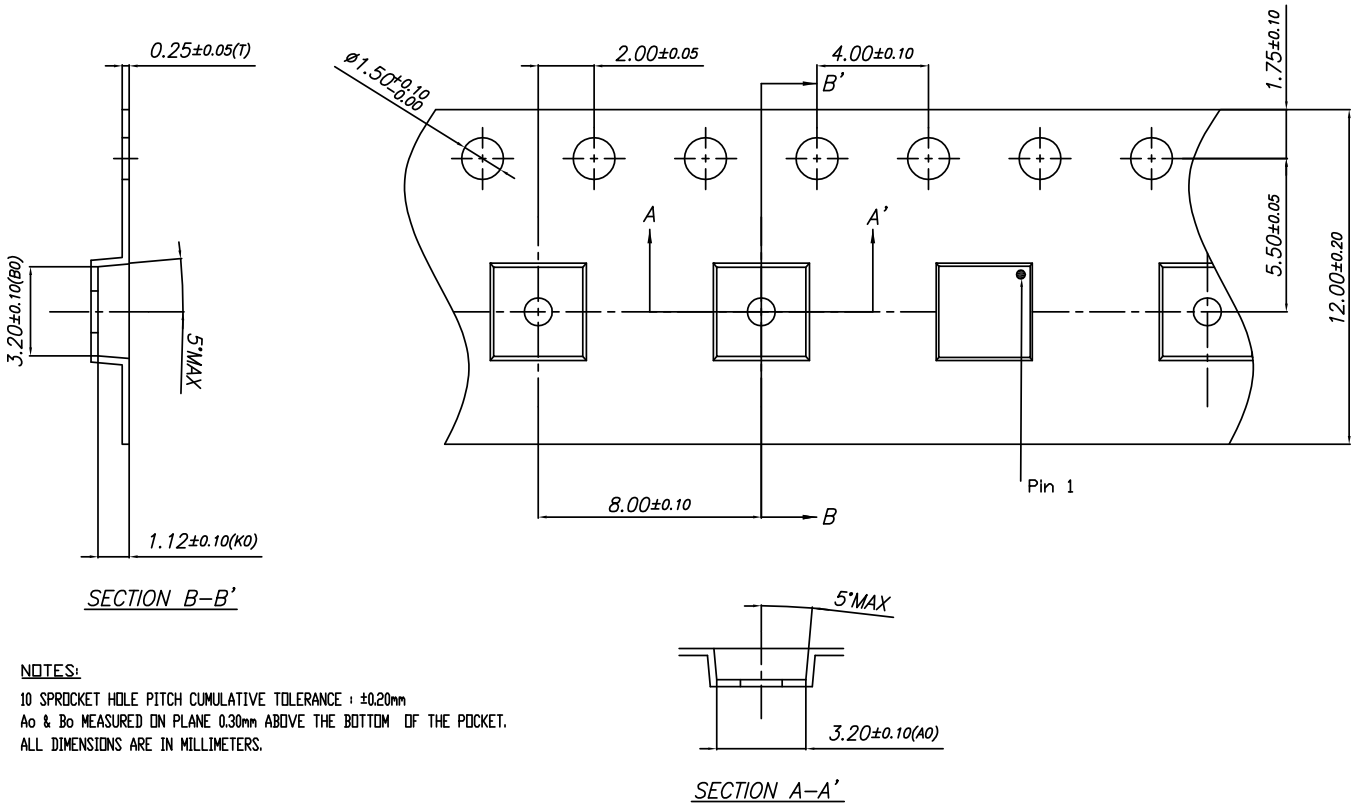


Figure 10. Tape and Reel Information

Ordering Information

Part Number	Description	Evaluation Board Part Number
SKY66052-11	3300 to 4200 MHz Wide Instantaneous Bandwidth High-Gain Linear Driver Amplifier	SKY66052-11EK1