DATA SHEET

# SKY76206-21: Mono Low-Power Multi-Level Class D Audio Amplifier IC

## Applications

- Wireless earbuds
- Wireless headphones
- Active noise cancellation (ANC) circuits
- Portable electronics

## Features

- Filterless multi-level Class D output
- Low power consumption:
  - Quiescent power of 800 µW @ 1.2 V
  - Standby power ($I^2C$ activity) of 60 µW @ 1.2 V
  - Reset power <4 µW
- High output efficiency:
  - 82% (62 mW output to 16 Ω)
  - 88% (100 mW output to 16 Ω)
- High quality audio performance:
  - DNR > 111 dB (A-weighted)
  - THD+N: –84 dB
  - PSRR: 94 dB at 20 kHz
  - Pop and click suppression <–76 $dBV_{PK}$
- Low latency: < 5 µs
- Supply voltage inputs:
  - VBAT (+2.3 V to +4.9 V)
  - VDDIO (+1.2 V to +1.8 V)
- Internally-generated low-voltage supplies
- Audio turn-on or turn-off time: 1.8 ms
- Operating modes:
  - Reset
  - Standby
  - Audio normal-gain mode: 0 dB
  - Audio high-gain mode: +6 dB
  - Fault
- Pulse density modulated (PDM) interface:
  - 3.072 MHz PDM clock, mono 1-bit PDM data
  - 3.072 MHz PDM clock, stereo 1-bit PDM data
  - 3.072 MHz PDM clock, 1.5-bit mono PDM data
  - 6.144 MHz PDM clock, 1.5-bit stereo PDM data

## Features

- Serial audio interface (SAI):
  - Support for 44.1 kHz, 48 kHz and 96 kHz 32-bit data
  - Support for $I^2S$ and left justified data formats
  - EN/WS pin used for word select
- Clock system:
  - Audio path clock derived from PDM or SAI clock input
  - Autonomous system clock for $I^2C$ configuration without a PDM or SAI clock present
- Digital control:
  - RESET_B to reset (active low)
  - EN/WS to enable if not in SAI mode (active high)
  - System and amp configuration (via $I^2C$)
  - Fault code read and clear (via $I^2C$)
- Host notification:
  - IRQ_B interrupt request (active low)
- Multi-level output driver/amplifier:
  - Programmable edge-rate control
  - Programmable non-overlap timing
  - Thermal protection
- Other features:
  - $I^2C$ address pin to enable stereo designs
  - On-chip supply and temperature fault protection
- Small PCB footprint, 1.54 mm x 1.54 mm x 0.471 mm package
  - 15-pin wafer-level chip-scale package (WLCSP), 0.35 mm pin pitch
  - MSL1 @ 260 °C per JEDEC J-STD-020
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance

## Block Diagram

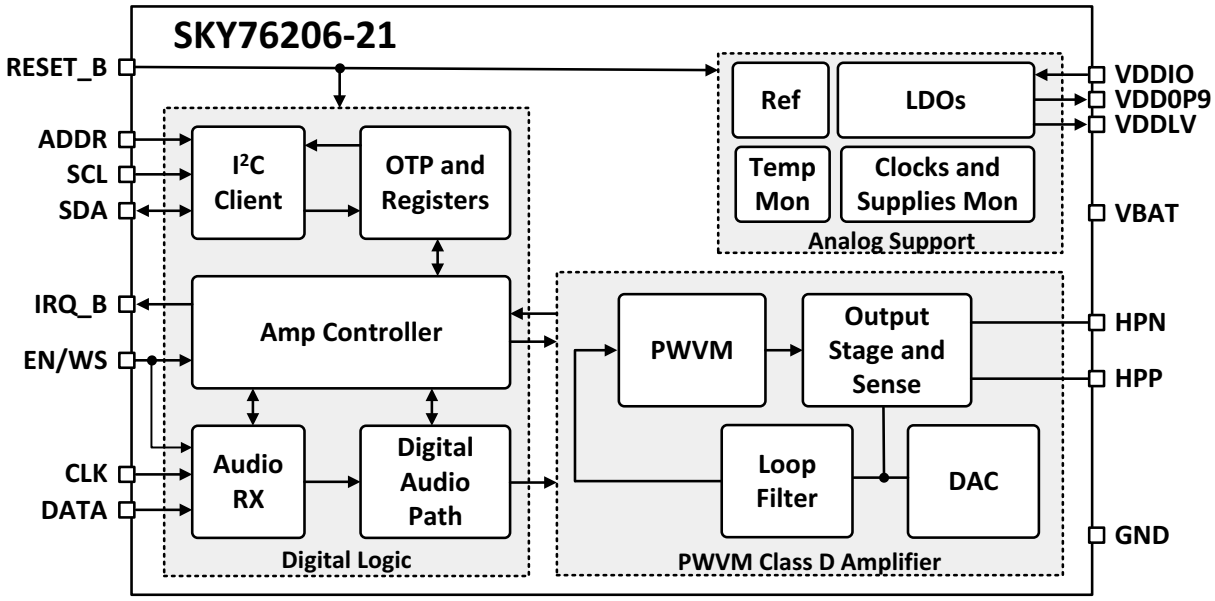



**Figure 1. Functional Block Diagram**

## Description

The Skyworks SKY76206-21 Mono Low-power Multi-Level Class D Audio Amplifier IC is an innovative Class DG amplifier that delivers world class audio performance in a compact package with ultra-low quiescent power levels, and is ideal for portable and wearable electronics.

Unlike most Class D amplifiers on the market, the SKY76206-21 directly processes a digital audio input to create its audio output. The audio signal is reproduced with very high fidelity, even in dense electronics with multiple nearby radio transmitters. The device is optimized for efficiency at low output power levels where most Class D amplifiers are highly inefficient, making it the right fit for wearables with high sensitivity speaker drivers. It has a low quiescent power in active mode, and its state-of-the-art pop and click suppression makes transitions into the low power consumption standby mode a seamless experience to the user while preserving battery life.

The SKY76206-21 requires two power inputs. VBAT (+2.3 V to +4.9 V) is commonly connected directly to a lithium-ion battery, avoiding the efficiency losses of a voltage regulator. VDDIO (+1.2 V or +1.8 V) must be a regulated voltage, selected to best match the output voltage levels of the external host microcontroller, driving the $I^2C$, digital audio, and GPIO nets. VDDIO is also the input source for the internal voltage regulator which generates two regulated voltages, VDD0P9 (+0.9 V) and VDDLV (+0.275 V). Each of these four voltage nets require only an external bulk capacitor adjacent to the pin for normal operation.

The differential audio output pins operate at 3.072 MHz, with a pulse-width and voltage modulated (PWVM) square wave, with a magnitude that varies between VDDLV (+0.275 V), VDD0P9 (+0.9 V), VDDIO, and VBAT. This differential output acts as a charge-pump into an inductive load (speaker driver) to recreate the audio signal. Figure 2 shows this in concept (timing is not to scale) for VDDIO = +1.8 V and VBAT = +3.8 V.

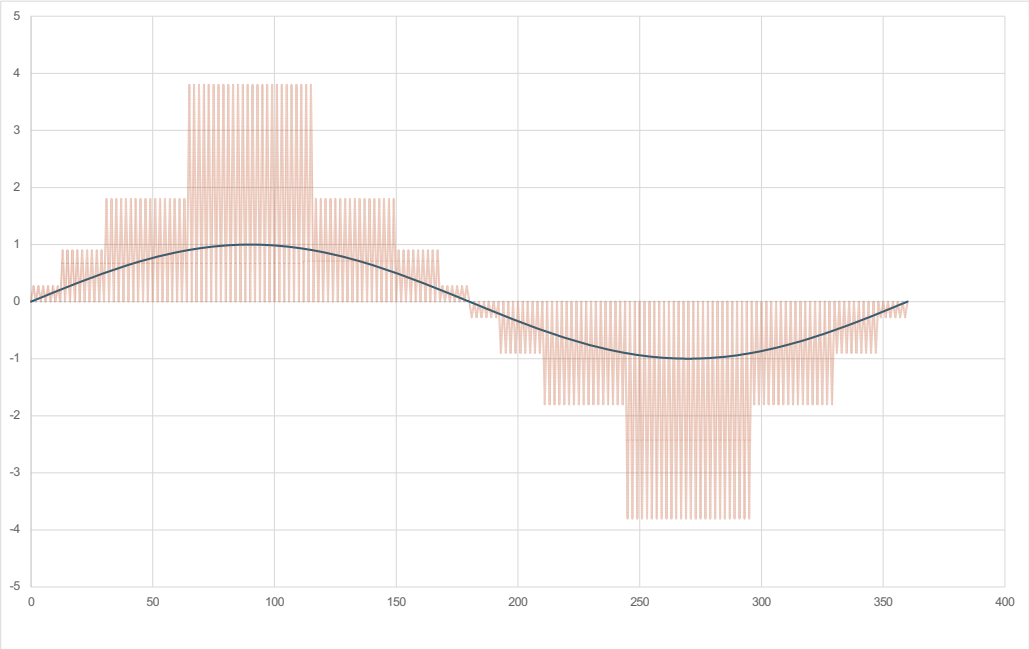



**Figure 2. Concept of SKY76206-21 Class DG Audio Output in Normal-Gain Mode**

The SKY76206-21 is digitally controlled using standard $I^2C$ interface serial data (SDA) and serial clock (SCL) pins. A second SKY76206-21 can share the same $I^2C$ bus by pulling down the ADDR address pin to ground. The ADDR pin enables stereo applications, since the same external microcontroller can control two SKY76206-21 devices, with one $I^2C$ bus and one PDM or SAI bus containing stereo content.

The SKY76206-21 also offers a robust status reporting capability. The IRQ_B interrupt request pin informs the external microcontroller when a status change occurs, prompting the external microcontroller to read status over the $I^2C$ interface.

The SKY76206-21 can support stereo audio streams of both PDM and SAI protocols through the CLK and DATA pins. The EN/WS pin can be programmed to function either as a PDM audio enable (EN) or an SAI word select (WS) input. Otherwise, the EN/WS pin is used to enable or disable audio, such as a mute function that saves power.

## Typical Application Circuit

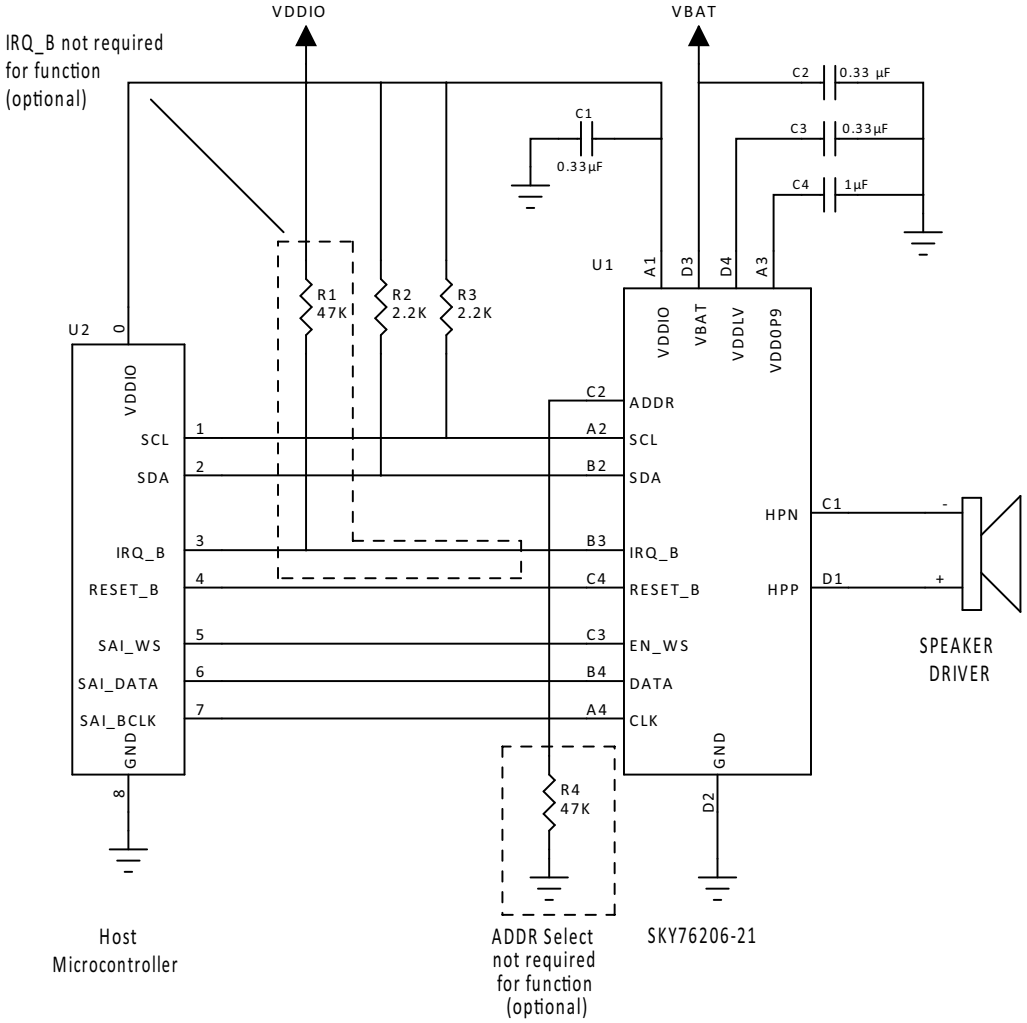



**Figure 3. Typical Application Circuit**

## Pinout

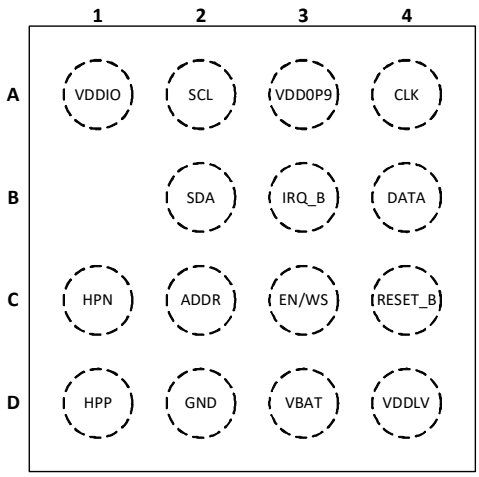



**Figure 4. Pinout (Top View)**

**Table 1. Signal Descriptions**

| Pin | Name | Type | Description |
|---|---|---|---|
| A1 | VDDIO | Power input | Input voltage used as a reference for all digital I/O. Recommend 50 mA source current. Requires a 0.33 µF capacitor to ground (GND). |
| A2 | SCL | Digital I/O | $I^2C$ clock pin, open drain. Requires 2.2 kΩ pull-up to VDDIO. |
| A3 | VDD0P9 | N/A | Internally generated voltage (+0.9 V). Requires a 1 µF capacitor to GND. Cannot be used as a power source for external circuitry. |
| A4 | CLK | Digital input | Digital audio clock input. For PDM, connect to PDMCLK. For SAI, connect to BCLK. |
| B1 | | | No pin |
| B2 | SDA | Digital I/O | $I^2C$ data pin, open drain. Requires a 2.2 kΩ pull-up to VDDIO. |
| B3 | IRQ_B | Digital output | Interrupt request, open drain active low. Requires a 47 kΩ pull-up to VDDIO if connected to external host. |
| B4 | DATA | Digital input | Digital audio data input. For PDM, connect to PDMDAT. For SAI, connect to SAI_DATA. |
| C1 | HPN | Analog output | Headphone output negative (differential to HPP). |
| C2 | ADDR | Digital input | $I^2C$ address select, internally pulled up. Sets the LSB of the 7-bit $I^2C$ device address for the chip. |
| C3 | EN/WS | Digital input | Dual functionality. For PDM, use as audio enable/disable. For SAI, connect to SAI_WS. |
| C4 | RESET_B | Digital input | Reset, active low. Must be driven to VDDIO for device to be in active state. When asserted (active low), keeps the device in lowest power state. |
| D1 | HPP | Analog output | Headphone output positive (differential to HPN). |
| D2 | GND | Ground | Common return net for all signals. |
| D3 | VBAT | Power input | Supply voltage from Li-Ion battery or a regulated supply (+2.3 V to +4.9 V). Recommend 100 mA source current. Requires a 0.33 µF capacitor to GND. |
| D4 | VDDLV | N/A | Internally generated voltage (+0.275 V). Requires a 0.33 µF capacitor to GND. Cannot be used as a power source for external circuitry. |

## Electrical Specifications

For all tables, performance is assured only under the conditions listed and is not invariant over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

**Table 2. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Battery voltage | VBAT | –0.3 | 6 | V |
| I/O voltage | VDDIO | –0.3 | 2.4 | V |
| Digital I/O pins | RESET_B, IRQ_B, EN_WS, SCL, SDA, CLK, DATA | –0.3 | VDDIO+ 0.3 | V |
| Audio output pins | HPP, HPN | –0.3 | 6 | V |
| Short circuit to GND (any pin) | | | Continuous | |
| Storage temperature | TSTG | –55 | +150 | °C |
| Operating temperature (functional only) | TOP | –40 | +85 | °C |
| Lead temperature (10 s) | TJ | | 300 | °C |
| **Electrostatic discharge (ESD)** | | | | |
| Human body model (HBM) R 1 kΩ, C = 100 pF | ESD HBM | –1500[2] | +1500 | V |
| Charged device model (CDM) | ESD CDM | –500[3] | +500 | V |

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.
2. In accordance with ANSI/ESDA/JEDEC JS-001.
3. In accordance with ANSI/ESDA/JEDEC JS-002.

***ESD Handling**: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

**Table 3. DC Supply Voltages**

Test conditions: Audio = 1 kHz into $Z_L$ = 16 Ω + 10 µH, $Fs_{PDM}$ = 3.072 MHz, 1-bit modulation mode, $T_A$ = 25 °C

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Input Supply Voltages** | | | | | |
| VBAT | Normal-gain mode (full performance) | 2.3 | 3.8 | 4.9 | V |
| | High-gain mode | 2.3[1] | 3.8 | 4.9 | V |
| VDDIO | | 1.1 | 1.2 | 1.95 | V |
| **LDO Regulator Output Voltages** | | | | | |
| VDD0P9 | Default voltage[2] | | 0.9 | | V |
| VDDLV | Default voltage[2] | | 0.275 | | V |

1. Maximum audio output voltage is limited and may have higher THD+N than specification (clipped) when VBAT is below typical.
2. VDD0P9 and VDDLV output are designed for internal device use only, cannot be used to power external circuits.

**Table 4. Audio Performance**

Test conditions: VBAT = 3.8 V, VDDIO = 1.2 V, f = 1 kHz, $Z_L$ = 16 Ω + 10 µH or 32Ω + 15 µH, $Fs_{PDM}$ = 3.072 MHz, 1-bit modulation mode, PDM low pass filter = lowest latency (PDM_LPF_SEL=0), default edge rate setting, measured with 20 kHz AES17 filter unless otherwise specified. $T_A$ = 25 °C

| Parameter | Conditions | Normal-Gain Mode | | | High-Gain Mode | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Amplifier gain | $D_{IN}$ = –3 dBFS, amp not clipping, $Z_L$ = 3.2 k Ω | | 0.0 | | | +6.0 | | dB |
| Maximum output voltage | $D_{IN}$ = 0dBFS, amp not clipping | | 1 | | | 2 | | $V_{RMS}$ |
| | | | 0 | | | +6 | | dBV |
| Maximum output power | $D_{IN}$ = 0 dBFS, amp not clipping, $Z_L$ = 16 Ω + 10 µH | | 62.5 | | | 250 | | mW |
| | $D_{IN}$ = 0dBFS, amp not clipping, $Z_L$ = 32 Ω+ 15 µH | | 31.25 | | | 125 | | mW |
| PDM input level for full-scale output | Amp not clipping | | –6 | | | –6 | | dBFS |
| $I^2S$ input level for full-scale output | Amp not clipping | | 0 | | | 0 | | dBFS |
| PDM idle-channel noise | $D_{IN}$ = –132 dBFS @ 1 kHz, A-weighted | | –111 | | | –108 | | dBV |
| $I^2S$ idle-channel noise | $D_{IN}$ = –132 dBFS @ 1 kHz, A-weighted | | –113 | | | –111 | | dBV |
| THD+N[1] | $D_{IN}$ = –3 dBFS @ 1 kHz | | –84 | | | –84 | | dB |
| Output dc offset voltage | $D_{IN}$ = –132 dBFS @ 1 kHz | –100 | 0 | 100 | –100 | 0 | 100 | µV |
| Noise at dc full-scale output | 1.414 Vdc output, A-weighted[2] | | –96 | | | | | dBV |
| | 2.828 Vdc output, A-weighted[2] | | | | | –93 | | dBV |
| Pop and click | All amp enable/disable transitions[2], unweighted | | –76 | | | –74 | | dBVpk |
| Power supply rejection ratio (PSRR) | f = 1 kHz | | 106 | | | 105 | | dB |
| | f = 10 kHz | | 99 | | | 94 | | |
| | f = 20 kHz | | 94 | | | 89 | | |
| Audio turn-on/turn-off time | Amp enable or disable transition | | 1.8 | | | 1.8 | | ms |
| Audio latency: PDM input to analog output | PDM LPF SEL = 0 (low latency mode) | | 4.9 | | | 4.9 | | µs |
| Audio attenuation in standby mode | Enable pin EN/WS = 0 (off) or $I^2C$ commanded | 110 | | | 110 | | | dB |
| Passband ripple | f = 20 Hz to 20 kHz with respect to 1 kHz, low latency mode (PDM LPF SEL = 0) | | ±0.5 | | | ±0.5 | | dB |
| Load resistance operating range | Across HPP and HPN | 11 | | | 11 | | | Ω |
| Load inductance | Across HPP and HPN | 5 | | | 5 | | | µH |
| Load capacitance | Single-ended: HPP to GND and HPN to GND | | | 100 | | | 100 | pF |
| | Differential: HPP to HPN | | | 50 | | | 50 | pF |

1. PDM or SAI. Background DAC calibration disabled for THD+N, full-scale output, and power measurement window.
2. Excludes error triggered events.

**Table 5. Power Consumption and Efficiency**

Test conditions: VBAT = 3.8 V, VDDIO = 1.2 V, f = 1 kHz, $Z_L$ = 16 Ω + 10 µH, $Fs_{PDM}$ = 3.072 MHz, 1-bit modulation mode, $T_A$ = +25 °C

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VBAT-only power consumption | All other supply voltages and I/O = 0 V | | 0.4 | | µW |
| Reset power consumption | RESET_B = 0; all supplies up, all I/O = 0 V | | 3.3 | | |
| Standby power consumption | $I^2C$ activity, all digital inputs = 0 V | | 54 | | |
| Quiescent power[1] ($D_{IN}$ = –132 dBFS @ 24-bit LSB) | VDDIO = 1.2 V, normal-gain mode, PDM | | 780 | | |
| | VDDIO = 1.2 V, normal-gain mode, SAI | | 730 | | |
| | VDDIO = 1.2 V, high-gain mode, PDM | | 800 | | |
| | VDDIO = 1.2 V, high-gain mode, SAI | | 720 | | |
| | VDDIO = 1.8 V, normal-gain mode, SAI | | 1100 | | |
| Incremental efficiency ($P_{OUT}/P_{IN}$) at 100 µW | Normal-gain mode, $Z_L$ = 16 Ω + 10 µH, $D_{IN}$ = –28 dBFS | | 34 | | % |
| | High-gain mode, $Z_L$ = 16 Ω + 10 µH, $D_{IN}$ = –34 dBFS | | 36 | | % |
| Incremental efficiency ($P_{OUT}/P_{IN}$) at 62 mW | Normal-gain mode, $Z_L$ = 16 Ω + 10 µH, $D_{IN}$ = 0 dBFS | | 82 | | % |
| Incremental efficiency ($P_{OUT}/P_{IN}$) at 100 mW | High-gain mode, $Z_L$ = 16 Ω + 10 µH, $D_{IN}$ = –4 dBFS | | 88 | | % |

1. Includes the out-of-band noise power from the host PDM signal.

**Table 6. Digital I/O**

Test conditions: VBAT = 3.8 V, VDDIO = 1.2 V, unless otherwise specified. $T_A$ = 25 °C

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input voltage high (VIH) | Threshold for valid input high | 0.7*VDDIO | | | V |
| Input voltage low (VIL) | Threshold for valid input low | | | 0.3*VDDIO | V |
| Output voltage low (VOL) | IOL = –100 µA | | 0.012 | 0.2 | V |
| Output current low (IOL) | VOL = 0.4 V, 1 mA drive strength setting | 1 | 2.3 | 5.8 | mA |
| | VOL = 0.4 V, 2 mA drive strength setting | 2 | 6.5 | 10.4 | mA |
| | VOL = 0.4 V, 4 mA drive strength setting | 4 | 9.6 | 13 | mA |
| | VOL = 0.4 V, 8 mA drive strength setting[1] | 8 | 13.5 | 16.7 | mA |
| Input leakage current | VIN = 0 to VDDIO | -4 | | 4 | µA |
| Input hysteresis | VDDIO = 1.2 V | | 280 | | mV |
| I/O pad capacitance[2] | Digital pins (except RESET_B) | | 3 | 5 | pF |
| | RESET_B pin | | 5.5 | 7.5 | pF |

1. Default setting
2. Total pad input capacitances to GND and VDDIO. AC capacitance at 1 MHz.

## Typical Performance Characteristics

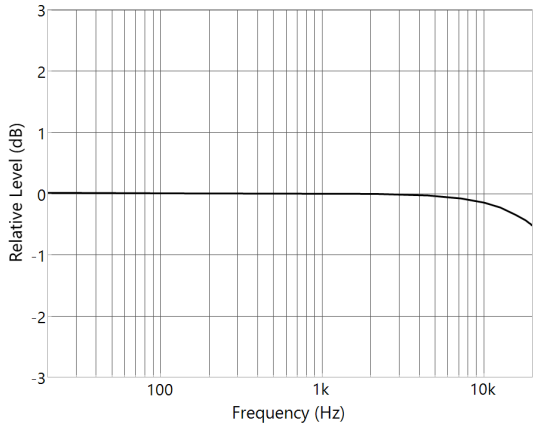



**Figure 5. Frequency Response I²S 48 kHz 16 Ω**

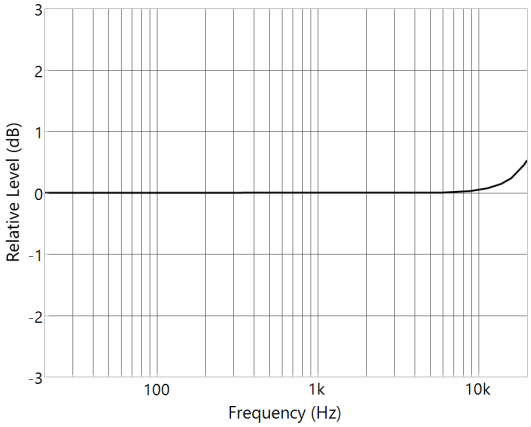



**Figure 6. Frequency Response PDM 1-Bit 3 MHz 16 Ω**

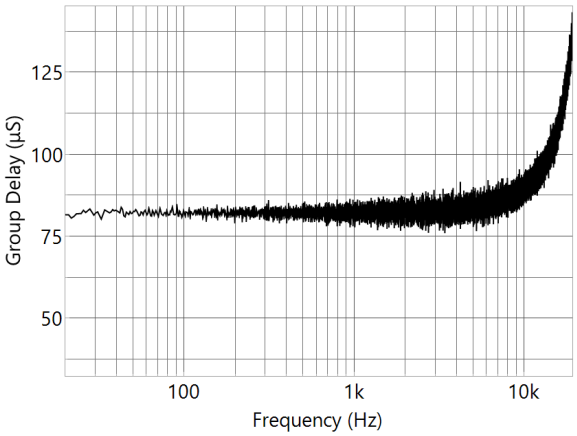



**Figure 7. Group Delay I²S 48 kHz 16 Ω**

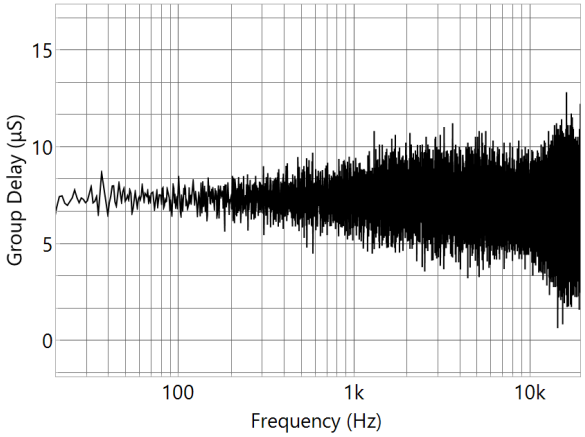



**Figure 8. Group Delay PDM 1-Bit 3 MHz 16 Ω**

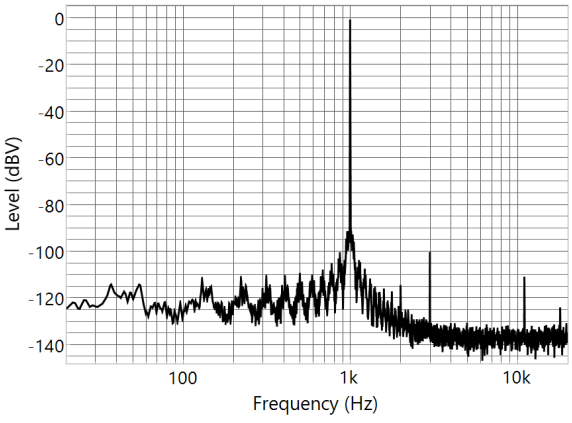



**Figure 9. FFT –2 dBFS PDM 1-Bit 3 MHz 16 Ω**

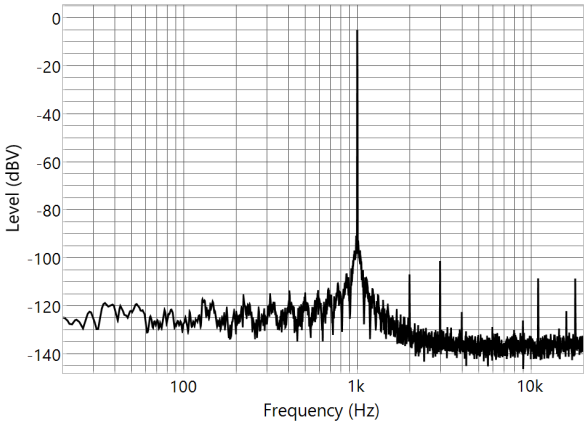



**Figure 10. FFT –2 dBFS PDM 1-Bit 3 MHz 32 Ω**

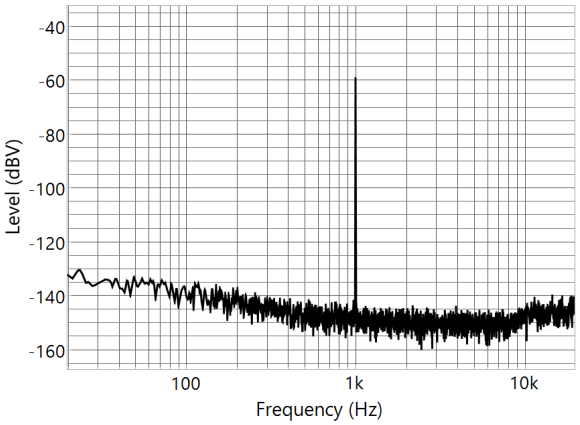



**Figure 11. FFT –60 dBFS PDM 1-Bit 3 MHz 16 Ω**

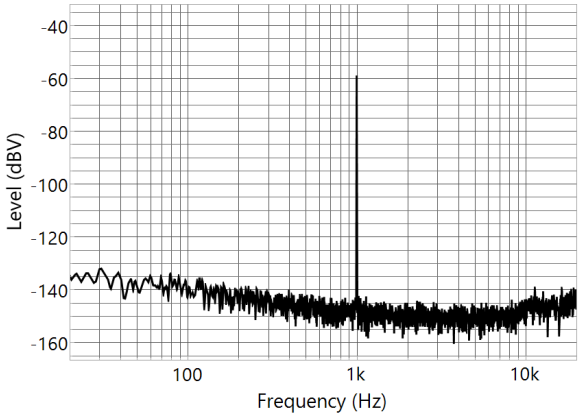



**Figure 12. FFT –60 dBFS PDM 1-Bit 3 MHz 32 Ω**

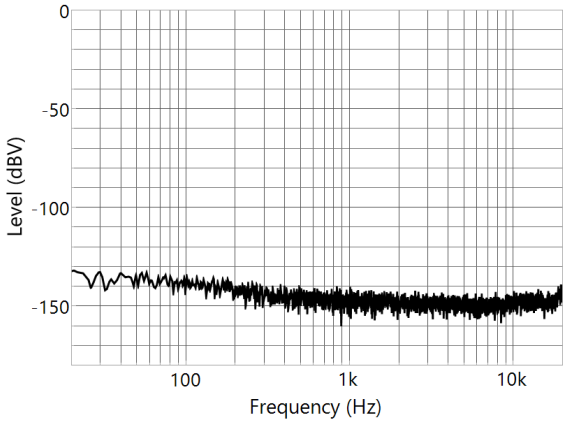



**Figure 13. FFT Dither PDM 1-Bit 3 MHz 16 Ω**

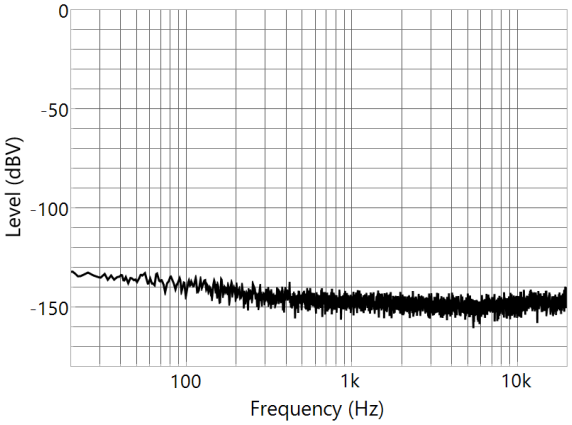



**Figure 14. FFT Dither PDM 1-Bit 3 MHz 32 Ω**

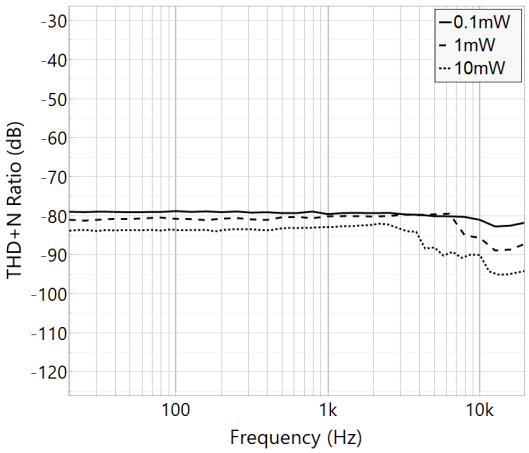



**Figure 15. THD+N versus Frequency PDM 1-Bit 3 MHz 16 Ω**

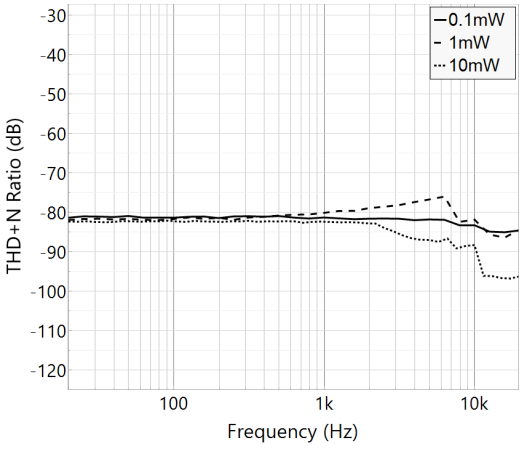



**Figure 16. THD+N versus Frequency PDM 1-Bit 3 MHz 32 Ω**

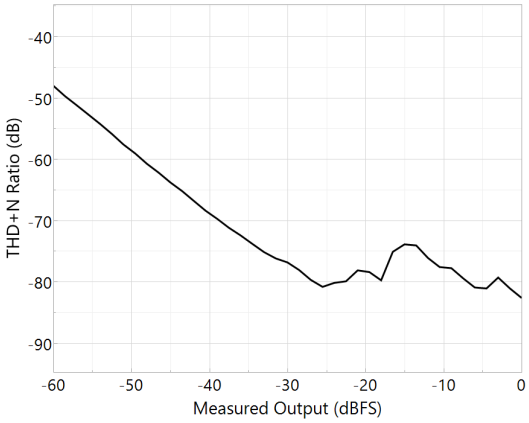



**Figure 17. THD+N versus Output Power 16 Ω**

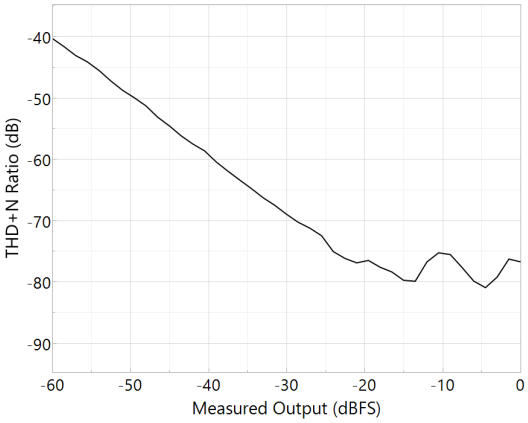



**Figure 18. THD+N versus Output Power 32 Ω**

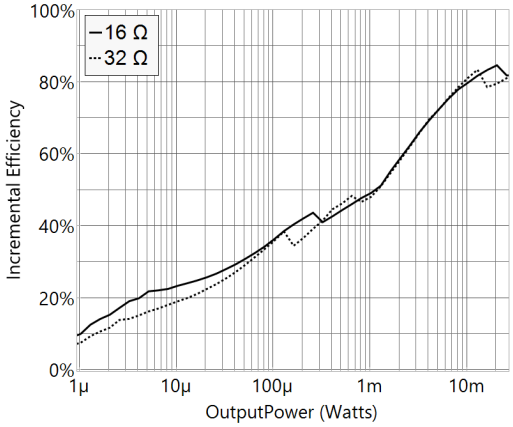



**Figure 19. Efficiency PDM 1-Bit 3 MHz 1.2 V Normal-Gain Mode**

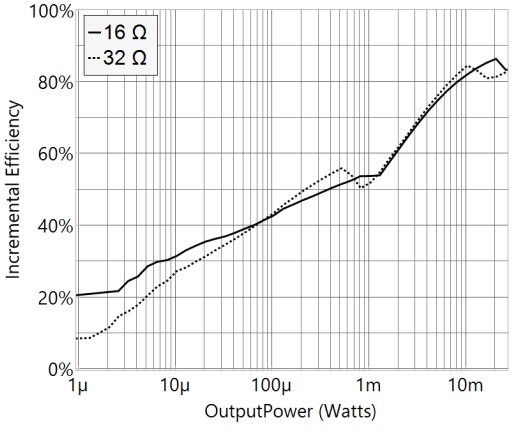



**Figure 20. Efficiency PDM 1-Bit 3 MHz 1.2 V High-Gain Mode**

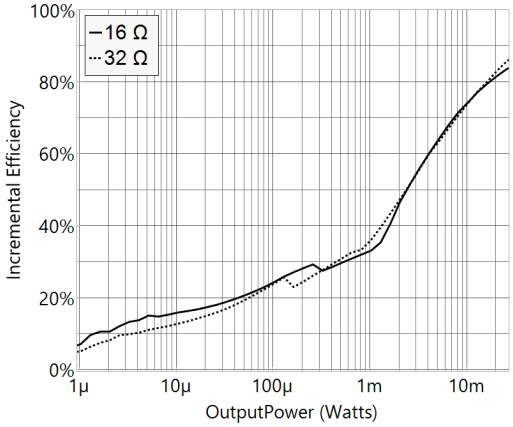



**Figure 21. Efficiency PDM 1-Bit 3 MHz 1.8 V Normal-Gain Mode**

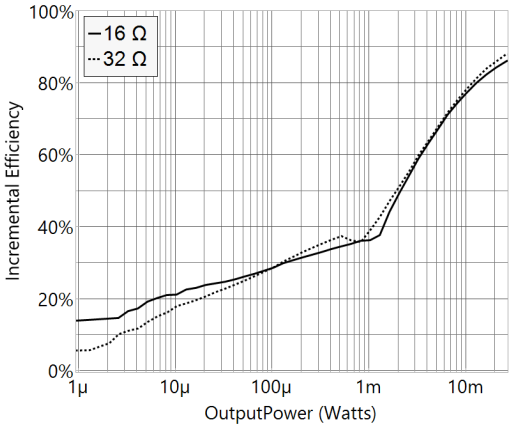



**Figure 22. Efficiency PDM 1-Bit 3 MHz 1.8 V High-Gain Mode**

# Digital Busses

## PDM Timing

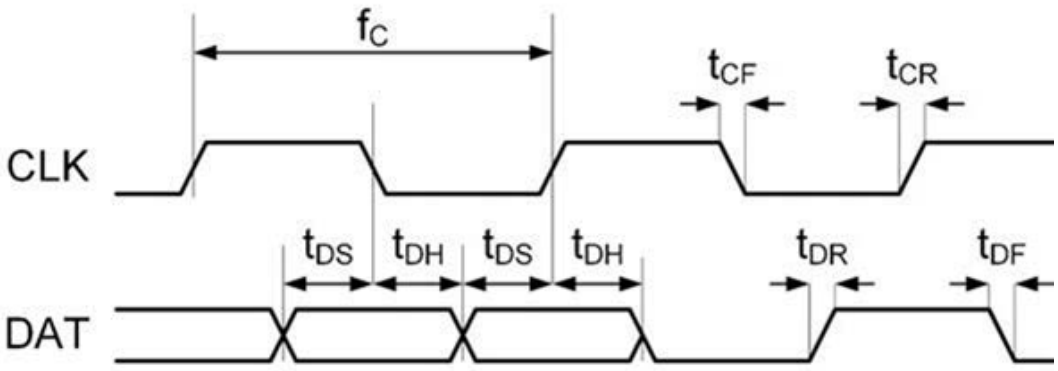



**Figure 23. PDM Timing**

**Table 7. PDM Interface Timing**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | PDM sample rate | | 2.7 | 3.072 | 3.3 | MHz |
| | Class D modulator clock frequency | Set by the input PDM clock frequency | | 3.072 | | MHz |
| fC | CLK frequency | Format = 1-bit or channels = 1 | 2.7 | 3.072 | 3.3 | MHz |
| | | Format = 1.5-bit and channels = 2 | 5.4 | 6.144 | 6.6 | MHz |
| | CLK jitter | TIE, f> = 100 Hz | | | 250 | ps RMS |
| | | Period jitter | | | 10 | ns pkpk |
| | CLK duty cycle | | 45 | | 55 | % |
| tDS | DAT to CLK setup time | | 20 | | | ns |
| tDH | CLK to DAT hold time | | 0 | | | ns |
| tCR | CLK rise time | | | | 10 | ns |
| tCF | CLK fall time | | | | 10 | ns |
| tDR | DAT rise time | | | | 10 | ns |
| tDF | DAT fall time | | | | 10 | ns |

## SAI Timing

See the *NXP® UM11732 I²S bus specification* for details.

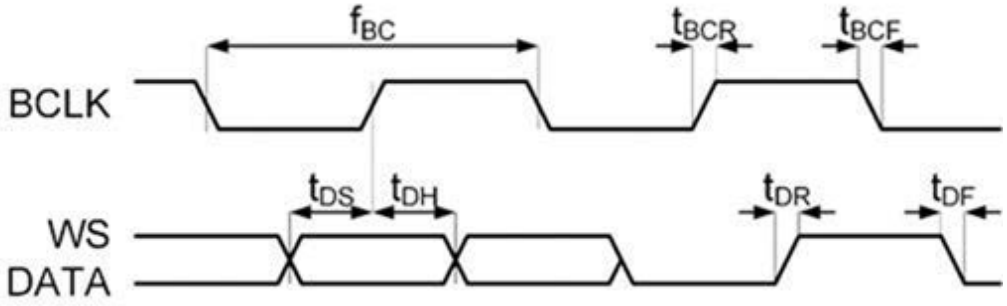



**Figure 24. SAI Timing**

**Table 8. SAI Timing**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fBC | BCLK frequency | Sample rate = 44.1 kHz | 2.7 | 2.82 | 2.9 | |
| | | Sample rate = 48 kHz | 2.9 | 3.072 | 3.2 | MHz |
| | | Sample rate = 96 kHz | 5.8 | 6.144 | 6.4 | MHz |
| fWS | Frame clock | 64 bits per frame | 44.1 | 48 | 96 | kHz |
| tBCDC | BCLK duty cycle | | 45 | | 55 | % |
| bWSDC | WS duty cycle | | 32 | | 32 | Bits |
| tBCR | BCLK rise time | | | | 10 | ns |
| tBCF | BCLK fall time | | | | 10 | ns |
| tDR | WS, DATA rise time | | | | 10 | ns |
| tDF | WS, DATA fall time | | | | 10 | ns |
| tDS | WS, DATA to BCLK setup time | | 30 | | | ns |
| tDH | BCLK to WS, DATA hold time | | 30 | | | ns |

## I²C Timing Requirements

Refer to *UM10204 I²C-bus specification and user manual* for details.

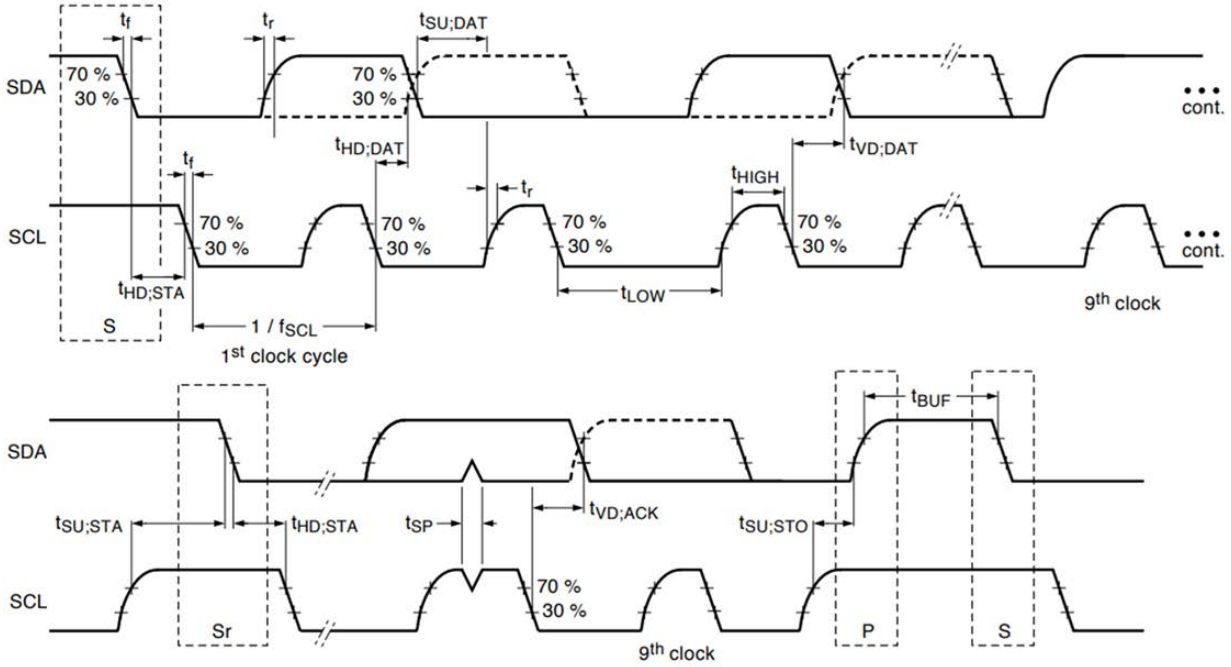



**Figure 25. I²C Timing Diagram**

**Table 9. I²C Timing Characteristics**

| Symbol | Parameter | Standard | | Fast Mode | | Fast Mode + | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| fSCL | SCL clock frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| tHD, STA | Hold time, repeated start condition | 4 | | 0.6 | | 0.26 | | µs |
| tLOW | Low period of SCL clock | 4.7 | | 1.3 | | 0.5 | | µs |
| tHIGH | High period of SCL clock | 4 | | 0.6 | | 0.26 | | µs |
| tSU, STA | Setup time, start condition | 4.7 | | 0.6 | | 0.26 | | µs |
| tHD, DAT | Data hold time: from SCL falling edge | 0 | | 0 | | 0 | | µs |
| tSU, DAT | Data setup time | 250 | | 100 | | 50 | | ns |
| tr | Rise time: SDA and SCL | | 1000 | 20 | 300 | | 120 | ns |
| tf | Fall time: SDA and SCL | | 300 | | 300 | | 120 | ns |
| tSP | Pulse width of spikes to be suppressed | | | 0 | 50 | 0 | 50 | ns |
| tSU, STO | Setup time, stop condition | 4 | | 0.6 | | 0.26 | | µs |
| tBUF | Bus-free time between stop and start | 4.7 | | 1.3 | | 0.5 | | µs |
| tVD, DAT | Data valid time | | 3.45 | | 0.9 | | 0.45 | µs |
| tVD, ACK | Data valid acknowledge time | | 3.45 | | 0.9 | | 0.45 | µs |

**Table 9. I²C Timing Characteristics (Continued)**

| Symbol | Parameter | Standard | | Fast Mode | | Fast Mode + | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| VnL | Noise margin at the low level | | 0.1*VDD | | 0.1*VDD | | 0.1*VDD | V |
| VnH | Noise margin at the high level | | 0.2*VDD | | 0.2*VDD | | 0.2*VDD | V |
| VIH | Threshold for valid input high | 0.7*VDDIO | | 0.7*VDDIO | | 0.7*VDDIO | | V |
| VIL | Threshold for valid input low | | 0.3*VDDIO | | 0.3*VDDIO | | 0.3*VDDIO | V |
| Cb | Bus capacitance | | 400 | | 400 | | 550 | pF |
| Ci | Pin capacitance | | 10 | | 10 | | 10 | pF |

## I²C Bit Format

The SKY76206-21 generally follows the *NXP® UM10204 I²C bus specification and user manual.* The device address is sent first, followed by a 16-bit register address, followed by 8-bit data packets. The device address is sent with a 7-bit device address with bit 0 = '0' for write and bit 0 = '1' for read, most significant bit first.

The 16-bit register address bytes are sent in big-endian format (upper byte first, lower byte second).

The 8-bit data bytes are written or read in little-endian format (lowest byte first, upper bytes next).

Multiple data byte transactions auto-increment the register address.

Figure 26 shows a typical read and write example of the I²C transaction.

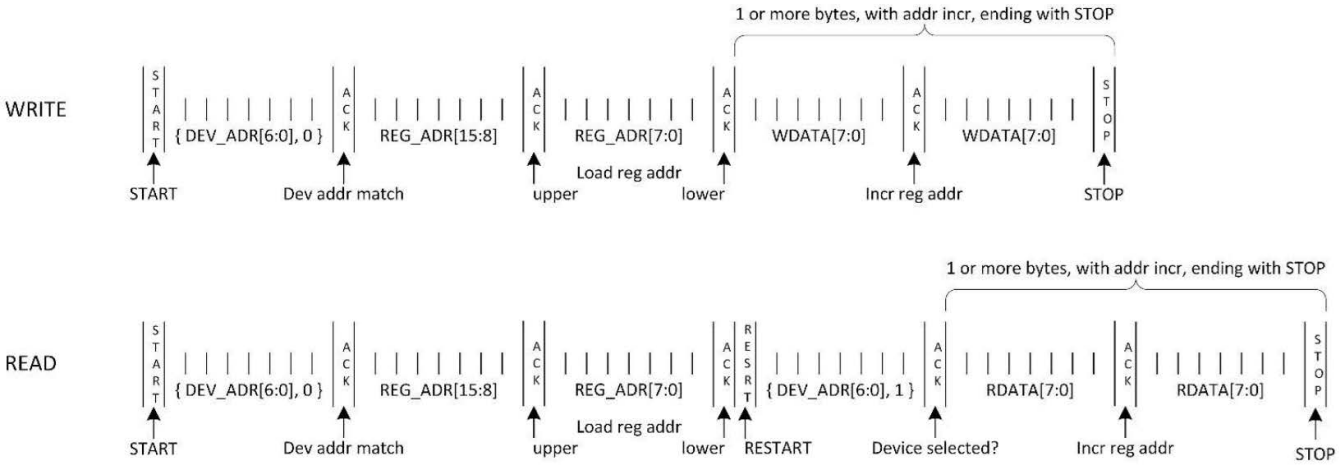



**Figure 26. I²C Read/Write Protocol**

# Operational Information

## Amplifier Modes

The amplifier has several modes of operation. Audio output modes include normal-gain mode, which has a gain of 0 dB and an output of 0 dBV = 1 $V_{RMS}$, and a high-gain mode, which has a gain of 6 dB and an output of +6 dBV = 2 $V_{RMS}$.

Low power modes include standby (no audio output), which occurs when the amplifier is commanded or in the event of a fault, and the reset mode (unprogrammed), which occurs when RESET_B is not pulled high to VDDIO.

## RESET_B Pin

The RESET_B pin is an active low input with an internal weak pulldown to GND, meaning that the amplifier stays in the reset mode (lowest power state) if RESET_B is not actively driven by an external host microcontroller or pulled-up to VDDIO.

RESET_B must be driven by an external source for normal operation.

**Table 10. RESET_B Pin Definition**

| Pin State | Pin Control Definition |
|---|---|
| RESET_B = 0 (GND or float) | Puts chip into the power down state. All circuits are off. |
| RESET_B = 1 (VDDIO) | Powers on chip (if all power supplies are valid). |

## IRQ_B Pin

The IRQ_B pin is an open drain active-low digital output pin interrupt request. It outputs a logic-low when a fault event occurs, provided the interrupt enable bits for that fault are enabled, to inform the external host microcontroller of a fault.

IRQ_B must be pulled-up to VDDIO with a 47 kΩ during normal operation.

**Table 11. IRQ_B Pin Definition**

| Pin State | Pin Control Definition |
|---|---|
| IRQ_B = 0 (GND) | Fault detected, interrupt sent to host processor. |
| IRQ_B = 1 (VDDIO) | No fault detected. |

## ADDR Pin

The ADDR pin sets the least-significant bit (LSB) of the 7-bit I$^2$C device address for the chip. It is internally pulled-up to VDDIO, so the pin can be left disconnected for applications where there is only one SKY76206-21 installed.

**Table 12. 7-Bit I$^2$C Device Address Selection Options**

| Pin State | I$^2$C Client Address |
|---|---|
| ADDR = 0 (GND) | 0x40 |
| ADDR = 1 (VDDIO or floating) | 0x41 |

## EN/WS Pin

The EN/WS pin is dual function enable (EN) and word sync (WS) control. The digital audio input format determines which function applies. The EASY_AMP_CFG register (0x0129) bit 1, nicknamed the EASY_EN_PIN_ENABLE bit, defines the function of the EN/WS pin. For SAI audio input formats, the pin operates in WS mode, functioning as the word sync or frame sync of the I$^2$S, and is driven by an external source. For PDM audio input formats, the pin operates in EN mode, enabling or disabling the audio similar to a mute function.

## PDM Interface

The PDM interface uses only the CLK and DATA pins for digital audio input. The PDM data format must be set with the EASY_AUDIO_INPUT (address = 0x0128) bits 6:0 before enabling the amplifier to avoid audible artifacts. The following tables and figures provide detail regarding the various PDM formats.

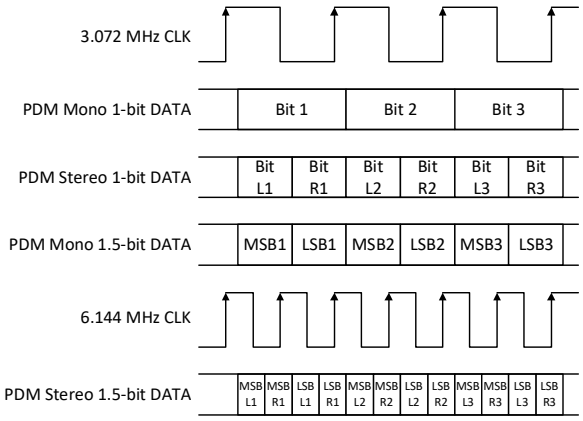



**Figure 27. PDM Data Formats**

**Table 13. PDM Clock Configuration**

| Channels | Bit Format | Typical CLK Frequency |
|---|---|---|
| 1 | 1-bit | 3.072 MHz |
| 2 | 1-bit | 3.072 MHz |
| 1 | 1.5-bit | 3.072 MHz |
| 2 | 1.5-bit | 6.144 MHz |

**Table 14. PDM Data Codes**

| Bit Format | Coded | Decoded |
|---|---|---|
| 1-bit | 1'b0 | -1 |
| 1-bit | 1'b1 | 1 |
| 1.5-bit | 2'b00 | -1 |
| 1.5-bit | 2'b01 | 0 |
| 1.5-bit | 2'b10 | Invalid |
| 1.5-bit | 2'b11 | 1 |

## PDM Low Pass Filters

The SKY76206-21 has four selectable PDM low-pass filter (LPF) coefficient sets to optimize the audio performance for either low latency or low noise. The PDM low pass filter attenuates out-of-band noise from the PDM data stream before going to the PWVM in the amplifier, reducing undesirable audio artifacts.

The PDM LPF is selected with the EASY_AUDIO_INPUT register (address = 0x0128) bits 5:4. Three of the PDM LPF options are read-only. See "Programming the SKY76206-21" for additional information.

**Table 15. PDM LPF Characteristics**

| PDM_LPF SEL | Filter Characteristics | Filter Type | OOB Peaking | Group Delay @ 10k |
|---|---|---|---|---|
| 0 | Custom third order for lowest latency | 20 kHz low latency | 9.4 dB @ 50 kHz | 2.6 µs |
| 1 | Third order Butterworth, 70 kHz to 3 dB corner | 40 kHz low latency | None | 4.6 µs |
| 2 | Third order Butterworth, 40 kHz to 3 dB corner | 20 kHz low noise | None | 8.3 µs |
| 3 | Third order elliptical, 45 kHz passband | 40 kHz low noise | –0.1 dB passband at 20 kHz | 5.6 µs |

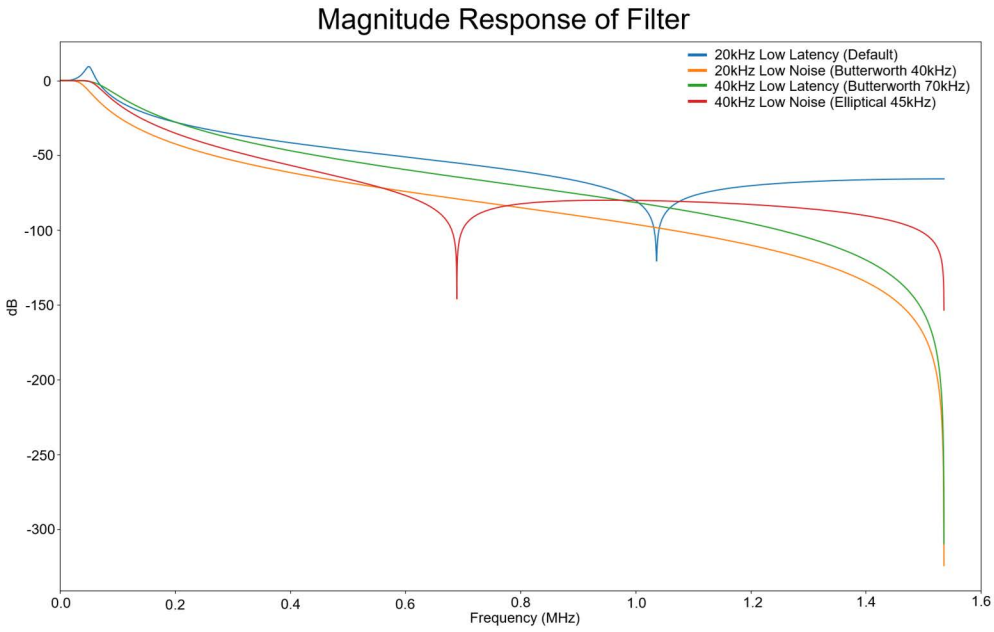



**Figure 28. PDM LPF Magnitude Response**

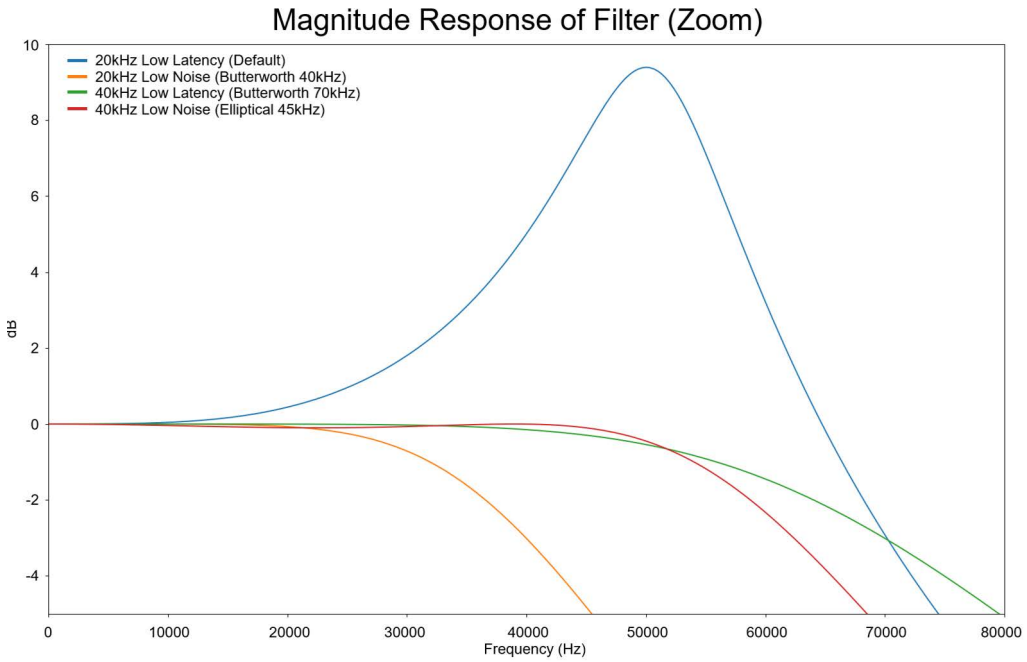



**Figure 29. PDM LPF Magnitude Response Zoom**

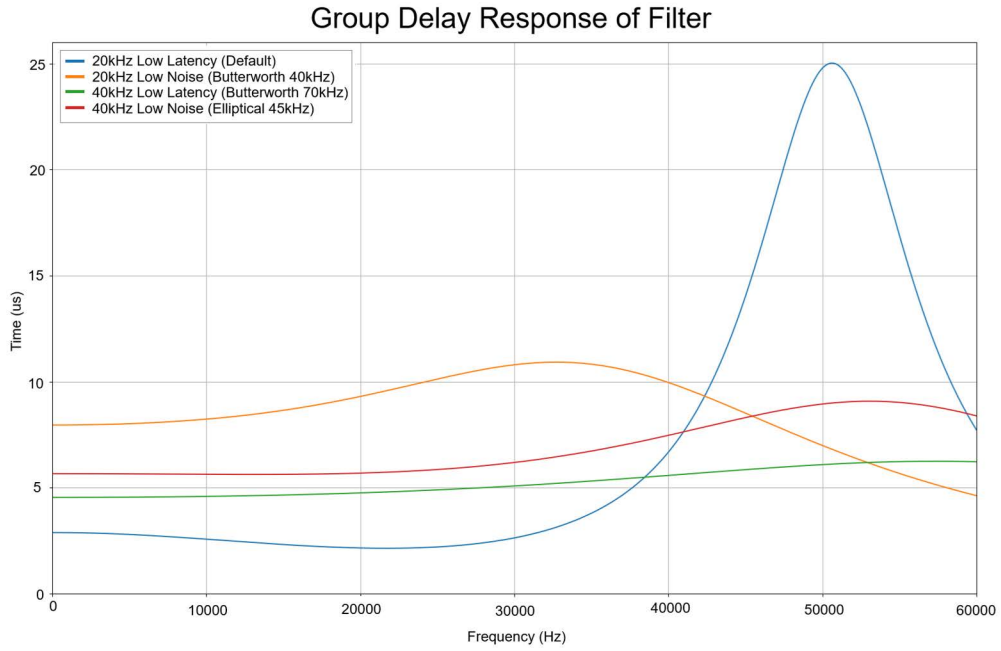



**Figure 30. PDM LPF Group Delay**

## Serial Audio Interface

The SAI accepts PCM data streams with the CLK, DATA, and EN/WS pins. The SAI interface can accept the standard two-channel $I^2S$ or left justified (LJ) mode. The sample rates supported are 44.1 kHz or 48 kHz and 96 kHz at 32 bits per channel. For standard two-channel applications, 64-bit clocks are required per frame. The SAI interface is set up with the EASY_AUDIO_INPUT register (address = 0x0128) bits 5:4.

**Table 16. Clock Rate Supported in Two-Channel $I^2S$ or LJ**

| Sample Rate | Bit Clock Frequency | Bits Per Channel |
|---|---|---|
| 44.1 kHz | 2.822 MHz | 32 |
| 48 kHz | 3.072 MHz | 32 |
| 96 kHz | 6.144 MHz | 32 |

**Table 17. SAI Data Format**

| SAI Data Format | Configuration Setting | Value | Description |
|---|---|---|---|
| $I^2S$ | WS invert | 0 | Normal: low = left sample, $I^2S$ format |
| | Data delay | 1 | BCLK cycle delay: $I^2S$ format |
| Left justified | WS invert | 1 | Inverted: low = right sample, left justified format |
| | Data delay | 0 | BCLK cycle delay: left justified format |

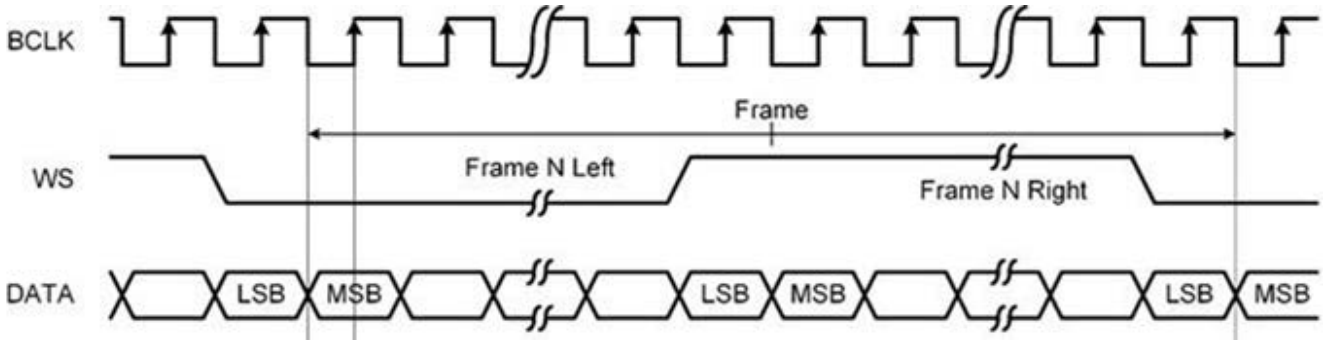



**Figure 31. SAI $I^2S$ Data Format**

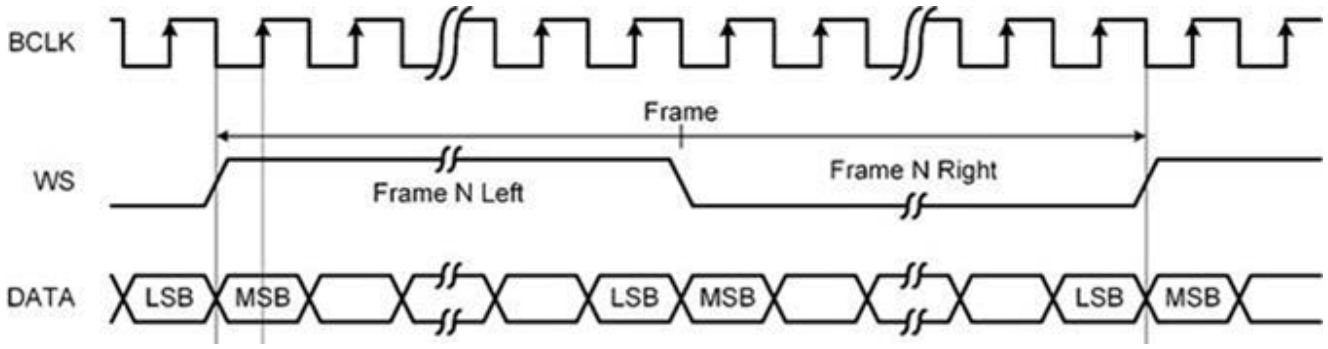



**Figure 32. SAI Left Justified Data Format**

## Error and Fault Reporting

The SKY76206-21 has a comprehensive error detection and reporting system. Faults are recorded in the AMPSTATE_FAULT_IRQ register (0x0302). The IRQ_B pin pulls low (GND) unless the fault is masked in the AMPSTATE_FAULT_IRQ_MASK register (address = 0x0306).

The chip stays in the fault state (no audio) until the fault is cleared, either by the external host microcontroller, or using an auto-recovery feature: FAULT_AR_ENABLE (address = 0x030A), that, when enabled, allows the chip itself to resume audio once the fault is cleared. An example is if there is a thermal fault, and the auto-recovery is enabled, the audio will resume once the chip cools without external intervention.

## Power Supply Sequencing and Audio Enable Timing

No special consideration is required for the power supply sequencing. Figure 33 provides the recommended sequence to power up and enable the audio.

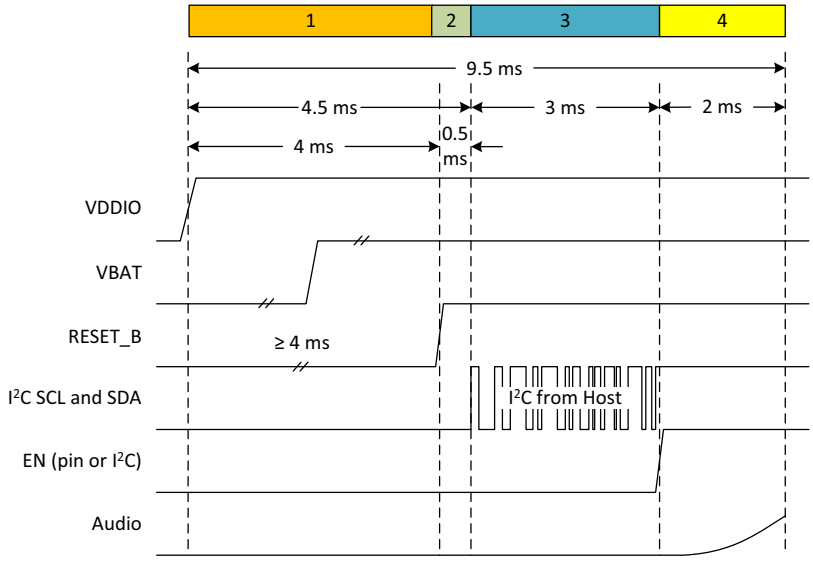



**Figure 33. System Timing**

# Programming the SKY76206-21

The SKY76206-21 is controlled and programmed via the $I^2C$ bus.

## Soft Reset

### CHIPRESET (address = 0x0404) bits [7:0]

The SKY76206-21 can be reset by writing 0xA5 to this register. After reset completes, the SKY76206-21 must be re-programmed as if at initial power-up to resume normal operation.

## Audio Control "Easy Mode"

The following commands provide an easy method to set up the SKY76206-21.

### EASY_MODE (Address = 0x012B) Bits [7:0]

Bit 0 enables the Easy Mode registers. Bits [7:1] are always '0'. Easy Mode is enabled by writing 0x01 to this register.

### EASY_AUDIO_INPUT (Address = 0x0128) Bits [7:0]

This register notifies the amp controller of specific information about the PDM or SAI digital input.

**Table 18. EASY_AUDIO_INPUT (Address = 0x0128) Bits [7:0] Setup for PDM**

| Bitfield Description | Bit | Bit = 0 | Bit = 1 |
|---|---|---|---|
| EASY_AIN_TYPE | 0 | PDM mode | |
| EASY_AIN_FORMAT | 1 | 1 bit | 1.5 bit |
| EASY_AIN_CH | 2 | Mono | Stereo |
| EASY_AIN_LR_SEL | 3 | Main channel | AUX channel |
| EASY_AIN_BW[1] | 4 | 20 kHz bandwidth LPF | 40 kHz bandwidth LPF |
| EASY_AIN_FILTER[1] | 5 | Low latency | Low noise |
| EASY_AIN_EQ | 6 | Always | |
| Unused | 7 | Always | |

1. The combination of EASY_AIN_BW and EASY_AIN_FILTER are used to create PDM_LPF_SEL[1] and PDM_LPF_SEL[0] which have a filter response as shown in "PDM Low Pass Filters".

**Table 19. EASY_AUDIO_INPUT (Address = 0x0128) Bits [7:0] Setup for SAI**

| Bitfield Description | Bit | Bit = 0 | Bit = 1 |
|---|---|---|---|
| EASY_AIN_TYPE | 0 | | SAI mode |
| EASY_AIN_FORMAT | 1 | $I^2S$ justified | Left justified |
| EASY_AIN_CH | 2 | | Stereo |
| EASY_AIN_LR_SEL | 3 | Left | Right |
| EASY_AIN_BW | 4 | 44.1 ksps to 48 ksps | 96 ksps |
| EASY_AIN_FILTER | 5 | Always | |
| EASY_AIN_EQ | 6 | Always | |
| Unused | 7 | Always | |

## EASY_AMP_CFG (Address = 0x0129) Bits [7:0]

This register controls the amplifier gain (bit 0), the handling of the EN/WS pin (bit 1), and sets the VDDIO voltage level (bits [3:2]). Bits [7:4] are always ‘0’.

- Bit 0 “EASY_GAIN” is set to '0' for 0 dB gain (normal-gain mode) and set to ‘1’ for +6 dB gain (high-gain mode).
- Bit 1 “EASY_EN_PIN_ENABLE” is only applicable in PDM mode. A setting of ‘0’ ignores the EN pin while a setting of ‘1’ follows the EN pin.
- Bit 3:2 “EASY_VDDIO_LEVEL” instructs the SKY76206-21 to expect VDDIO to be +1.2 V if set to ‘00’ or +1.8 V if set to ‘11’.

## EASY_AMP_ON (Address = 0x012A) Bits [7:0]

Bit 0 enables the amplifier block when set to ‘1’ and disables it when set to ‘0’. Bits [7:1] are always ‘0’. To turn the amplifier block on, this register must be 0x01. Additionally, the EN pin must be at VDDIO (PDM mode and EASY_EN_PIN_ENABLE=1 only), and a valid clock must be present on the CLK pin. There can be no active faults.

## Additional Registers

These registers are required to be programmed at boot-up of the SKY76206-21.

### RESERVED (Address = 0x0A00) Bits [7:0]

Program this register to 0x96.

### RESERVED (Address = 0x0A01) Bits [7:0]

Program this register to 0x96.

### RESERVED (Address = 0x00AE) Bits [7:0]

Program this register to 0x0B.

### RESERVED (Address = 0x00AF) Bits [7:0]

Program this register to 0x07.

## Internal Tone Generator

The SKY76206-21 has a built-in tone generator so it can output a sine wave without an external digital audio source.

### TONE_GEN_FREQ (Address = 0x05C0) Bits [23:0]

The tone generator frequency is determined by the equation TONE_GEN_FREQ*0.1831 Hz. The default setting 0x001555 sets the frequency to 1 kHz.

### TONE_GEN_AMPL (Address = 0x05C8) Bits [7:0]

The tone generator amplitude is broken into two parts: bits [3:0] are a scaling factor that when set to '0000' represents full scale (0 dBFS), otherwise each bit scales the amplitude by 1/16. Bits [7:4] right shift the scaling factor. The default setting is 0x00 which does not scale the amplitude.

### TONE_GEN_OFFSET (Address = 0x05C4) Bits [23:0]

The tone generator dc offset is determined by the signed integer register TONE_GEN_OFFSET and defaults to 0x000000. Each bit represents a 119.2 µV increment in dc offset ($1/2^{23}$).

### TONE_GEN_CTL (Address = 0x05C9) Bits [7:0]

The tone generator is enabled by setting bit 0 to '1' and disabled by setting to '0'.

The tone generator wave shape is changed by setting bits [2:1] to '00' for sine, '01' for triangle.

The tone generator disables other audio sources by setting bit 3 to '1' and mixes other audio sources by setting to '0'.

Bits [7:4] are not used and should be all zero.

## Fault and Status Registers

### AMPSTATE_STATE_STATUS (Address = 0x0328) Bits [7:0]

This read-only register replies with the live state of the amplifier. Bit 2:0 are the only bits that contain information. The other bits [7:3] are '0'.

**Table 20. AMP_STATE_STATUS (Address = 0x0328) Bits [7:0]**

| Response | Current State |
|---|---|
| 0x00 | <invalid> |
| 0x01 | OTP reading |
| 0x02 | <unused> |
| 0x03 | Standby |
| 0x04 | Amp turn-on |
| 0x05 | Amp turn-off |
| 0x06 | Audio playing |
| 0x07 | Fault |

### AMPSTATE_FAULT_IRQ (Address = 0x0302) Bits [31:0]

This register logs active faults or statuses by changing the associated fault bit from ‘0’ to ‘1’. Each fault can be cleared by writing ‘1’ to that bit (W1C = write '1' to clear), and all can be cleared by writing 0x000FFFFF to this register.

### AMPSTATE_FAULT_IRQ_MASK (Address = 0x0306) Bits [31:0]

The AMPSTATE_FAULT_IRQ_MASK (address = 0x0306) enables or disables the reporting of the fault or status with the IRQ_B pin.

## FAULT_AR_ENABLE (Address = 0x030A) Bits [15:0]

This register determines what happens after a fault or status change is detected. If set to '0', the chip stays in fault until the external host microcontroller reads and clears the fault. If set to '1', the amplifier automatically restarts once the fault is cleared.

**Table 21. Fault/Status, Fault/Status Mask, and Auto-Recovery Bits**

| Bit | Fault Bit Name | Mask Bit Name | Fault Auto-Recovery Bit Name | Fault Description | Source |
|---|---|---|---|---|---|
| 0 | SUPPLY_0P9V_FAULT_IRQ | SUPPLY_0P9V_FAULT_IRQM | SUPPLY_0P9V_FAULT_AR | VDD0P9 below min. allowed voltage | Supply monitor |
| 1 | SUPPLY_VBAT_FAULT_IRQ | SUPPLY_VBAT_FAULT_IRQM | SUPPLY_VBAT_FAULT_AR | VBAT below min. allowed voltage | Supply monitor |
| 2 | TEMP_FAULT_IRQ | TEMP_FAULT_IRQM | TEMP_FAULT_AR | On-chip temp. detector exceeds limit | Temp monitor |
| 3 | OTPRD_FAULT_IRQ | OTPRD_FAULT_IRQM | OTPRD_FAULT_AR | OTP errors at start-up | OTP |
| 4 | **Reserved** | | | | |
| 5 | PDMCLK_FAULT_IRQ | PDMCLK_FAULT_IRQM | PDMCLK_FAULT_AR | Invalid PDM clock period or pulses missing | Audio RX |
| 6 | PDMSTA_FAULT_IRQ | PDMSTA_FAULT_IRQM | PDMSTA_FAULT_AR | Invalid PDM data stuck at symbol for > 31 samples | Audio RX |
| 7 | PDMIVC_FAULT_IRQ | PDMIVC_FAULT_IRQM | PDMIVC_FAULT_AR | PDM invalid coding (1.5-bit) | Audio RX |
| 8 | **Reserved** | | | | |
| 9 | PLL_FAULT_IRQ | PLL_FAULT_IRQM | PLL_FAULT_AR | Phase-locked loop (PLL) is not locked | Clock |
| 10 | SAI_WS_FAULT_IRQ | SAI_WS_FAULT_IRQM | SAI_WS_FAULT_AR | SAI word strobe (EN/WS) not at correct rate | Audio RX |
| 11 | **Reserved** | | | | |
| 12 | **Reserved** | | | | |
| 13 | CLIP_IRQ | CLIP_IRQM | N/A | Digital audio clipping in the signal limiter | Digital audio path |
| 14 | PDM_LPF_OVERFLOW_IRQ | PDM_LPF_OVERFLOW_IRQM | N/A | PDM LPF bits are overflowing | Digital audio path |
| 15 | PDM_DSM_OVERFLOW_IRQ | PDM_DSM_OVERFLOW_IRQM | N/A | PDM audio DAC DSM overflow | Digital audio path |
| 16 | WD_OVERFLOW_IRQ | WD_OVERFLOW_IRQM | N/A | WATCHDOG overflow | Amp controller |
| 17 | **Reserved** | | | | |
| 18 | AMP_AUDIO_IRQ | AMP_AUDIO_IRQM | N/A | Amp is ready to play audio (not a fault) | Amp controller |
| 19 | LF_OVERLOAD_IRQ | LF_OVERLOAD_IRQM | N/A | Loop filter overload (output audio clipped) | Loop filter |

# Customization

## USER_GAIN (Address = 0x0022) Bits [15:0]

The user gain address allows adjustment of the digital gain applied after the digital EQ. The default gain of 0x01D9 is set so a –6 dBFS PDM input or 0 dBFS PCM input results in 0 dBV (1 $V_{RMS}$) amplifier output, in normal-gain mode.

Bits [15:9] are unused and are always '0'. Bits [8:5] represent an exponent while bits [4:0] represent a mantissa. The equation for the gain, in dB, is: *20*LOG((1+(Bits[4:0]/32))*(2^(Bits[8:5]-14))*0.5614)*

The default setting 0x01D9 = 111011001 binary, so the mantissa bits [4:0] are 11001 binary = 25 decimal, and the exponent bits [8:5] are 1110 binary = 14 decimal:
*20*LOG((1+25/32) * 2^(14-14) * 0.5614) = 20*LOG(1.781 * 1 * 0.5614) = 20*LOG(1) = 0 dB*

## TS_FAULT_CODE_TRIM Register (Address = 0x7F92) Bits [7:0]

The temperature monitor threshold to trigger a shutdown fault is written in the TS_CTL register (address = 0x0626) bits 7:0. To ensure that the part does not exceed the absolute maximum rating of +85 °C, this register should be confirmed and may need to be adjusted. It is required to read the TS_FAULT_CODE_TRIM register (address = 0x7F92) bits 6:0 for the calculation.

In the example below, TS_FAULT_CODE_TRIM = 0x1F = 31 decimal:

*TS_CTL [7:0] = 128 + TS_FAULT_CODE_TRIM + (TFAULT - 27) / 1.312*

*TS_CTL [7:0] = 128 + 31 + (85 - 27) / 1.312*

*TS_CTL [7:0] = 128 + 31 + 44 = 203 = 0xCB*

## Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY76206-21 is rated to Moisture Sensitivity Level 1 (MSL1) at 260°C and can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, “Solder Reflow Information,” document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: *JEDEC Standard J-STD-020*.

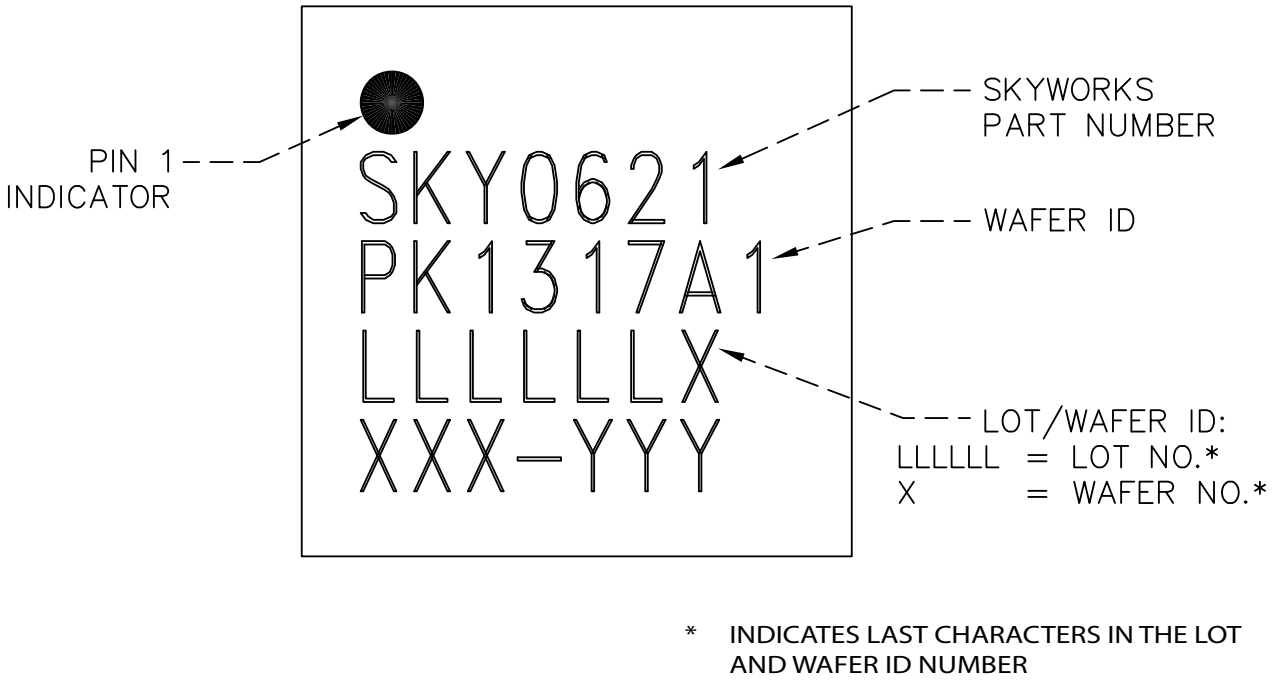
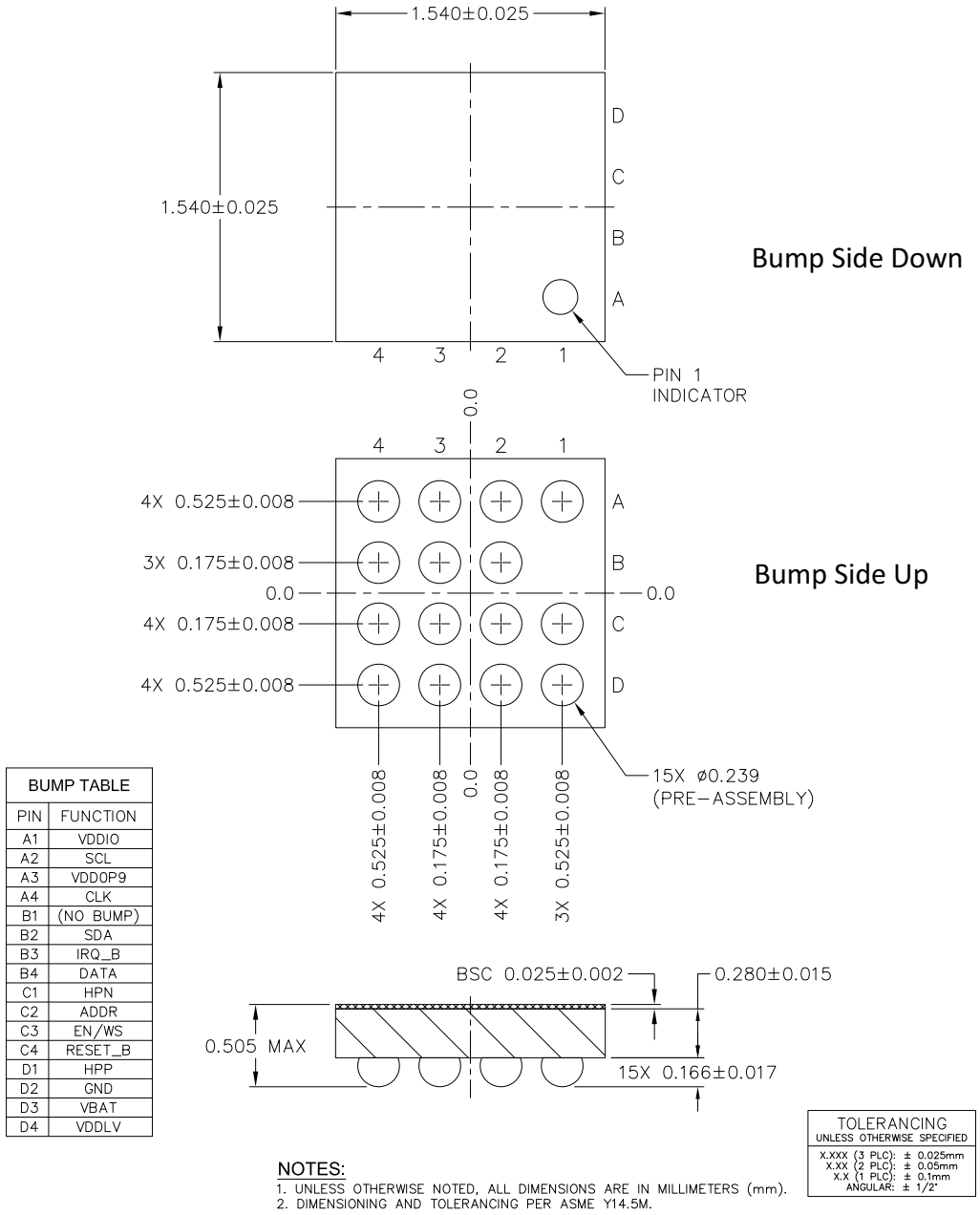



**Figure 34. Typical Part Marking**




| BUMP TABLE | |
|---|---|
| PIN | FUNCTION |
| A1 | VDDIO |
| A2 | SCL |
| A3 | VDDOP9 |
| A4 | CLK |
| B1 | (NO BUMP) |
| B2 | SDA |
| B3 | IRQ_B |
| B4 | DATA |
| C1 | HPN |
| C2 | ADDR |
| C3 | EN/WS |
| C4 | RESET_B |
| D1 | HPP |
| D2 | GND |
| D3 | VBAT |
| D4 | VDDLV |

**Figure 35. Package Dimensions**

## Ordering Information

| Part Number | Description | Evaluation Board Part Number |
|---|---|---|
| SKY76206-21 | Mono Low-Power Multi-Level Class-D Audio Amplifier IC | SKY76206-21EVK1 (Mono) |
| | | SKY76206-21EVK2 (Stereo) |

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