PRODUCT SUMMARY

SKY76280-22A: Speaker Magic™ Digital Audio Processing System-on-Chip (SoC)

Applications

- Powered speakers, soundbars
- Audio-video receivers
- Gaming audio systems and audio hubs
- Other audio processors

Features

- Implements Skyworks and third party trademarked audio algorithms including Dolby Atmos® and DTS-X®
- Three programmable Cadence HiFi 5 cores at 415 MHz
- Integrated shared 8 MB RAM
- Integrated, customer-programmable Arm® Cortex®-M3 MCU
- Enables AI-noise cancellation and AI dialog boost[1]
- Enables spatial calibration and individual speaker response calibration
- Integrates seamlessly with Skyworks low latency wireless link solutions
- Autonomous self-boot from flash for accelerated time to audio
- Nine I^2S input/nine I^2S output, 32-channel TDM input/32-channel TDM output
- Two SPI/I^2C ports
- Three SPI controllers (one with XIP for flash)
- JTAG/SWD, one I^2C controller, one UART
- 12 mm x 12 mm 88-pin QFN package
- Commercial temperature range from 0 °C to 70 °C
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Description

The SKY76280-22A is the fourth generation ultra-high-performance Digital Audio Processing SoC from the Skyworks Speaker Magic™ SoC family targeting soundbar and other immersive audio applications.

The SKY76280-22A is the centerpiece of a complete soundbar solution that supports leading audio formats including Dolby Atmos, DTS-X.

The audio processor SoC allows full customization of the audio post-processing pipeline with a graphical user interface.

The SoC enables seamless integration with other Skyworks wireless SoCs that support lossless audio with sub-µs latency variation for wireless sub-woofer and wireless surround speaker systems.

The SKY76280-22A supports nine I^2S TX and nine I^2S RX ports, as well as 32-channel inputs and outputs as TDM ports.

Selectable serial interfaces are included for added system flexibility. This includes primary and secondary host serial ports. Both ports support SPI or I^2C protocol.

The SoC supports three SPI controllers (SPI0, SPI1, and SPI2) with SPI2 dedicated for external SPI flash memory (quad mode supported).

One I^2C and one UART port are also available.

All on-chip processor and memory clocks are derived from a single PLL which locks to the incoming REFCLK signal at 36.864 MHz.

1. Subject to constraints for specific usage scenarios