Trends in AI Server Power Supply Architectures

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The rapid scaling of artificial intelligence (AI) servers and hyperscale data centers is driving new requirements for high efficiency, high density power supply unit (PSU) architectures. AI workloads demand precise power delivery, fast transient response, and robust isolation to support GPUs, accelerators, and heterogeneous compute platforms.

This document explores the AI server PSU application landscape and highlights how Skyworks Solutions is expanding its solutions to address critical power management challenges, including efficiency optimization, power density, reliability, and system scalability. By leveraging advanced analog, isolation, and power technologies, Skyworks is actively enabling the next generation AI infrastructure for data center and enterprise deployments.

Prospective increases in data center power requirements is shown below. The electrical power is obtained through the utility service at medium voltage alternating current (MVAC) levels (35 kV). It is then distributed through the data center for various purposes.

About 60% of the power is required for the processors, networking and accelerators, while 40% is needed for the cooling infrastructure. The power distribution structure includes battery back-up units (BBU), uninterrupted power supplies (UPS), and renewable energy sources as a sustainable and supplemental source of power.

Artificial intelligence (AI) is redefining data center design. Training and inference clusters built around GPUs and other accelerators are driving unprecedented rack power densities. McKinsey estimates that demand for AI-ready data center capacity will rise at an average rate of 33% a year between 2023 and 2030. This means that around 70% of total demand will be to host advanced-AI workloads by 2030. Generative AI, currently the fastest-growing advanced-AI use case, will account for around 40 percent of the total demand.

The platform under development is a 400 VDC to 50 VDC multiphase LLC resonant converter intended for high power AI server PSU applications. Silicon carbide (SiC) transistors are employed on the primary side to enable high frequency operation, improved efficiency, and power density, while traditional silicon MOSFETs are used for synchronous rectification on the secondary side.

The platform integrates multiple Skyworks analog voltage sensors, digital isolators, and the latest generation Skyworks isolated gate drivers from the Performance and Value series family, supporting robust control and signal isolation across primary and secondary domains.

This design is positioned as an evaluation platform rather than a turnkey reference design, providing flexibility to explore topology tradeoffs, component selection, and performance optimization for next generation AI server power architectures.

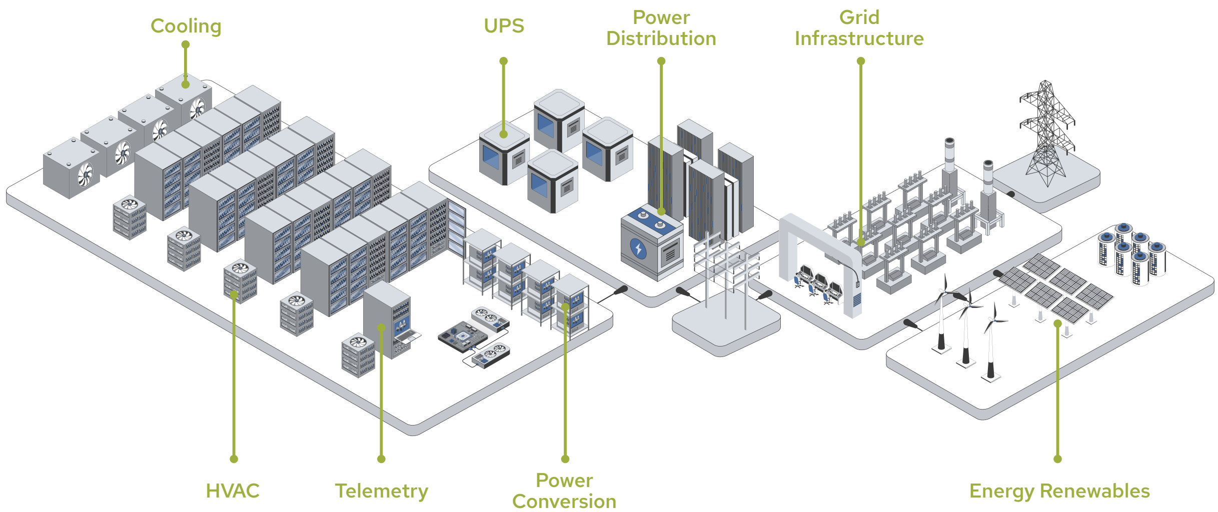
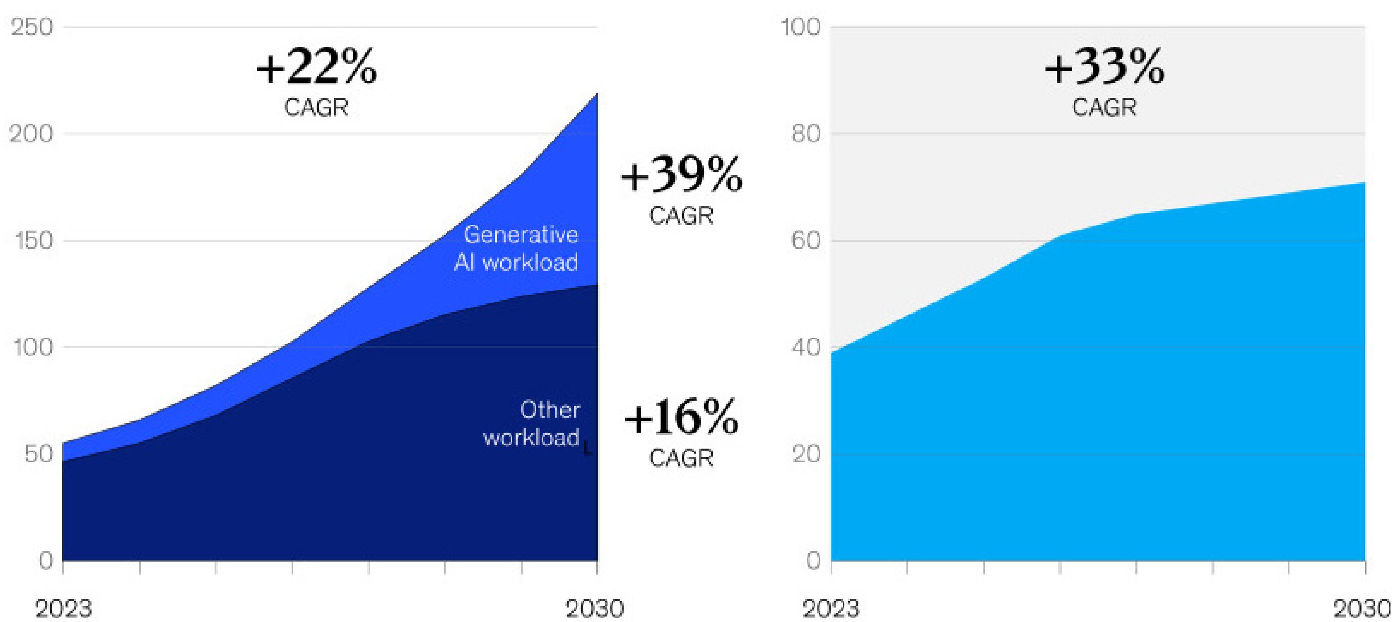


Figure 1: Data Center Power Layout

AI is the key driver of growth in demand for data center capacity.

Estimated global data center capacity demand,[1] gigawatts

Demand for advanced-AI capacity,[1] % of total data center capacity demand



[1]Midrange scenario is based on analysis of AI adoption trends; growth in shipments of different types of chips (application-specific integrated circuits, graphics processing units, etc) and associated power consumption; and the typical compute, storage, and network needs of AI workloads. Demand is measured by power consumption to reflect the number of servers a facility can house.

Figure 2: Data Center Power Requirements Trend
Source: AI data center growth: Meeting the demand | McKinsey

AI is driving a step function in data center power. AI servers are fundamentally different from traditional CPU based servers in that GPU and accelerator TDPs now exceed 1,000 W per device, AI server shelves commonly draw 8 to 15 kW each and AI racks operate at 140 to 200 kW, with roadmaps beyond 600 kW per rack.

This power density growth is not incremental—it requires a rethinking of the entire electrical distribution chain. The reason legacy architectures fall short is because traditional power delivery models were optimized for 5 to 15 kW racks with 12 VDC server architectures and multiple AC to DC conversion stages. At AI scale power levels, these approaches suffer from high current, excessive copper losses, bulky cabling, reduced efficiency, and higher total cost of ownership (TCO).

To address efficiency, scalability, and sustainability challenges, hyperscalers and leading colocation providers are aligning around power system innovations driven by the Open Compute Project (OCP). OCP was founded by hyperscale operators and is the primary industry forum for defining power architectures purpose-built for high density computing. These specifications are designed to scale efficiently with AI workloads while preserving interoperability across vendors.

The transition from traditional to HVDC architectures is outlined below by the OCP (Figure 3).

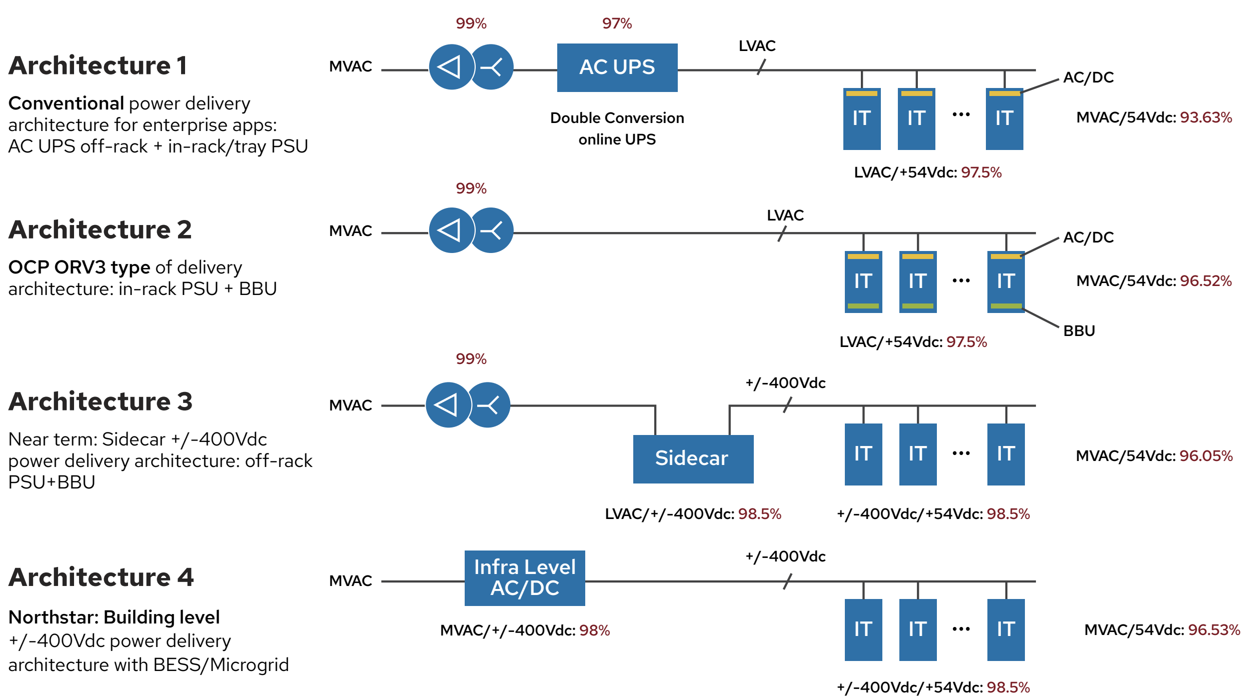


Figure 3: OCP Defined Evolution of the Power Distribution Structure for IT Racks

Architecture	Typical End to End Efficiency	Relative Loss Drivers
AC → 12 VDC (Legacy)	~88–90%	Multiple conversions, high I^2R losses
AC → HVDC → 54 VDC (Side-car)	~93–95%	Reduced current, fewer stages, retains 54 VDC to compute shelf
AC → HVDC (+/- 400/800 VDC)	~95–97%	Minimal distribution loss, optimized conversion

Table 1: Comparative Power Delivery Loss for Traditional Versus New Architecture

A three to seven percent efficiency improvement translates directly into lower energy costs at scale, reduced cooling load and improved power usage effectiveness (PUE). As an illustration on the significance of why the VDC voltage level matters, here's an estimation of how much current is needed for a 60 kW rack:

- At 12 VDC: ~5,000 A
- At 54 VDC: ~1,100 A
- At 400 VDC: ~150 A
- At 800 VDC: ~75 A

Lower current dramatically reduces conductor losses, connector stress, and copper usage, key enablers for AI scale racks. The value proposition boils down to the following:

- Lowers the total cost of ownership (TCO) due to higher efficiency reduces annual energy and cooling costs, smaller cables, and fewer PSUs reduce material and maintenance expense.
- Enables faster AI scaling by supporting 40 kW to 100+ kW racks without major redesign (with side-car option) and modular OCP designs accelerate deployment.
- Sustainability and compliance requirements are met due to reduced power loss result in lower carbon emissions per AI workload which aligns with hyperscaler and regulatory sustainability targets.
- Last but not least, it ensures multi vendor compatibility through OCP standards, thereby reducing vendor lock in.

AI is accelerating the shift from legacy 12 VDC power architectures to OCP aligned high voltage DC systems. Supported by ORv3 HPR V4, high voltage DC distribution, these architectures deliver superior efficiency, scalability, and reliability, critical foundations for AI driven data centers. For customers planning the next phase of AI infrastructure, adopting OCP power architectures is no longer optional, it is a strategic imperative.

Power Conversion Structure

Architecture Overview

AI server power delivery is currently characterized by two parallel architectural approaches: currently deployed PSU solutions optimized for today's production platforms (see Architecture 2 in Figure 3), and near term deployment architectures emerging to address rising power density, efficiency, and scalability requirements (see Architecture 3 in Figure 3).

Currently Deployed Architectures

The AC/DC stage converts single-phase AC input (up to 274 VAC) to a nominal 400 VDC output using a bridgeless totem pole power factor correction (PFC) boost converter. At power levels up to 3 kW, the system typically employs a single high frequency switching leg. For higher power ratings, the design scales through interleaved operation with parallel high frequency legs, supporting configurations of up to three legs and total power levels of up to 12 kW.

Although gallium nitride (GaN) devices are often considered attractive for this application, many industry recommendations favor silicon carbide (SiC) solutions. SiC offers a higher voltage operating range, greater robustness, improved field-proven reliability and a more favorable system-level cost structure at higher power levels. In server power supply units where the grid environment is generally less demanding, a hybrid topology is commonly reported in the literature. This approach typically uses GaN devices in the high-frequency switching leg to maximize efficiency and improve power density while silicon devices are retained in the low-frequency leg to balance cost and reliability.

The DC/DC stage converts the intermediate 400 VDC bus to a nominal 50 VDC output (used here for simplicity). In practice, the output voltage is often adjustable and load dependent. For example, a major hyperscaler player's ORv3 V1 specification allows the DC output voltage to vary between approximately 47.5 V and 51 V depending on load conditions and PMBus commands: 51 V at no load and approximately 50.5 V at full load.

Additionally, system-level communication typically enables a further programmed reduction of the output voltage by up to 3 V. Similar flexibility is specified in ORv3 HPR V1 (48 V, 5.5 kW), where the allowable output voltage range extends from 48 V to 51 V. To meet stringent efficiency targets and ensure favorable electromagnetic noise characteristics, the DC/DC stage is usually implemented using an LLC resonant converter with synchronous rectification.

Depending on the output power level, the primary-side topology varies. Low- and mid-power designs typically use a half bridge (HB) or full bridge (FB) configuration. At the high-power end (up to 12 kW), three phase bridge implementations are employed. In practice, a three phase bridge consists of three interleaved, parallel half bridge legs, with third harmonic current components present at a real or artificially generated primary-side star point.

On the secondary side, a full bridge synchronous rectifier is most commonly used. Some lower power power supply units employ a push-pull transformer with the corresponding push-pull rectifier. When a three phase primary is used, the secondary may be realized either as multiple parallel full bridge rectifiers or as a three phase bridge rectifier. The latter is composed of three interleaved, parallel half bridge legs, again exhibiting third harmonic content at an existing or virtual secondary-side star point.

Silicon and low voltage GaN devices are the most common semiconductor choices for this stage, balancing efficiency, switching performance, and cost. Due to the inherent complexity of the topology a flexible, digital control is required. A common approach in both academic research and fielded solutions is to employ separate digital controllers for the PFC and DC/DC stages, with coordination achieved through isolated serial communication between the two controllers.

Near-Term Deployment Architectures

In near-term deployment architectures, two power distribution approaches are defined between the power rack and the IT rack: a ±400 VDC system and an 800 VDC system. The ±400 V option can be implemented either as a two wire configuration, where the midpoint (MID) is not connected to the IT rack, or as a three wire configuration (illustrated in light grey in Figure 4).

The ±400 V approach introduces additional design considerations related to midpoint grounding. Specifically, the midpoint may be solidly grounded (SG, Z=0) or high resistance grounded (HRG, High Z), each presenting different trade offs in terms of fault detection, safety, system availability, and operational complexity. The advantages and disadvantages of these grounding schemes are further discussed in the Mt. Diablo specification, which provides guidance on selecting grounding strategies aligned with reliability and protection objectives.

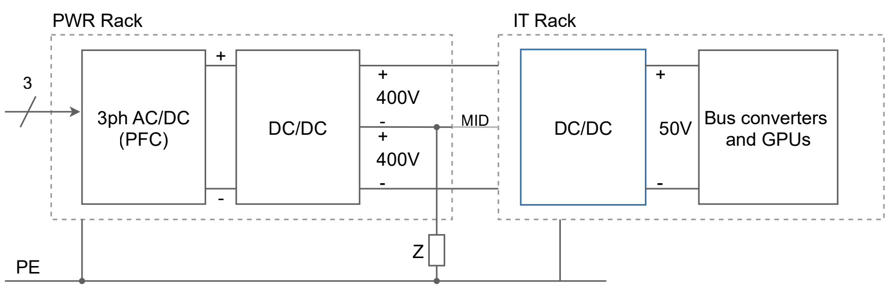


Figure 4. ORv3 HPR V4 Distribution Structure 400 V System

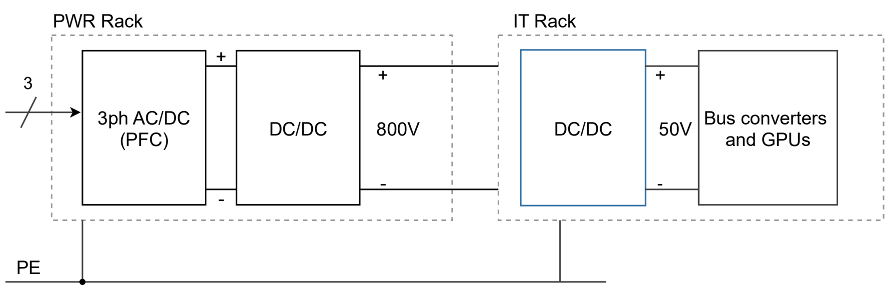


Figure 5. ORv3 HPR V4 Distribution Structure 800 V System

Power Sidecar Rack

Within the near term deployment architecture, the Power Sidecar Rack is realized around a front end AC/DC stage followed by an isolated DC/DC conversion stage. The AC/DC conversion from three phase AC to an 800 VDC bus with power factor correction can be implemented using several alternative concepts. A common approach beyond two level converters are the rectifier versions of established three level converter topologies.

The Vienna rectifier - corresponding to the rectifier form of the T-type three level inverter - has emerged as a particularly attractive solution and serves as a clear example where newly introduced bidirectional GaN transistors provide tangible benefits in efficiency and switching performance.

In addition, rectifier implementations of the flying capacitor three-level topology are also commonly proposed as viable front-end solutions.

Downstream of the rectifier, the DC/DC isolation stage performs an 800 V to 800 V conversion and is typically based on variations of the LLC resonant converter principle, with specific implementations influenced by whether 1200 V or 650 V semiconductor devices are available from a given technology. In contrast to the 800 V to 50 V converters located within the IT rack - where power density is often the dominant objective - the Power Sidecar Rack DC/DC stage places stronger emphasis on achieving very high efficiency.

IT Rack

In contrast to the Power Rack, the IT Rack converter must balance very high efficiency with increasing demands on power density, driven by space constraints and proximity to the load. In the near term system plans, the IT rack is supplied through an isolated 800 V to 50 V DC/DC power distribution board. Nevertheless, the literature also reports active efforts toward direct 800 V to 12 V and even 800 V to 6 V conversion, motivated by the desire to reduce or eliminate intermediate bus conversion (IBC) stages and thereby improve overall system efficiency and architectural simplicity.

Across these approaches, the dominant circuit family remains the LLC resonant converter, with architectural choices largely determined by the available semiconductor voltage class (1200 V versus 650 or 750 V class devices).

On the primary side of the isolated DC/DC stage, several converter structures are commonly considered. One widely used approach employs two-level full-bridge legs implemented with 1200 V SiC devices, forming a conventional full bridge (FB) LLC primary. Alternatively, three level primary structures are frequently explored when using 650 or 750 V class or slightly higher voltage SiC or GaN devices. These include flying capacitor three-level converters and DNPC (diode neutral point clamped) topologies, which reduce device voltage stress and switching losses while maintaining high efficiency. Many publications further investigate the three-level series half bridge (TLSHB) structure as an effective compromise between component count, controllability, and efficiency.

Additional variants include full bridge primaries supplied from two series-connected 400 V inputs, as well as analogous topologies implemented with three phase legs instead of a single full bridge, enabling improved current sharing and potentially lower ripple at very high power levels.

Our platform under development, is a realization of the DC/DC stage visible in Figure 4 and 5. This design is positioned as an evaluation platform rather than a turnkey reference design, providing with flexibility to explore topology tradeoffs, component selection, and performance optimization.

Target Converter Performance

According to section above—up to the ORv3 HPR V2 specification—the front-end power stage consists of a single phase PFC delivering a nominal DC output voltage of approximately 400 VDC. This intermediate bus is followed by an isolated DC/DC stage that converts the voltage to a nominal 50 VDC for IT load distribution. To achieve a high power factor and compliant input current waveform, the PFC control bandwidth is intentionally limited, which restricts its ability to regulate fast load transients. Consequently, the downstream isolated converter must provide good dynamic performance to ensure a stable and well regulated 50 VDC output. The ORv3 HPR V2 specification defines a maximum converter power level of up to 12 kW.

Near term system concepts described by the ORv3 HPR V4 specification introduce ±400 VDC distribution, which similarly necessitates the use of isolated step down conversion within the IT rack to generate the 50 VDC bus. For these converters, high power density and conversion efficiency are key requirements, driven by rack level power scaling and thermal constraints. The literature commonly addresses this challenge by employing two 400 VDC to 50 VDC converters, with their inputs connected in series and their outputs connected in parallel (ISOP). This arrangement allows operation from an 800 VDC bus while enabling effective sharing of the load current. The HPR V4 specification targets output power levels of 25 kW or higher per power supply unit (PSU). When applying this ISOP structure to an HPR V4 design, a similar 400 VDC to 50 VDC conversion block can be utilized as in earlier implementations, even though the required power levels and primary design objectives may differ.

In this work, the focus is on an ORv3 HPR V4 compliant IT rack power supply converting from an ±400 VDC (or 800 VDC) input to a 50 VDC output bus and implemented with two series input/ parallel output converters. However, experimental investigation is carried out using a reduced output power implementation to evaluate candidate converter topologies and design trade offs. Each conversion block is realized as an interleaved, three phase LLC resonant converter, enabling high efficiency, scalability, improved thermal distribution, and reduced component current stress. The overall structure is illustrated in Figure 6.

The target nominal output power is 3 kW, with a maximum overload capability of 60% (up to 4.8 kW). The target peak efficiency is 98%, resonant frequency is 100 kHz and the nominal output voltage is 50 VDC. The design must conform to the general form factor of a server power supply unit (PSU).

In a ±400 VDC architecture, an isolated DC/DC conversion stage is implemented in the power sidecar rack, which can provide a stabilized input voltage for the converter located in the IT rack. As a result, many designs reported in the literature explore LLC converters operating without output voltage feedback, leveraging a regulated input voltage. This allows improved efficiency and reduced converter size, both of which are critical requirements in IT rack applications. In contrast, the present study assumes a moderately varying input voltage range (±10%) rather than a fully regulated input. Consequently, output voltage regulation is maintained by means of feedback control using variable switching frequency.

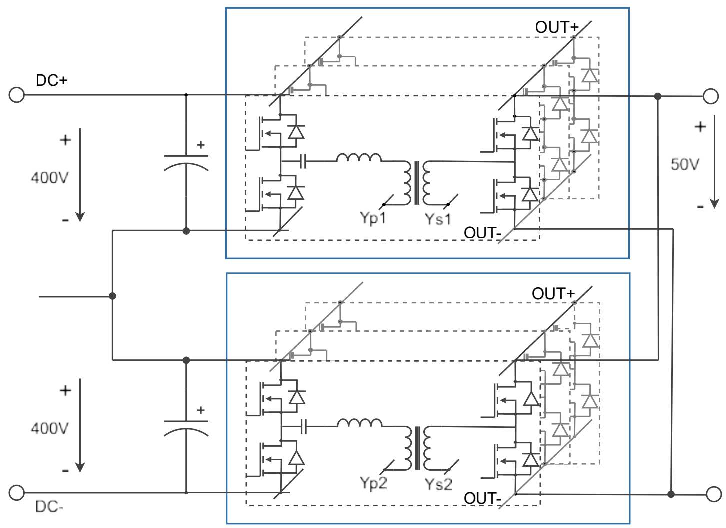


Figure 6. Input Series Output Parallel (ISOP) Conversion for 800 VDC Input Design

Selected Converter Approach

The selected converter structure is shown in Figure 7. The The primary circuit is composed of three half-bridge legs effectively forming a three phase circuit. Each phase has separate, independent transformer and resonant circuits connected in a star configuration. The primary circuit uses 650 V, SiC transistors in a TO-Leadless (TOLL) package with a typical channel resistance of 22 mΩ at room temperature. The SiC transistors are one possible solution providing a field proven, robust, and scalable solution.

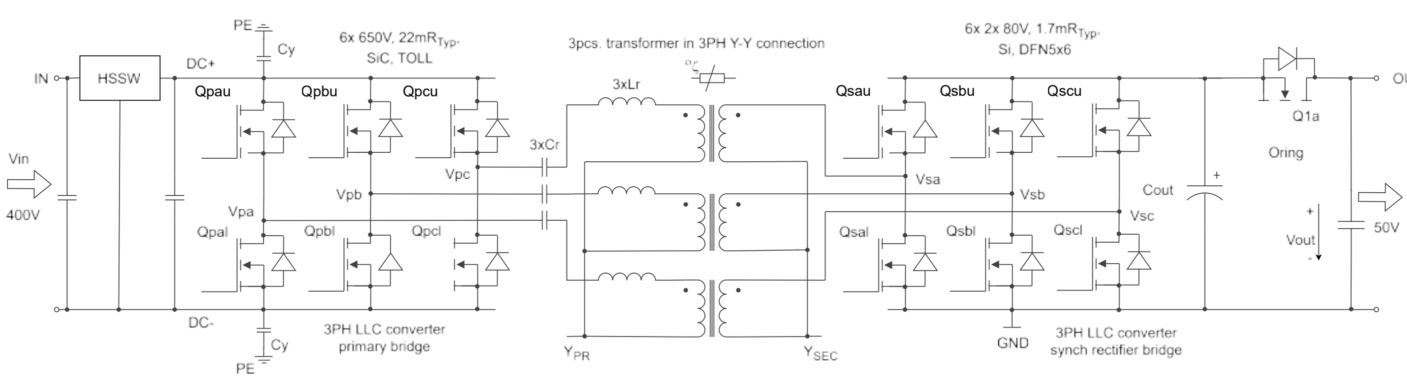


Figure 7. 3ph, Y-Y Connection LLC Converter Simplified Drawing

The secondary circuits are also connected in star connection and the synchronous rectifiers form a three-phase rectifier, implemented with Si MOSFETs. In each output phase branch, two 80V, 1.7 $m\Omega_{Typ.}$ MOSFETs in DFN5x6 BSC (bottom side cooled) package are used in parallel.

The circuit concept advantages and disadvantages are summarized below:

Advantages:

- Reduced input and output capacitor current ripple due to interleaved operation.
- Higher effective ripple frequency when designing input and output filters, enabling smaller passive components.
- Reduced subharmonic content of the transformer primary voltage, as interleaving suppresses n*3rd harmonics (where n is a positive integer).
- Various transformer connection options (Y, Δ combinations) allow more optimal transformer ratios for different nominal input and output voltage levels.
- Reduced component stress per phase, which eases device selection and improves reliability margins.
- Semiconductor losses are distributed among parallel power branches, simplifying thermal management and heat dissipation.
- Easy scalability to higher power levels by increasing the number of phases or per phase power.

Disadvantages:

- Increased control complexity; however, this is typically manageable, as modern digital controllers provide fully configurable three phase control capabilities.
- Active phase current balancing may require additional hardware and/or software resources.
- Earlier degradation of efficiency at light load, since phase shedding is more difficult to implement in resonant converters.
- Diminishing benefits at lower power levels (below approximately 10 kW), where the circuit becomes increasingly over engineered relative to performance needs.

For the assumed target power level of 3 kW, a single phase LLC converter would represent a competitive and more power optimized solution, offering comparable efficiency and significantly reduced complexity. Nevertheless, the three phase LLC architecture is deliberately selected in this work, as the design is considered a scaled down prototype of a higher power (12 kW) converter. The reduced power implementation serves primarily as an experimental platform to investigate the architectural behavior, control concepts, and scalability of the three phase LLC topology, rather than to achieve an optimal solution for the given power rating.

The LLC converter primary employs transistors in a TOLL package mounted on an FR4 PCB. Heat is transferred from the transistor tab into the PCB through an array of filled and capped vias located beneath the tab. These vias are filled with a thermally conductive epoxy material. Although this construction increases PCB cost, it enables efficient heat transfer through the PCB while providing a repeatable and easily manufacturable solution compared to microvia based thermal designs.

Heat conducted through the PCB is subsequently transferred from the bottom PCB surface to an external heatsink via an electrically isolating thermal interface material (TIM). In this construction, an approximate 3 K/W thermal resistance across the PCB can be achieved. For higher power levels, advanced top side cooled power packages can be used on the primary side. Such packages enable direct heatsink attachment via a low thermal resistance TIM and improved thermal performance.

On the secondary side, the transistors utilize a bottom cooled DFN 5×6 package. Heat is similarly transferred through PCB layers using thermal vias. Due to the lower power dissipation per device, the secondary-side heat is typically dissipated through the PCB without an additional heatsink.

For higher output current applications, a double side cooled (DSC) package variant with otherwise identical footprint can be employed, enabling heatsink attachment on the top side of the package for enhanced thermal management.

Beyond the core power conversion stages, the PSU is complemented by an input hot swap switch (HSSW) and an output ORing diode function. The output ORing is implemented using the same MOSFET devices employed for the secondary synchronous rectification. In total, eight DFN 5 × 6 packaged MOSFETs are utilized for this switch.

The HSSW circuit add three functions:

- Hot plug functionality: Provide controlled connection to a live supply rail.
- Inrush current limitation: Input surge current limitation during turn on.
- Short circuit and overload protection: Disconnects load from the supply in case of short circuit or overload.

Beyond the main protective functions, the circuit also serves as a system interface subcircuit and provides functionality like input undervoltage and overvoltage protection, input power good reporting, controlled short circuit/fault turn-off (soft turn-off), delayed fault response to overcome nuisance trips, DC link measurement in general, input current/power monitoring, pass switch safe operating area (SOA) and thermal protection, contribution to current sharing management in redundant power architectures and prevention of back-feeding with parallel power supplies.

The HSSW functions such as inrush current limiting, controlled turn off under short circuit or overload conditions, and short duration overvoltage limiting are realized by operating the series pass device in its linear mode.

In high voltage and high current applications, this mode of operation cannot be safely or efficiently implemented using conventional IGBT or silicon MOSFET devices, as their SOA is severely limited; even SiC MOSFETs require significant SOA derating when operated linearly. Consequently, recent publications report the use of SiC JFET devices for such applications.

SiC JFETs offer high robustness, excellent thermal stability, and a wide linear mode SOA, and typically exhibit an open circuit failure mode, which is advantageous for protection functions. The main trade off is a more complex gate drive requirement. To address this, normally on SiC JFETs are commonly combined with a low voltage MOSFET in a cascode configuration, resulting in an effective normally off device suitable for practical hot swap implementations.

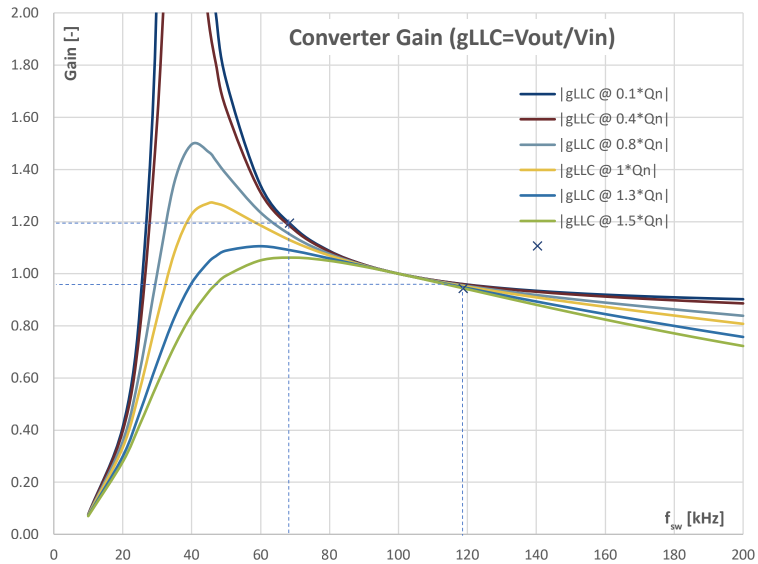
Simulated Circuit Waveforms

The three phase Y–Y connected LLC converter is driven by a 50% duty cycle square wave excitation at a switching frequency f_{SW}. The resonant frequency of the tank, f_r, is 100 kHz. The input voltage varies only within a narrow operating range. Output voltage regulation is achieved by varying the switching frequency. Operation both below and above the resonant frequency are considered in the design. The steady state control characteristic of the converter is estimated using the first harmonic approximation (FHA) method, which is widely adopted in the literature for resonant converter analysis. In this approach, only the fundamental component of the square wave excitation is considered, while higher order harmonics are neglected.

The resulting gain characteristic is shown in Figure 8. In this representation, the input voltage (Vin) corresponds to the AC phase to star point voltage first harmonic of one primary phase (Vpa-Vypr), while the output voltage (Vout) denotes the regulated DC output voltage. The voltage gain is derived from a single phase equivalent circuit comprising the resonant elements reactance (X_{Lr}, X_{Cr}), the reactance of transformer magnetizing inductance (X_{Lm}), and the equivalent AC load resistance (R_{ac}). The gain curves are parametrized by the load condition, expressed in terms of the quality factor (Q). The transformer ratio is selected according to the nominal input/output voltages and slightly higher than eight because of the assumed nominal DC link voltage of 410 V.

The three interleaved phases yield circuit waveforms altering from the ideal half or full bridge LLC converter, especially when switching frequency alters from the resonant frequency. Relevant circuit waveforms are examined by time domain simulation and summarized in Figure 9 to Figure 11. Current stresses calculated by simulation are close to stresses obtained by FHA analysis. Figure 9 shows idealized waveforms when operating at the resonance frequency with notations used in Figure 7. The upper section shows idealized secondary current waveforms as well as output capacitor ripple current.

One main advantage of interleaved operation is the significantly reduced input/output capacitor ripple current. The lower section shows secondary reflected current waveforms of one phase of the circuit together with primary bridge output potential. (Output potential with respect to the existing or artificial midpoint of the DC link.) Due to interaction of phases, the primary star-point (YPR) has a square wave component with three times the switching frequency and 1/3 of amplitude. This effect yields transformer voltage and associated magnetizing current with less harmonic content as one can seeon the current waveshape. Table 2 summarizes relevant effective currents in this operating mode assuming nominal input power. Figure 10 and Figure 11 show output power waveforms above and below resonance.



where,

$$g_{LLC}(Q, f, mr) = \frac{V_{out}}{V_{in}} = \left|\frac{jX_{Lm} \parallel R_{ac}}{jX_{Lm} \parallel R_{ac} + (jX_{Lr} + jX_{Cr})}\right|$$

$$\omega = 2 \cdot \pi \cdot f_{SW},\ X_{Lr} = \omega \cdot L_r,\ X_{Cr} = (\omega \cdot C_r)^{-1},\ X_{Lm} = \omega \cdot L_m,$$

$f = \frac{f_{SW}}{f_r}$, relative switching frequency

$mr = 1 + \frac{L_m}{L_r} = 8$, ration of magnetizing (L_m) and resonant (L_r) inductance

$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}}$, resonance frequency

$R_{ac} = \frac{6}{\pi^2} \cdot n^2 \cdot \frac{V_{out}^2}{P_{out}}$, reflected load resistance

$Q = \frac{Z_r}{R_{ac}}$, quality factor

$Z_r = \sqrt{\frac{L_r}{C_r}}$, characteristic impedance

$n = \frac{N_p}{N_s} = 8.2$, transfer ration, primary/secondary

Figure 8. Converter Gain by FHA Method

Vout = 50 V, iout = 60 A (Pout=3kW)			Vin_{Min}	Vin_{Nom}	Vin_{Max}
			Nominal Load		
Vin	[V]	Input DC link	350	413	430
fsw	[kHz]	Actual switching frequency	69.7	100.0	112.1
iQsau	$[A_{Rms}]$	Rectifier PhA upper synch transistor	31.4	31.4	31.4
isa	$[A_{Rms}]$	Transformer PhA secondary current	44.4	44.4	44.4
ipa	$[A_{Rms}]$	Transformer PhA primary current	6.2	5.8	5.7
IQpau	$[A_{Rms}]$	Primary PhA upper transistor RMS current	4.9	4.4	4.3
imagA	$[A_{Rms}]$	Transformer PhA magnetizing current	3.0	2.1	1.9
Iin	$[A_{Rms}]$	Input current effective	8.4	7.9	7.7
ICin	$[A_{Rms}]$	Input capacitor AC ripple	4.1	2.9	7.7
$vCrA_{Max}$	[V]	Resonant capacitor peak voltage	158.0	103.3	90.9
$vCrA_{Rms}$	[V]	CrA effective voltage	111.7	73.0	64.3
ΨLmA_{Max}	μWb_{Peak}	LmA peak magnetic flux	596.0	415.4	370.6
ΨLmA_{Rms}	μWb_{Rms}	LmA rms magnetic flux	421.4	293.7	262.0
ΨLrA_{Max}	μWb_{Peak}	LrA peak magnetic flux	175.3	164.3	162.1
ΨLrA_{Rms}	μWb_{Rms}	LrA rms magnetic flux	124.0	116.2	114.6

Table 2. Summary of Current Stresses with Nominal Load

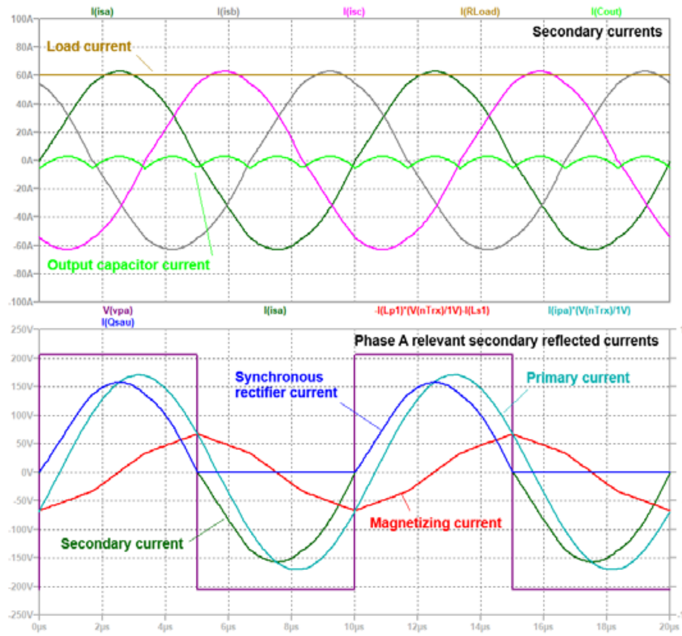


Figure 9. Relevant Circuit Waveforms at fsw=fr

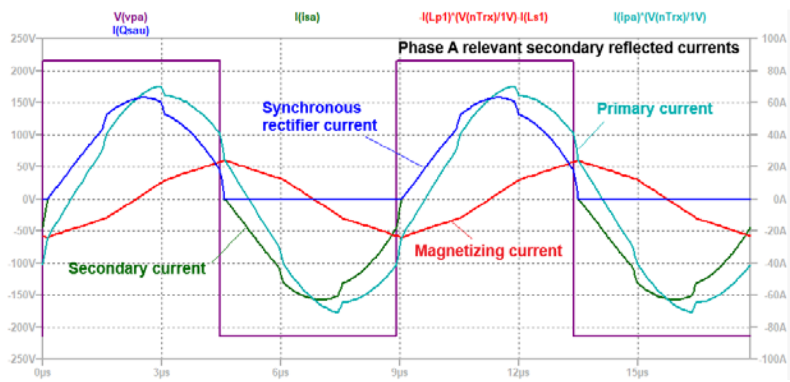


Figure 10. Circuit Waveforms with Nominal Power Above Resonance (fsw>fr)

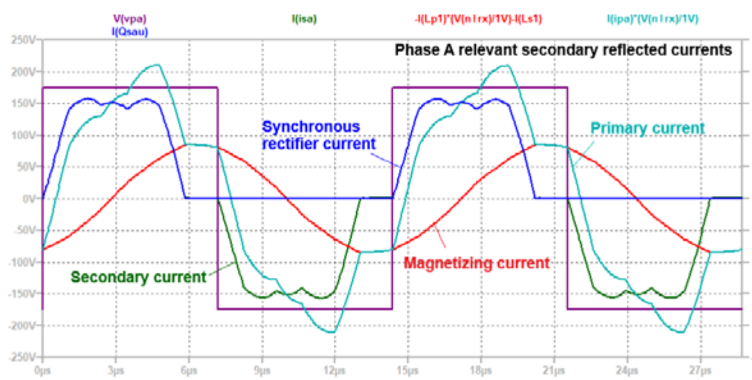


Figure 11. Circuit Waveforms with Nominal Power Below Resonance (fsw<fr)

System Structure

The converter discussed is redrawn in Figure 12. The secondary consists of two parallel windings, while the switches are implemented using separate MOSFETs with individually driven gate circuits. This allows comparing various secondary configurations with minimal changes. The output ORing switch is not detailed, these are parallel connected MOSFETs with a single driver.

The converter needs a precise and flexible control insensitive to ambient influence. Therefore, a digital controller is applied. Interfacing the power circuit and the digital controller requires several sensors and actuators between them. The processor ground (GND) is selected on the safe potential domain, to make any user interface easier. Signals originating from the hazardous, high voltage area must be isolated with double (or reinforced) insulation strength. Excluding the hot swap functionality, the power converter requires isolation between the primary side and the controller for the following signals: transistor gate drive signals, DC link voltage measurement, high voltage side hot spot temperature measurement, and phase current measurements.

The phase currents are measured with a current transformer in this application. Skyworks BOM contribution are summarized in Table 3. Furthermore, Skyworks Value and Performance series gate driver family is utilized in different parts of the system, as it offers devices with varying functionality, package options, isolation ratings, and gate drive strength.

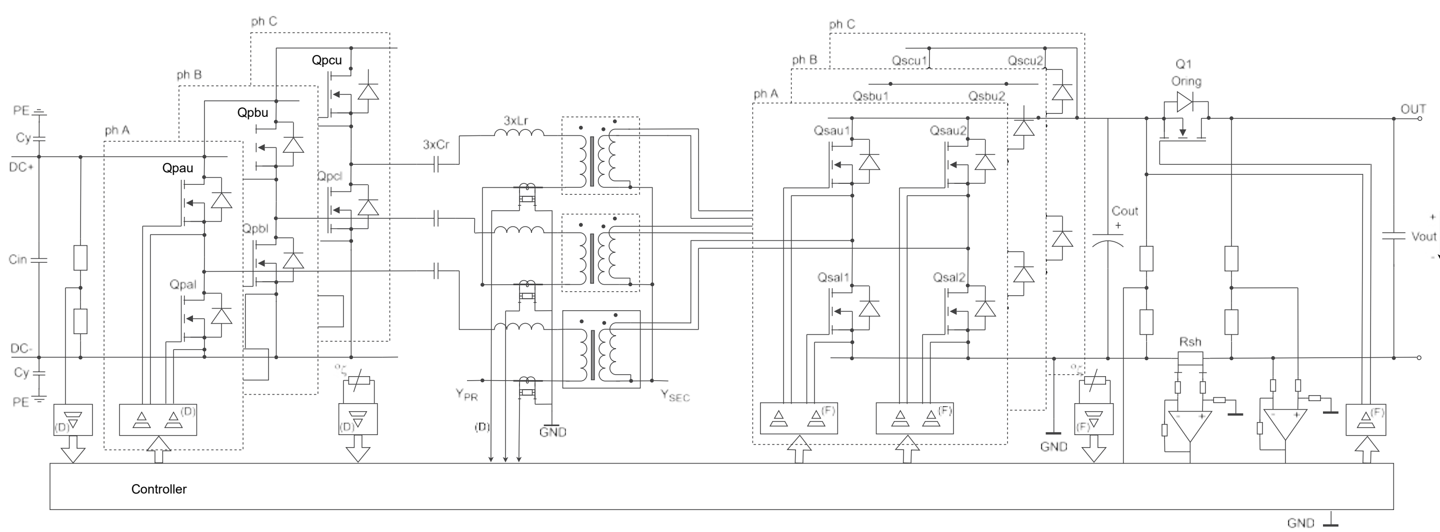


Figure 12. System Structure

The digital controller may be referenced to the secondary negative rail, as shown in Figure 8. In this configuration, the simplest and most common approach is to use non-insulated low-side and level-shifted high-side drivers to control the synchronous rectifier transistors.

However, in this application, the output rails carry relatively large currents, have significant physical dimension, and operate at high switching speeds. Therefore, it is advantageous to insulate the low-side gate signals, resulting in an insulated half-bridge driver for each secondary branch. The output OR-ing switch requires only a single low-voltage functional insulation. The output voltage is measured before the output switch using a simple divider, and after the output switch using a differential amplifier, without the need for galvanic insulation. Similarly, the DC output current is measured using a shunt and an associated differential amplifier.

Circuit Function	Part Number	Insul. Class	Package	VISO	Comments
DC link isolated voltage measurement	Si8932D-IS4	D	WB-SOIC-8	5.0 kV_{RMS}	Single-ended in/out isolated amplifier
Primary-side isolated gate driver	Si82E39AEE-IS3	D	WB SOIC-14	6.0 kV_{RMS}	UVLO = 15 V, deglitch = NA, IO: VIA, VIB, universal configuration, enable input
Alternative primary-side isolated gate driver	Si82F39AEE-IS3	D	WB SOIC-14	6.0 kV_{RMS}	UVLO = 15 V, SelVCD™, IO: VIA, VIB, universal configuration, enable input
Secondary-side isolated gate driver	Si82D39ACB-IM3	F	LGA-13	2.5 kV_{RMS}	UVLO = 12 V, deglitch = NA, IO: VIA, VIB, universal configuration, enable input
Output ORing switch isolated gate driver	Si82D39ACB-IM3	F	LGA-13	2.5 kV_{RMS}	UVLO = 12 V, deglitch = NA, IO: VIA, VIB, universal configuration, enable input
Isolated digital signaling	Si86S663BE-IS2	D	WB SOIC-16	6.0 kV_{RMS}	3F/3R channel, deglitch = NA, output low
Primary-side isolated transistor driver in ACF converter	Si82D39ACB-IM3	F	LGA-13	2.5 kV_{RMS}	UVLO = 12 V, deglitch = NA, IO: VIA, VIB, universal configuration, enable input
Synchronous rectifier isolated driver in auxiliary converter	Si82A30ACE-IS4	D	SSO-8	6.0 kV_{RMS}	UVLO = 12 V, deglitch = NA, IO: In: VIA, Out: VO+,VO-, enable input
Isolated I2C communication	Si86S605AB-IU	F	QSOP-16	2.5 kV_{RMS}	1F/1R bi-directional I2C

Table 3. Skyworks BOM Contribution

DC link voltage is measured with an Si8932 series, isolated amplifier. This is a single channel, single ended input, single ended output amplifier. Typical parameters are: 0.16 mV offset, 0.06% gain error, 0.75 μV/°C offset drift, -5 ppm/°C gain error drift, and 75 kV/μs CMTI between others. Due to the fail-safe output feature of the amplifier, the component serves as a power good test for the 5 V auxiliary supply referenced on the DC link.

A wide body stretched SOIC- 8 package version is used, maintaining external clearance and creepage of 8 mm, adequate for PSU requirements (<300 VAC system voltage, OVIII, PD2, altitude: 3050 m, fsw = 120 kHz, Vw = 350 Vp).

The primary transistors are driven by the Si82Ex, a 6A HB/dual driver with low propagation delay, small channel-to-channel and part-to-part skew. The driver also ensures a minimum of 200 kV/μs CMTI. The family ensures versatile UVLO options between 4 V to 15 V. Here, an SiC transistor with gate voltage level of +15 V/-5 V, the 15 V UVLO option is selected. The wide SMD package is used, providing 8 mm creepage and clearance. We note that each transistor position is supplied with an insulated gate drive supply (GDS) not detailed here. An alternative solution for primary transistor gate drive is the Si82Fx series selectable variable current drive (SelVCD™) gate driver. This option is detailed in the next section.

The secondary transistors are driven by the Si82Dx, a 1 A fully insulated HB/dual driver. The gate signal isolation improves noise behavior even if gate drive supply is provided from a common source for lower transistors and with a bootstrap for the high side transistors, as in the above system. While the insulation voltage is very small and the insulation class is only functional here, we can use a family member with lower voltage ratings and significantly smaller package (LGA14). This allows more optimal layout with reduced gate circuit parasitics.

The output ORing switch requires only a single insulated drive signal. However, it also requires an insulated gate drive supply not available in this design. While the Si82D39ACB dual driver has independent channels, one channel is used to implement a low power, non-controlled power supply running from an external clock. Alternatively, when proper supply power is available, one can use the Si82Ax single channel member of the family.

The primary hot-spot temperature is sensed with an NTC resistor. Even though the resistor is insulated from the primary circuit, it is in close vicinity of power semiconductors and the insulation to the HV circuitry does not fulfill basic or double insulation requirements. A common, low cost solution is to convert the NTC resistor voltage with an astable multivibrator to a PWM signal with a frequency of few tens of kHz and a duty cycle proportional to the resistor signal. The PWM signal is then transferred to the controller side through a digital isolator. The PWM information is read by the capture function of the processor timers. Skyworks offers digital isolators with various configurations, functionalities, speeds, and other parameters.

In this design, power supplies on both sides of the isolator are readily available, but several other signals not detailed in this paper between primary and secondary had to be isolated. Therefore the digital isolator Si86S663BE-IS2 was chosen, which integrates 3-3 forward and reverse channels.

The converter requires auxiliary power for different subcircuits, including the control processor and associated digital/analog circuitry, gate drive circuits and cooling fan. The detailed discussion of the overall power supply structure is beyond the scope of this paper. However, the general governing targets of high efficiency, high power density server PSUs are valid even for low power auxiliary supplies.

The traditional auxiliary power supply is the multi-output flyback converter. To improve efficiency and enable higher switching frequencies, an active clamp flyback (ACF) converter can be used. A high side clamp is applied, allowing the use of cost-effective and efficient N-channel MOSFETs for the auxiliary transistor (Qa) which requires a high side driver. This task can be accomplished with a level shift high-side driver or alternatively the insulated driver Si82Dx. This solution offers a clean primary circuit layout and reduces gate circuit noises.

In an alternative auxiliary supply, suitable for higher output currents, a flyback output utilizes a synchronous rectifier. In this case, assume the primary circuit has a regular dissipative snubber as shown in Figure 14. The synchronous rectifier can be controlled by the auxiliary output of an active clamp controller. This yields a "no diode emulation" mode of operation of Qa and a resulting negative magnetizing current prior to primary transistor turn-on, thereby achieving a ZVS turn-on feature.

Unlike the ACF converter shown in Figure 13, the leakage energy is not recovered in this configuration. An isolated gate driver, such as the Si82Ax, can be used to drive the synchronous transistor. Its low propagation delay yields a short body diode conduction interval and results in better efficiency at high switching frequencies. The gate driver has a small (7 ns) part-to-part propagation delay skew, therefore when the same driver is used on the primary side an even more precise timing is provided.

The advantages of primary side active clamp (ZVS switching and leakage energy recovery) and secondary synchronous rectification (reduced rectifier conduction loss) can be combined in a single converter if this is economically justified. This is shown in Figure 11.

Server power ecosystems (including ORv3) uses PMBus protocol for power supply control and telemetry (V, I, T measurements). An isolated communication between PSU controller and system controller breaks ground loops and ensures noise and error free communication. In this system a low power I2C isolator is utilized, Skyworks SI86S605AB-IU.

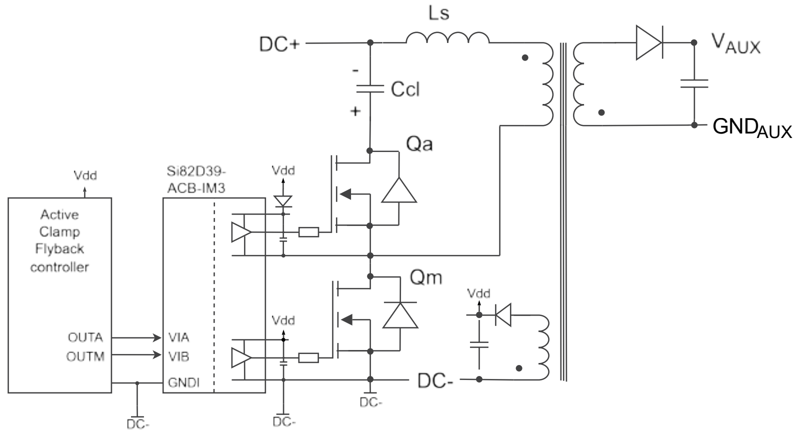


Figure 13. ACF Converter Primary Transistor Drive with Si82Dx

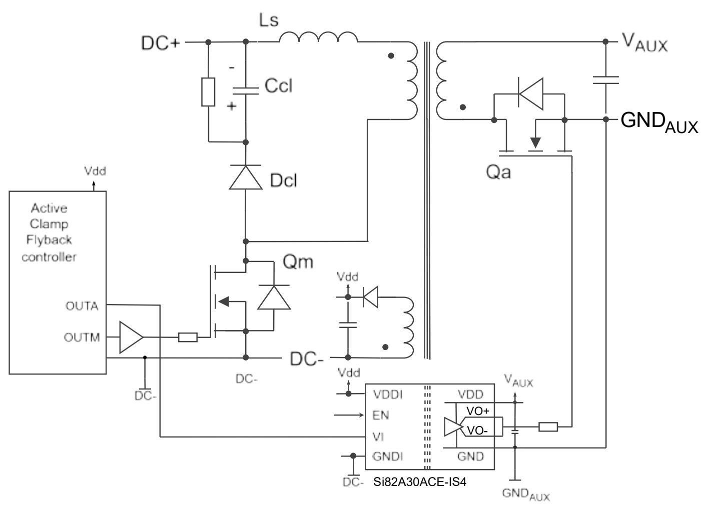


Figure 14. Synchronous Rectifier Transistor Drive with Si82Ax

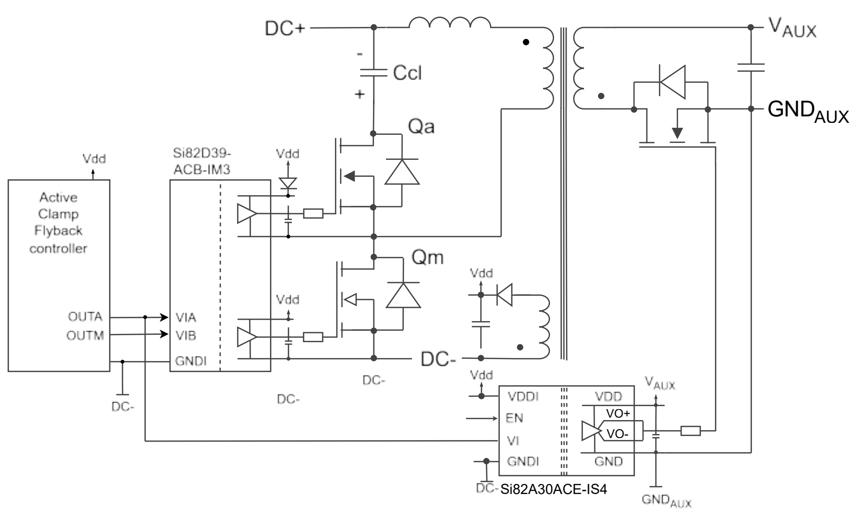


Figure 15. Primary ACF Converter with Synchronous Rectification

Advanced Gate Drive Alternatives from Skyworks

Traditional voltage mode drivers (TVMDs) have been widely used for years but suffer from several limitations. Their output drive strength cannot be adjusted dynamically without using multiple output pins, increasing board area, component count, and cost due to additional resistors and steering diodes. As a result, designers must pick gate resistor values for worst case conditions, sacrificing efficiency during the majority of normal operation.

At high slew rates, particularly with HEMT devices, the Miller effect can cause parasitic turn on and catastrophic failures. Conventional mitigation methods include slowing turn on switching speeds, utilizing a negative gate drive voltage, or a mixture of both. Both of these reduce efficiency by increasing switching losses or body diode conduction during deadtime.

Skyworks SelVCD™ (Selectable Variable Current Drive) technology addresses these challenges with a novel current mode output structure. SelVCD eliminates external gate resistors, allowing maximum pull down strength during transients and significantly improving immunity to parasitic turn on.

The source and sink currents can be adjusted in real time from the isolated side, enabling adaptive gate drive behavior based on bus voltage, load current, or ambient temperature. See AN 1390 for more details.

SelVCD drivers integrate a Miller clamp using the gate output pin, made possible by the absence of gate resistors. In dual drivers such as the Si82Fx, this enables a built in Miller clamp in a compact NB SOIC 16 or WB SOIC 14 package that would otherwise require larger packages in TVMD implementations. Compared to TVMDs in similar packages, this integrated Miller clamp can allow designers to eliminate the negative gate drive rail, further improving efficiency and simplifying system design.

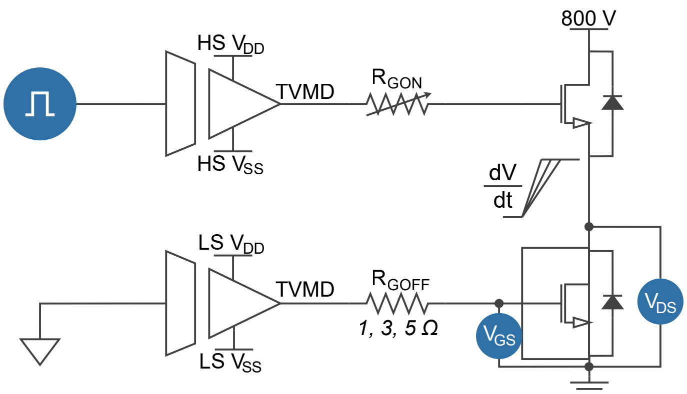


Figure 16: 6 A Traditional Voltage Mode Driver

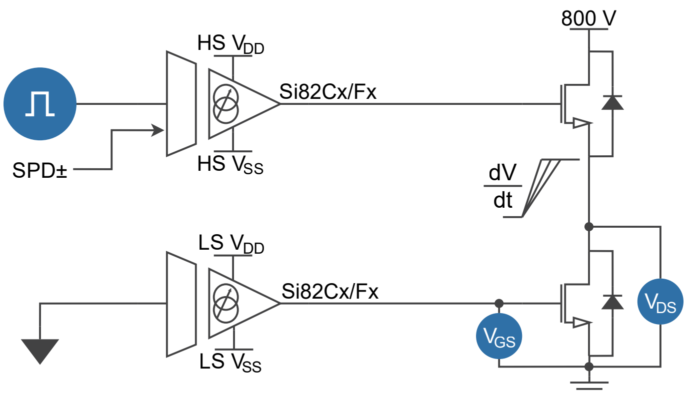


Figure 17: 4 A SelVCD™ Driver

To show the benefit of the SelVCD-enabled Miller clamp, a half bridge test setup utilizing two 1200 V 16 mΩ SiCFETs. The high side gate driver is pulsed to apply a dv/dt to the low side FET drain. The low side FET is attempted to be kept off utilizing the gate driver. The FET data sheet requests a turn-on voltage of +15 V and a turn-off voltage between -3 to - 4 V. However, to show the benefit of SelVCD, a 0 V turn-off voltage is used. A 6 A TVMD with an internal pull down R_{DSON} of 0.7 Ω is utilized. In the TVMD case, the turn-on speed is varied by changing the R_{GON} and in the SelVCD gate driver case, the SPD+ setting is varied from SPD+ 0 to SPD+ 7.

For the low side gate driver, the R_{GOFF} is varied between typical gate resistors of 1, 3, and 5 Ω while the SelVCD gate driver is directly tied to the gate of the SiCFET.

As shown in Figure 18, the TVMD has the possibility of parasitic turn-on at higher slew rates, while SelVCD allows the gate to remain under the $V_{GS(th),min}$ condition even at the most extreme slew rates.

With just the addition of two resistors on the input side, existing designs can be cross compatible with existing dual driver pinouts while being able to utilize the SelVCD technology.

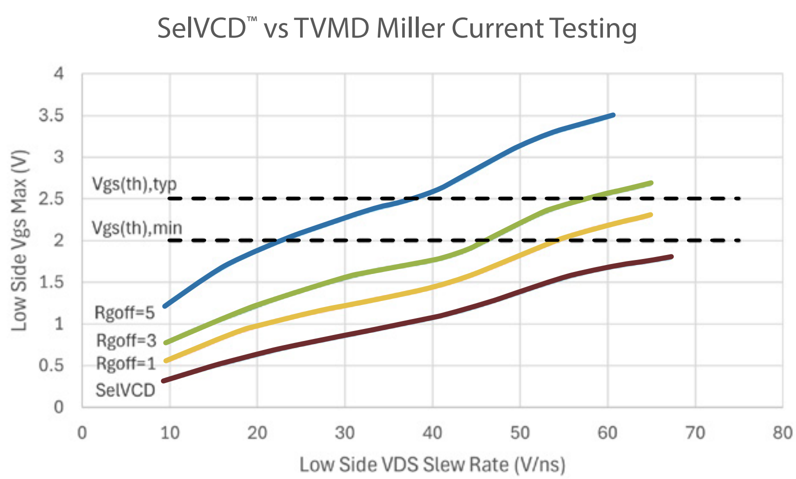


Figure 18: SelVCD™ vs TVMD Miller Current Testing

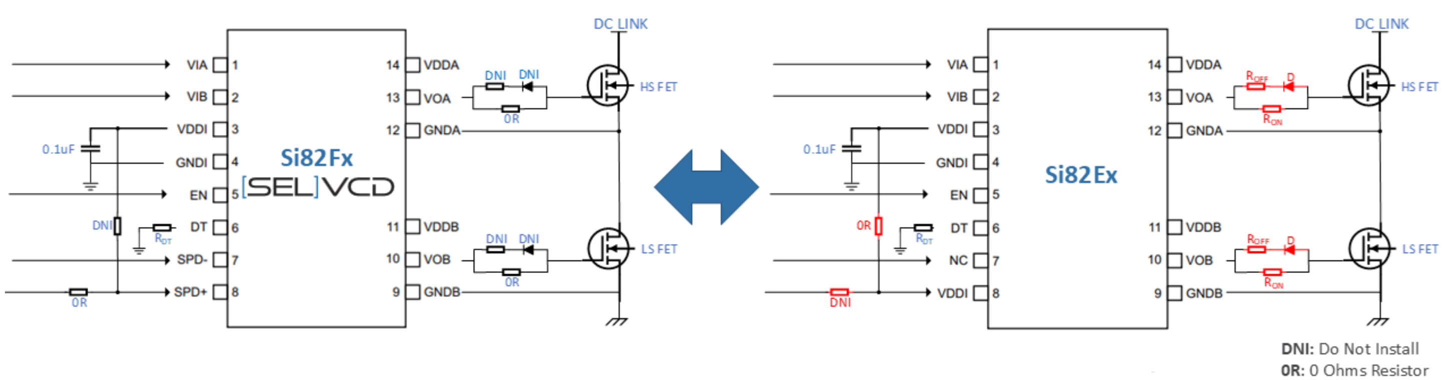


Figure 19: Si82Fx vs. Si82Ex BOM Choices

Conclusion

The rapidly increasing power demand of hyperscale data centers and AI servers is driving the adoption of alternative, high voltage power distribution architectures. These systems require power conversion stages with significantly higher power capability, efficiency, and power density. Among the available topologies, the LLC resonant converter represents a widely adopted solution for isolated DC/DC conversion. To meet rising power levels, multiphase implementations—particularly three-phase LLC structures—provide an effective and scalable approach.

In this work, a three phase LLC converter design with reduced power is investigated as a potential building block for such high power systems. Although the implementation operates at a lower power level, it enables the evaluation of key architectural, control, and scalability aspects relevant to higher power designs. The converter requires distributed isolated measurement and gate drive functions, each with specific performance and integration requirements.

To address these requirements, gate drivers from the Skyworks Si82Ax-Fx gate driver family provide suitable solutions across different parts of the system, enabling optimized selection with respect to isolation capability, package options, gate drive strength, functional features, and UVLO characteristics. The overall system implementation is further supported by the use of analog and digital isolators in various configurations, resulting in a robust, flexible, and scalable architecture.

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