

APPLICATION NOTE

AN1423: Si5350/Si5351 Frequently Asked Questions

This document answers some of the most frequently asked questions for the Si5350 and Si5351 CMOS clock generator products. If you do not find the answers you are looking for, please contact [Skyworks Support and Resources](#).

Product Family

Si5350 (Pin-Controlled)

- Si5350A: XTAL only
- Si5350B: XTAL and VCXO capability
- Si5350C: XTAL and CLKIN

Si5351 (I²C Programmable)

- Si5351A: XTAL only
- Si5351B: XTAL and VCXO capability
- Si5351C: XTAL and CLKIN

Table 1. Frequently Asked Question Links

Cross-Reference Link
1. Where can I find Si5350- and Si5351-related collateral?
2. Where is the RoHS and REACH compliance information for Si5350 and Si5351?
3. How can I obtain a Si5350 or Si5351 with a custom startup frequency?
4. What is the default I2C address of the Si5351 when the part does not have an A0 pin?
5. How can I burn the NVM on a blank Si5351 part?
6. What if I want a feature in my custom Si5350 or Si5351 that is not configurable in ClockBuilder Pro?
7. Can a CMOS clock be driven into the XA or XB pins of the Si5350 or Si5351?
8. What is the output-to-output skew of the MultiSynth™ outputs?
9. How long does a glitch-less frequency transition take?
10. Can the Si5350 or Si5351 duplicate a PWM input?
11. Does changing the drive strength through the control registers change the output slew rate?
12. Why is there a separate programming guide (AN1234) for the 16-QFN Si5351?
13. Why does CLK3 on a 16-QFN Si5350 or Si5351 show a phase shift from the other outputs?
14. What is the minimum PLL lock range of the Si5350 or Si5351?
15. Is there a ppm/°C output error or ppm output error over time spec for the Si5350 or Si5351 devices?
16. What are the Si5350 or Si5351 power-up sequencing requirements for VDD/VDDO? What if I can't meet it?
17. How do you interface Si5350 or Si5351 clock outputs to HCSL, LVDS, and LVPECL receivers?

1. Where can I find Si5350- and Si5351-related collateral?

Table 2. Product Links

Link Type	Link
Product pages	https://www.skyworksinc.com/Products/Timing/CMOS-Clock-Generators
Evaluation board (EVB)	https://www.skyworksinc.com/Products/Timing/Evaluation-Kits/clock/si535x-b20qfn-evb-evaluation-kit
ClockBuilder® Pro software	https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software
IBIS models	Available on the specific product pages
Schematic footprint and symbols	Available on the specific product pages
Request technical support	Skyworks Support and Resources

Table 3. Relevant Application Notes

Link Type	Link
Application notes	AN619: Manually Generating an Si5351 Register Map for 10-MSOP and 20-QFN Devices
	AN1234: Manually Generating an Si5351 Register Map for 16QFN Devices
	AN554: Si5350/51 PCB Layout Guide
	AN551: Crystal Selection Guide for Si5350/51 Devices

2. Where is the RoHS and REACH compliance information for Si5350 and Si5351?

Please refer to the part number search on the website for the Certificate of Conformance.

https://www.skyworksinc.com/product_certificate.aspx

3. How can I obtain a Si5350 or Si5351 with a custom startup frequency?

Use ClockBuilder Pro to create a custom part number. After creating a custom plan, you have the option to submit the configuration to Skyworks. This officially creates the part number in our system. After this step, contact your local distributor to order this new part number.

ClockBuilder Pro software can be found here: <https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software>

4. What is the default I²C address of the Si5351 when the part does not have an A0 pin?

The default address of the Si5338 is always 0x60h unless a different custom I²C address was selected when creating a custom part number.

The A0 bit described in Figure 6 in the data sheet is only an option for the Si5351A. All other Si5351 devices either have 0x60h as their default address, or an I²C address defined by a custom configuration from ClockBuilder Pro.

When creating a custom part number for the Si5351, you have the option to define a new I²C address.

5. How can I burn the NVM on a blank Si5351 part?

Skyworks does not currently support customer NVM burning for this product family. However, you can easily create a new custom part with a newly defined default startup state using ClockBuilder Pro. Once the part is submitted at the end of the process, contact your local distributor to order the new part number.

6. What if I want a feature in my custom Si5350 or Si5351 that is not configurable in ClockBuilder Pro?

If ClockBuilder Pro is currently missing a configuration option supported by the Si5350 or Si5351 that you would like included in your custom part, create a new support ticket and we can add the new settings.

An example of a configuration option currently missing in ClockBuilder Pro is the ability to buffer external references such as a crystal or CLKIN directly to an output.

Remember to include the existing ClockBuilder Pro Project and a description of the functionality you would like added. We can then send a new updated ClockBuilder Pro Project file back to you. Submit the new modified configuration and the new part number will include your required functionality.

7. Can a CMOS clock be driven into the XA or XB pins of the Si5350 or Si5351?

Yes. Drive the ac-coupled clock into XA and leave XB unconnected. However, limit the signal level into XA to $< 1 V_{pp}$.

8. What is the output-to-output skew of the MultiSynth™ outputs?

All outputs are within ± 500 ps of one another at power up (if pre-programmed), or if PLLA and PLLB are reset simultaneously via register 177. If only PLLA or PLLB is reset, then only the outputs associated with the PLL in question are assured to be within ± 500 ps of each other.

If an output frequency is dynamically changed, output-to-output skew of that clock is not assured until a soft reset is performed.

If using a Si5351 in a 16-QFN package, please see [13. Why does CLK3 on a 16-QFN Si5350 or Si5351 show a phase shift from the other outputs?](#)

9. How long does a glitch-less frequency transition take?

The Int, R, and N register values inside the interpolative dividers are updated when the LSB of R is written using I²C. A good rule for calculating the transition time is: $5 * \text{Multisynth_Period} + 200 \text{ ns}$.

When using the frequency select pin, the transition time is on the order of 100 μs .

10. Can the Si5350 or Si5351 duplicate a PWM input?

Yes, just set the output to buffer the CLKIN signal. The Si5350 or Si5351 can easily buffer a PWM input.

Set the CLKx_SRC[1:0] bits in the CLKx Control register to 01. This bypasses the PLL/VCXO and MultiSynth™ synthesis stages and connects CLKx directly to the CLKIN input. See [AN619](#) for more details for 10-MSOP and 20-QFN parts and [AN1234](#) for more details on a 16-QFN part.

11. Does changing the drive strength through the control registers change the output slew rate?

Yes. Decreasing the drive strength from 8 mA increases the rise/fall times, and subsequently decreases the slew rate.

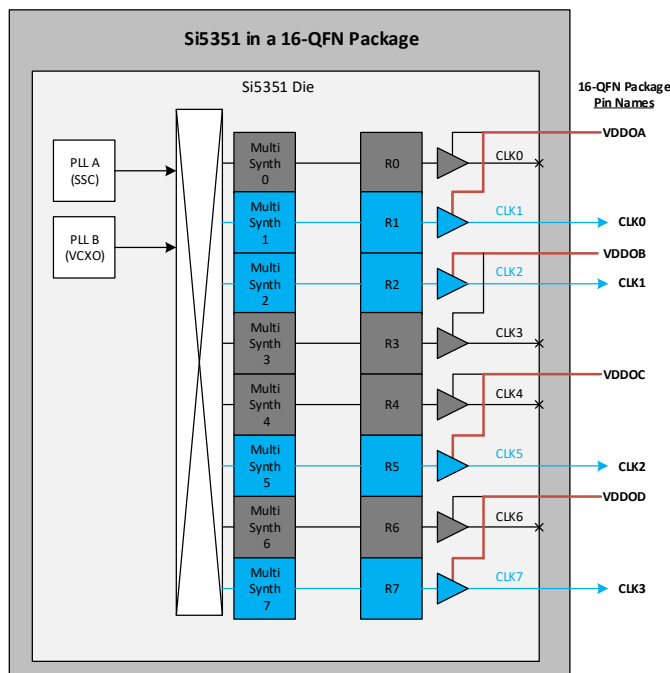
Note: The data sheet rise/fall times are all based on an 8 mA drive strength.

12. Why is there a separate programming guide (AN1234) for the 16-QFN Si5351?

The 3 x 3 mm 16-QFN Si5351 is a special four-output version of the original 4 x 4 mm 20-QFN Si5351. Each output on the 16-QFN part has its own individual VDDO supply. This isolation of the outputs from one another dramatically reduces crosstalk, improving the jitter performance of the device.

The 16-QFN Si5351 uses the same die as the 20-QFN Si5351. For the 20-QFN package, all eight outputs are bonded out to external pins on the package. However, for the new 16-QFN package, only a subset of the original eight outputs were bonded out to pins.

The diagram below shows the relationship between the outputs of a 20-QFN and a 16-QFN Si5351. CLK0, CLK3, CLK4, and CLK6 are no longer used (outlined in gray). Instead, CLK1, CLK2, CLK5, and CLK7 are used (outlined in blue), and they become the new CLK0, CLK1, CLK2, and CLK3 for the 16-QFN part.



This concept becomes important when programming the Si5351 by hand, without the help of ClockBuilder Pro. CLK0, CLK1, CLK2, and CLK3 of the 16-QFN part still use the registers assigned to the original CLK1, CLK2, CLK5, and CLK7 referred to in [AN619](#). This crossover could become problematic, especially when configuring the numerous output dividers.

[AN1234](#) was created to simplify this crossover. All register names were converted over to match the 16-QFN nomenclature. For example, register 17 now refers to CLK0 Control instead of CLK1 Control. Aside from that, all of the same 20-QFN formulas and design concepts still apply to the 16-QFN.

It is always recommended to use ClockBuilder Pro to configure any Si5351, either by creating custom orderable part numbers or by creating register exports for in-system volatile programming. However, for those who want to still program the 16-QFN device by hand, [AN1234](#) should make that easier.

13. Why does CLK3 on a 16-QFN Si5350 or Si5351 show a phase shift from the other outputs?

For output frequencies below 3.5 MHz, CLK3 can demonstrate a phase shift from CLK0, CLK1, and CLK2 on the 16-QFN Si5350 or Si5351, even if those outputs are programmed to the same output frequency.

MultiSynth3 (MS3), which is the output divider for CLK3 in a 16-QFN package (also the same as MS7 for CLK7 for a 20-QFN package), can only be set to divide ratios of even integers between 6 and 254. See [AN1234](#). The MultiSynths for CLK0, CLK1, and CLK2 do not have this limitation as they can be set to 4, 6, 8, and any fractional value between 8 and 2048.

16-QFN Si5351 Output MultiSynth Dividers	Allowed Divide Values
MS0, MS1, MS2	4, 6, 8, and fractional values between 8 and 2048
MS3	Even integer between 6 and 254

This difference can come into play for output frequencies less than 3.5 MHz. To achieve those lower frequencies, CLK3 is forced to begin using its R divider in conjunction with MS3, while the other clock outputs are still able to use the much larger range of their MultiSynth. This means that there can be different output divider solutions for the same frequency.

If the output divider solution between two clocks at the same frequency is different, we cannot assure that they are phase-aligned due to the differences in delay caused by the different divide values.

14. What is the minimum PLL lock range of the Si5350 or Si5351?

The PLL can track any abrupt input frequency changes of 3 to 4 percent without losing lock to it. Any input frequency changes greater than this amount do not necessarily track from the input to the output.

15. Is there a ppm/°C output error or ppm output error over time spec for the Si5350 or Si5351 devices?

No. Depending on the frequencies needed, most outputs can be generated with a 0 ppm error. Essentially, this means any error at the output is due to inaccuracies in the crystal selected and not from the Si5351A.

The device works on multiply/divide ratios and has a resolution of 20 bits, which translates roughly to 0.1 ppm worst-case frequency synthesis error.

16. What are the Si5350 or Si5351 power-up sequencing requirements for VDD/VDDO? What if I can't meet it?

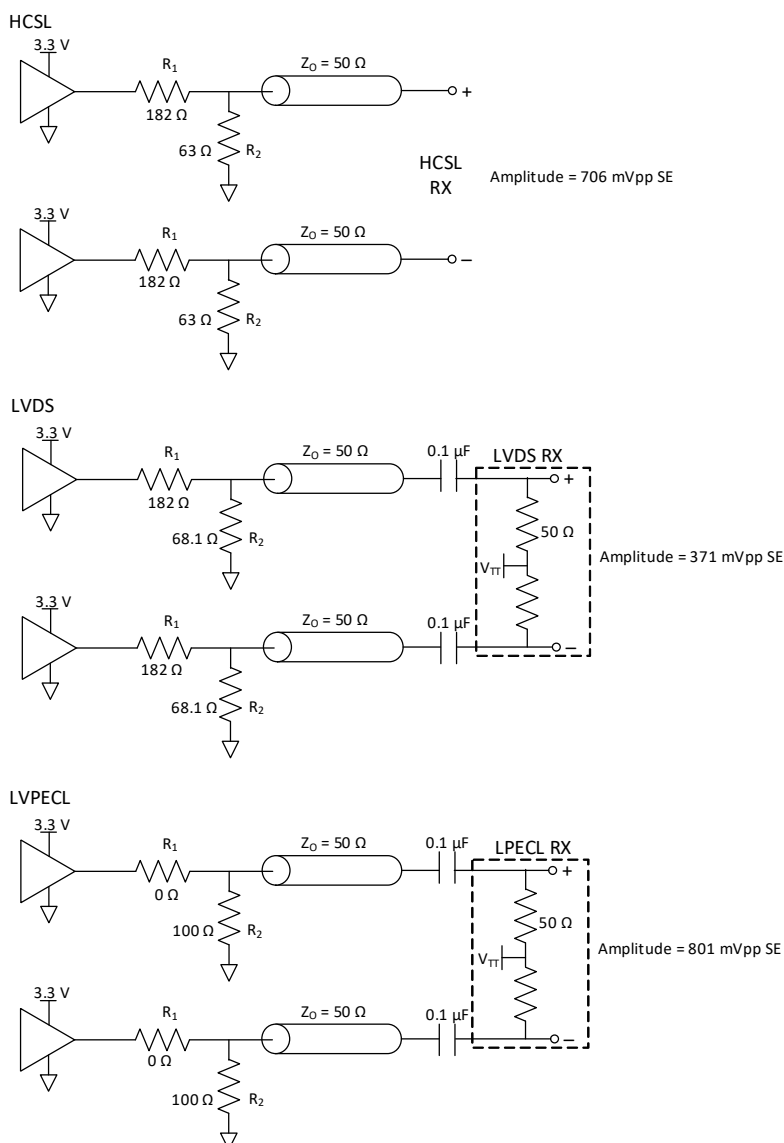
The VDDOx should come up either before or at the same time as VDD. A PLLA_RST and PLLB_RST can be performed by writing a 1 to reg177 and bits 5 and 7 respectively to realign the output-to-output phase skew.

Note: The Si5351 (I²C-controlled version) is required to perform PLL reset. This is not possible with the Si5350.

17. How do you interface Si5350 or Si5351 clock outputs to HCSL, LVDS, and LVPECL receivers?

The Si5350 or Si5351 clock outputs can emulate some of the most common differential I/O interface standards. To generate a differential signal, two clock outputs of the same frequency must be used. In addition, one clock must be inverted 180 degrees out of phase with respect to the other.

By default, all clock outputs are in phase. Invert one of the two output clocks by setting CLKx_INV = 1. For 20-QFN and 10-MSOP devices, see [AN619](#). For 16-QFN devices, see [AN1234](#) for programming instructions. The circuits required to interface to each of these standards are shown below.



18. Revision History

Revision	Date	Description
A	August, 2025	Initial Skyworks document release.

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