APPLICATION NOTE

AN1435: Si53x/Si55x/Si57x/Si59x XO and VCXO Frequently Asked Questions

This document answers the most frequently asked questions (FAQs) for the Si53x/Si55x/Si57x/Si59x XO and VCXO products. See Table 1 for more details on the devices covered by this document.

Table 1. Covered Products

Type	Product	Number of Frequencies	OE Pin	Phase Jitter (fs RMS)	Frequency Range (MHz)
Low jitter XO	Si530	Single	1 or 2	300	10 to 1417
	Si531	Single	1		
	Si532	Dual	2		
	Si533	Dual	1		
	Si534	Quad	2		
	Si570	Any (I^2C-enabled)	2		
Low jitter VCXO	Si550	Single	2	500	10 to 1417
	Si552	Dual	n/a		
	Si554	Quad	2		
	Si571	Any (I^2C-enabled)	2		
General purpose XO	Si590	Dual	1 or 2	500	10 to 810
	Si591	Quad	1		
	Si598	Any (I^2C-enabled)	2		
General purpose VCXO	Si595	Single	2	700	10 to 810
	Si596	Dual	n/a		
	Si597	Quad	2		
	Si599	Any (I^2C-enabled)	2		

Table 2. Frequently Asked Question Links

Question Category	Cross-Reference Link
Packaging	1.1. "Are pinouts, PCB land patterns, and package dimensions compatible with industry standards?"
	1.2. "What is the material composition of the pins?"
	1.3. "Is the plating process immersion gold, electroless gold or electrolytic?"
	1.4. "What is the Moisture Sensitivity Level (MSL) of the ceramic packages?"
	1.5. "Are the CLCC packages hermetically sealed?"
	1.6. "Are any flame retardants (halogen compounds) used in these devices?"
Quality and production	2.1. "Where can I find RoHS, REACH, or other materials-related compliance information?"
	2.2. "Are the oscillator products available in tape and reel?"
Thermal and soldering	3.1. "What is the maximum operating junction temperature of these devices?"
	3.2. "What are the ΘJA, ΘJB, and ΘJC for these devices?"
	3.3. "What is the typical temperature rise of these devices?"
	3.4. "Are the devices compatible with both leaded and “lead-free” assembly processes?"
	3.5. "What are the max reflow temperatures and profiles recommended for “lead-free” and “leaded” solder reflow processes?"
	3.6. "How many solder reflow cycles can the crystal oscillators support?"
General part functionality	4.1. "Can these oscillators output a sinusoid waveform instead of a square wave?"
	4.2. "Can VDD be set to a voltage other than the recommended driver voltage (e.g., when running a 3.3 V LVDS part at 2.5 V)?"
	4.3. "What is the power supply bypassing and filtering recommendations for these oscillators?"
	4.4. "How are the differential output buffers tristated?"
	4.5. "What is the frequency versus temperature behavior of these oscillators?"
	4.6. "Is it acceptable to route traces directly beneath these crystal oscillators?"
I^2C communication (Si570/71 and Si598/99 devices only	5.1. "What is the I2C address of my I2C programmable oscillator?"
	5.2. "Is the I2C bus working correctly?"
	5.3. "What are some troubleshooting suggestions to consider if there are general I2C communication problems?"
	5.4. "Are the I2C inputs on a 1.8 V or 2.5 V Si570/71 or Si598/99 3.3 V-tolerant?"
	5.5. "When is a voltage translator needed when interfacing the Si570/71 or Si598/99?"
	5.6. "What are the digital threshold levels for SCL and SDA?"
	5.7. "Are there any specific differences that make the Si570/71 and Si598/99 I2C compatible as opposed to I2C conformant?"
	5.8. "What speeds of operation can these devices support?"
	5.9. "Do these devices support clock stretching?"
	5.10. "What is the recommended approach to implement I2C voltage level translation?"

Table 2. Frequently Asked Question Links (Continued)

Question Category	Cross-Reference Link
I^2C programming procedure (Si570/71, Si598/99 devices only)	6.1. "Is the correct Si570/71 register bank being written based on device stability?"
	6.2. "Why do we need to calculate fXTAL when reconfiguring the output clock for large changes in output frequency?"
	6.3. "What is the tuning resolution?"
	6.4. "What kind of memory is used in the device?"
	6.5. "Can I change the default startup frequency or the I2C address?"
	6.6. "How is speed grading implemented?"
	6.7. "What happens if we attempt to program a new frequency outside of the specified speed grade of the device?"
	6.8. "What determines whether the DCO needs to be “frozen” when programming a new frequency?"
	6.9. "How does freezing the DCO help?"
	6.10. "Why is there a max Unfreeze to NewFreq Timeout spec?"
	6.11. "Is the Unfreeze to NewFreq timeout spec being exceeded?"
	6.12. "Why does the device reset when attempting a large frequency step without properly freezing the DCO?"
	6.13. "What is the “anchor” frequency?"
	6.14. "What happens to the output clock when making frequency changes?"
	6.15. "Does the device respond if every transaction is terminated by a stop before another start is sent?"
	6.16. "Should a delay be assumed for RST_REG just as with power up?"
	6.17. "What is a good software delay to use after a RECALL or RST_REG?"
	6.18. "What is the difference between RECALL and RST_REG?"
	6.19. "If one chooses to assert a RECALL, what is the general sequence of operations?"
	6.20. "Is there a significant advantage to asserting a RECALL as opposed to a RST_REG?"
VCXO functionality	7.1. "What is Absolute Pull Range (APR)?"
	7.2. "Why is there no min APR listed for 2.5 V or 1.8 V for certain Kv values?"
	7.3. "What is the resolution of the VC ADC in these devices?"
	7.4. "What is the input capacitance looking into the control voltage pin of these VCXOs?"

Table 3. Product Links

Link Type	Link
Oscillator part number lookup utility	tools.skyworksinc.com/TimingUtility/timing-part-number-search-results
Oscillator product pages	www.skyworksinc.com/Products/Timing-Oscillators
Oscillator phase noise lookup utility	www.skyworksinc.com/tools/oscillator-phase-noise
Evaluation boards/development kits	www.skyworksinc.com/Products/Timing/Evaluation-Kits#collapseOscillator
Programmable oscillator calculator	www.skyworksinc.com/en/application-pages/Programmable-Oscillator-Software
Quality and reliability reports	www.skyworksinc.com/Quality
Request technical support	www.skyworksinc.com/support

Table 4. Relevant Application Notes

Link Type	Link
Application note	AN587: Output Termination Guide
	AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)

1. Packaging

1.1. Are pinouts, PCB land patterns, and package dimensions compatible with industry standards?

Yes, the single frequency devices allow drop-in replacement of existing XOs or VCXOs. The dual and quad frequency devices allow drop-in or minimal change replacement of many similar XOs or VCXOs.

PCB land pattern and package dimension information can be found in device data sheets on the Oscillators product pages.

1.2. What is the material composition of the pins?

The pad composition on the 5 x 7 mm and the 3.2 x 5 mm CLCC package is NiAu (Nickel Gold):

- Ni (Nickel) thickness ranges between 1.27 and 8.89 µm.
- Au (Gold) thickness ranges between 0.3 and 1.0 µm.

Refer to the Skyworks Certificate of Conformance web page (search by part number) to find the Certificate of Conformance for the materials used in this device.

1.3. Is the plating process immersion gold, electroless gold or electrolytic?

These oscillators use an electroless gold process.

1.4. What is the Moisture Sensitivity Level (MSL) of the ceramic packages?

Per the JEDEC specification (IPC/JEDEC J-STD-020C, July 2004), the devices are classified as MSL 1, which refers to the lowest moisture sensitive classification level.

Although the JEDEC specification applies to “non-hermetic” (e.g., plastic) packaging, Skyworks tests the MSL of our oscillator products according to the JEDEC specification noted above.

1.5. Are the CLCC packages hermetically sealed?

Yes, the CLCC cavity is hermetically sealed during the lid sealing process.

1.6. Are any flame retardants (halogen compounds) used in these devices?

No, Skyworks oscillator packages are halogen- and phosphorous-free.

2. Quality and Production

2.1. Where can I find RoHS, REACH, or other materials-related compliance information?

Refer to the Skyworks Certificate of Conformance web page for full RoHS, REACH and other material composition information. Type the entire part number, including the dash suffix.

2.2. Are the oscillator products available in tape and reel?

Yes, all oscillator products are available in tape and reel.

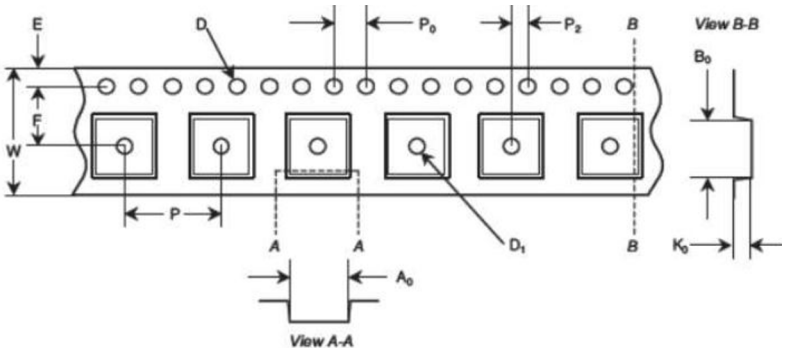
To specify tape and reel, please include the “R” suffix on the part number when you place your oscillator order. Refer to the Look Up an Oscillator or Clock web page for additional part number information. For example, the “R” at the end of the 530AA100M000DGR part number specifies the tape and reel option.

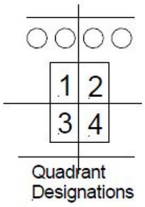
Note: *Part numbers that do not include an "R" suffix are shipped in coil tape which uses the same carrier tape dimensions with trailer and footer, but does not include a reel hub. Coil tape part numbers (without an "R" suffix) are typically only used for small quantity orders and tape and reel part numbers (with an "R" suffix) should be used for larger quantities.*

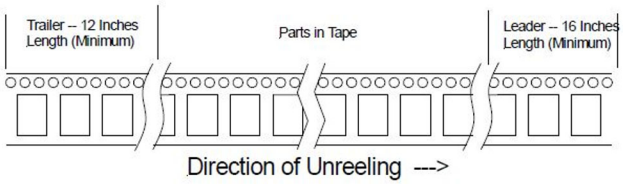
Tape and reel specifications are shown in Table 5, Table 6, Figure 1, and Figure 2, and quantity information for all Skyworks products is available upon request from your local sales representative.

Table 5. Tape and Reel Specifications

Pkg	No. of Leads	Package Description	Carrier Tape							Reel Size Diameter (inch)	Reel Hub Diameter (inch)	Pin-1 Orientation (Quadrant)
			Width	Pitch	Pocket Size				Parts per Meter			
			W (mm)	P1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	K1 (mm)				
CLCC	4, 6, 8	CLCC 3.2 x 5	12	8	3.7	5.5	1.4	N/A	125	7	2.5	1
CLCC	4, 6, 8	CLCC 5 x 7	16	8	5.6	7.6	1.9	N/A	125	7	2.5	1







Tape Pitch	8 mm
Minimum Number of pockets for leader	51
Minimum Number of pockets for trailer	39

Figure 1. Standard Carrier Tape Dimensions

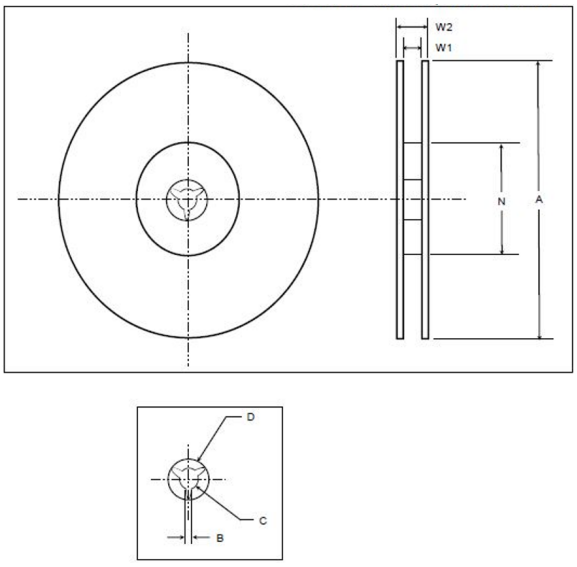


Figure 2. Reel Diagram (7 in.)

Table 6. Minimum Number of Pockets for Leader and Trailer (7-inch Reels)

		Symbol	Carrier Tape Width	
			12 mm	16 mm
Flange	Diameter (mm)	A	330.0	330.0
	Space between flange (mm)	W1	12.8	16.8
	Thickness (mm)	W2	18.2	22.2
Hub	Outer diameter (mm)	N	102.0	102.0
	Arbor hole diameter (mm)	C	13.0	13.0
	Key slit width (mm)	B	2.0	2.0
	Key slit width (mm)	D	20.2	20.2

2.3. What are the qualification test requirements for the Skyworks lead-free, RoHS-compliant, CLCC packages?

Because lead-free PCB assembly processes require higher reflow temperatures, the CLCC package assemblies have been qualified to be compatible with lead-free processes and temperatures. For representative package qualification tests, refer to Table 7. Final test results are included in the Si5xx Product Qualification Report.

Table 7. Qualification Test Requirements

Inspection Parameter	Method
Mechanical shock	MIL-STD-883, Method 2002
Mechanical vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and fine leak	MIL-STD-883, Method 1014
Physical dimensions	MIL-STD-883, Method 2016
Resistance to solder heat	MIL-STD-883, Method 2036
Wire pull and ball shear	MIL-STD-883, Method 2011
Die shear	MIL-STD-883, Method 2019
Internal moisture content	MIL-STD-883, Method 1018
External visual	MIL-STD-883, Method 2009
Internal visual	MIL-STD-883, Method 2014
HT storage	JEDEC JESD22 JA103
ELFR	JEDEC JESD22 JA108
Temperature cycle	JEDEC JESD22 JA104
HTOL	JEDEC JESD22 JA108

3. Thermal and Soldering

3.1. What is the maximum operating junction temperature of these devices?

The devices were designed to support a maximum operating junction temperature of 125 °C. This internal temperature should not be exceeded during device operation.

Operating ambient temperature range is –40 °C to +85 °C. Operation at temperatures outside of this range poses the risk of not meeting data sheet performance specifications.

The absolute maximum operating junction temperature above which damage may occur is T_J = 150 °C.

3.2. What are the Θ_{JA}, Θ_{JB}, and Θ_{JC} for these devices?

Table 8. Thermal Resistance and Characteristics

Device	Package	Θ_{JA} (°C/W)	Θ_{JC} (°C/W)	Test Conditions	Max Junction Temp (°C)
Si53x, Si55x, Si57x, Si59x	5 x 7 mm CLCC	84.6	38.8	JEDEC four layer 2S2P	125
Si59x only	3.2 x 5 mm CLCC	31.1	13.3		

Θ_{JA} has been estimated previously to be approximately 40 °C/W based on measurements using our evaluation boards.

Note: *The evaluation board layout, traces, connectors, etc. drop the lid case temp from an expected simulated 23 °C temp rise to a cooler, measured 9 °C temp rise.*

3.3. What is the typical temperature rise of these devices?

In still air when directly soldered to a multilayer board, the temperature rise from self-heating, as measured on the device surface, is approximately 9 °C. If the device is mounted in a small spring latch socket, temperature rise may increase to between 20 °C and 30 °C.

3.4. Are the devices compatible with both leaded and “lead-free” assembly processes?

Yes, the NiAu lead finish on the device is compatible with both leaded (SnPb) and “lead-free” solder processes and pastes.

3.5. What are the max reflow temperatures and profiles recommended for “lead-free” and “leaded” solder reflow processes?

For lead-free processes, the Peak/Classification Temperature (Tp) is 260 °C. For leaded (SnPb) processes, the Peak/Classification Temperature (Tp) is 240 °C.

Refer to the latest JEDEC specification (IPC/JEDEC J-STD-020C, July 2004). Excerpts below are included for reference only, to be used as starting values for developing a specific assembly profile. All temperatures refer to the top side of the package, measured on the package body surface.

Table 9. JEDEC J-STD-020 Specification Excerpt (Reference Only)

Profile Feature	SnPb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)	3 °C/second max	3 °C/second max
Preheat: • Temperature min (Tsmin) • Temperature max (Tsmax) • Time (Tsmin to Tsmax)	 100 °C 150 °C 60 to 120 seconds	 150 °C 200 °C 60 to 180 seconds
Time maintained above: • Temperature (TL) • Time (tL)	 183 °C 60 to 150 seconds	 217 °C 60 to 150 seconds
Peak/Classification Temperature (Tp)	240 °C	260 °C
Time within 5 °C of Tp	20 seconds	20 to 40 seconds
Ramp-down rate	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max

3.6. How many solder reflow cycles can the crystal oscillators support?

Skyworks crystal oscillators are compliant with JEDEC J-STD-020. It is safe to reflow these devices up to three times at the peak reflow temperature.

4. General Part Functionality

4.1. Can these oscillators output a sinusoid waveform instead of a square wave?

No, these devices are only designed to produce square waves.

4.2. Can VDD be set to a voltage other than the recommended driver voltage (e.g., when running a 3.3 V LVDS part at 2.5 V)?

Skyworks oscillators are carefully characterized over process, voltage, and temperature so we can confidently assure the minimum, typical, and maximum specifications listed in the data sheets. Although the oscillator may still function at voltages other than the specified driver voltage, important data sheet specs like jitter can no longer be assured if the device is operated outside its specified voltage.

4.3. What is the power supply bypassing and filtering recommendations for these oscillators?

These hybrid devices each contain a significant amount of internal bypass capacitance. There is a discrete X7R 0.01 µF bypass capacitor internal to the package and a few 100 pF on the die.

To be conservative, we generally recommend adding an additional 0.01 uF bypass cap close to the VDD pin on the device.

4.4. How are the differential output buffers tristated?

When OE is de-asserted, the output drivers go into tristate mode so that each output pin has ≥ 1 MΩ resistance to VDD or GND. When tristated, leakage current outputs are shorted to a rail are ~0.1 µA up to 2 µA.

For differential output modes, the tristated buffer is disconnected from VDD so that the Common Mode (CM) output resistance to VDD is ≥ 1 MΩ.

The nominal Differential Mode (DM) output resistance (i.e., between CLKOUT+ and CLKOUT-) is as follows:

- LVPECL: 400 Ω
- CML, LVDS: 200 Ω

4.5. What is the frequency versus temperature behavior of these oscillators?

The frequency versus temperature behavior of these oscillators is dominated by the temperature characteristic curve of the internal crystal which is used as a reference by the DSPLL®.

Figure 3 is a graph containing the frequency versus temperature curve for a 125 MHz XO with an internal 114.285 MHz third overtone crystal that has ± 20 ppm temperature stability, which applies to the Si53x, Si55x, and Si57x devices.

This curve is applicable to all similarly configured XOs and VCXOs with V_C set to 0 V.

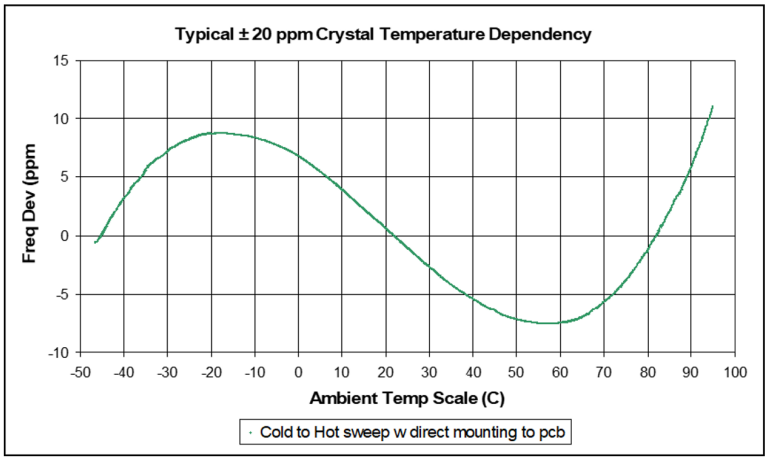


Figure 3. Frequency versus Temperature Behavior

4.6. Is it acceptable to route traces directly beneath these crystal oscillators?

These devices all use CLCC packages. Therefore, the bottom of the package, excluding the pads, is insulated and traces can be routed directly beneath the device without shorting. Even if there is room, this is not generally recommended since oscillator noise can couple to the traces.

It is much better to route traces on the other side of the PCB or internally, where there is at least one intervening reference plane (i.e., a GND plane or well-bypassed VDD plane between the traces and the oscillator).

5. I²C Communication (Si570/71 and Si598/99 Devices Only)

5.1. What is the I²C address of my I²C programmable oscillator?

Try using the Skyworks online Look Up an Oscillator or Clock to find the I²C address. Type in the full custom part number into the search bar and click **Search**. The resulting page shows all of the custom features associated with that part number, including the I²C address.

The I²C address is a 7-bit address. Our experience with MCUs has been to place the 7 bits in the upper bits of an 8-bit word with the LSB reserved for the data direction bit. In other words, to send 0x55 as the I²C address in a write command, the bit order would look like this:

Sub-Node Address	Data Dir Bit
1010101	0
0xAA	

5.2. Is the I²C bus working correctly?

Probing the device I²C pins with an oscilloscope can sometimes reveal signal integrity problems. Skyworks oscillator I²C communication is normally very robust, so if other devices on the I²C bus are communicating successfully, then the Skyworks oscillator I²C should also work.

5.3. What are some troubleshooting suggestions to consider if there are general I²C communication problems?

- Can you confirm I²C communication by reading the contents of registers 07 to 12?
  - You should be able to verify that they are appropriate for the programmed startup frequency. If not, there may be a hardware or timing problem. Here are some follow-up questions and suggestions.
- Are there pullups on the I²C bus?
- Is the programmed I²C address correct and is the device being addressed correctly?
- Is the NewFreq assertion arriving within 10 ms of unfreeze?
  - See the programming constraints table in the data sheet.
- Are read commands terminated properly?
  - Make sure that the master is sending a Not Acknowledge and a Stop after the last read data byte to terminate the read command.

5.4. Are the I²C inputs on a 1.8 V or 2.5 V Si570/71 or Si598/99 3.3 V-tolerant?

No. Digital I/O signals should be limited to a maximum voltage within the nominal VDD range supplying the device (i.e., 1.8 V, 2.5 V, or 3.3 V). While the device may operate otherwise (e.g., 3.3 V I/O into a 2.5 V device), it is not specified for this and reliability may be degraded.

5.5. When is a voltage translator needed when interfacing the Si570/71 or Si598/99?

The I^2C pullup resistors should be tied to the same VDD as the oscillator. The master needs to be able to read and write on the I^2C bus using these same pull ups. If that is not the case, then a voltage translator is recommended.

For example, the C8051F320 MCU uses open emitter outputs that can support direct connection of its I^2C lines to an Si57x/Si59x with pull ups to 2.5 V or 3.3 V. However, the MCU itself runs on nominal 3.3 V and has difficulty understanding the difference between a 1.8 V logic HIGH and LOW. In this case, one can employ a voltage translator such as the NXP® GTL2002 which is a 2-bit bidirectional low voltage translator. The MCU side of the translator is pulled up to 3.3 V and the DUT side is pulled up to 1.8 V.

5.6. What are the digital threshold levels for SCL and SDA?

The I^2C interface VIH and VIL specs are the same as that specified for Output Enable (OE) in the device data sheet. The Si570/71 and Si598/99 digital I/O V_{IH} and V_{IL} are specified as 0.75 x V_{DD} min and 0.5 V max, respectively.

5.7. Are there any specific differences that make the Si570/71 and Si598/99 I^2C compatible as opposed to I^2C conformant?

One specific difference regards digital thresholds. These devices are designed to operate using several nominal supplies (i.e., VDD = 1.8 V, 2.5 V, or 3.3 V). As noted above, VIH and VIL are specified as 0.75 x VDD min and 0.5 V max, respectively. However, the I^2C spec states that VDD-related input levels VIH and VIL should be 0.7 x VDD min and 0.3 x VDD max, respectively. For example, if VDD = 3.3 V, then VIL = 0.5 V which is less than the I^2C spec 0.3 x 3.3 V = 0.99 V.

The second specific difference is SCL. SCL is bidirectional per the I^2C standard. However, it is only an input to the device. Therefore, unlike other I^2C sub-nodes, the Si570/71 or Si598/99 does not have the ability to hold SCL down until ready.

5.8. What speeds of operation can these devices support?

- 100 kbps: standard mode
- 400 kbps: fast mode

5.9. Do these devices support clock stretching?

No. While the Serial Clock Line (SCL) is generally bidirectional per the I^2C standard, it is only an input to the device. Therefore, they cannot hold SCL down to delay communication.

5.10. What is the recommended approach to implement I^2C voltage level translation?

The digital I/O, including SCL and SDA, are based on standard foundry I/O cells which have not been modified for the I^2C input voltage requirements. This is why SDA VIL = 0.5 V max.

The Skyworks Si5xx-PROG-EVB supports multi-VDD testing of the Si514 and Si570 devices and other similar EVBs using a Texas Instruments® PCA9306 instead of a PCA9517. This is the recommended approach to implement I^2C voltage level translation.

6. I²C Programming Procedure (Si570/71, Si598/99 Devices Only)

6.1. Is the correct Si570/71 register bank being written based on device stability?

The Si570 and the Si571 devices use different configuration registers for 7 ppm temperature stability devices than they do for 20 ppm or 50 ppm temperature stability devices. The temperature stability of a Si570 or a Si571 can be confirmed using Look Up an Oscillator or Clock.

You can also see the second ordering option code in the full Si570 or Si571 part number to determine the stability.

Note: *Si598/99 does not change registers based on device stability and always use registers 7 to 12.*

Table 10. Device Stability Options

Second Ordering Option Code	Selected Stability Option	Configuration Register Addresses (Decimal)
A	50 ppm temperature stability, 61.5 ppm total stability	7 to 12
B	20 ppm temperature stability, 31.5 ppm total stability	7 to 12
C	7 ppm temperature stability, 20 ppm total stability	13 to 18

6.2. Why do we need to calculate f_{XTAL} when reconfiguring the output clock for large changes in output frequency?

Each device has a unique crystal. The crystal frequency is nominally 114.285 MHz for the Si570/71 devices and is 39.17 MHz for the Si598/99 devices, but may be offset from this value by ± 2000 ppm. We calculate f_{XTAL} in order to determine the exact crystal frequency, then use this information to adjust the DSPLL feedback divider ratio and output divider ratios.

The procedure for determining the internal crystal frequency from the register values of a device is described in the device data sheets.

$$Fxtal = \frac{(Fout \times HSDIV \times N1)}{RFREQ}$$

Note: *The RFREQ used in the above equation is the register value divided by 2^28.*

It is a common error to calculate the internal crystal frequency for one device and then use that same crystal frequency for all later devices. This leads to offset errors in the output frequency accuracy from part to part. The internal crystal frequency must be calculated for each individual device.

6.3. What is the tuning resolution?

< 1 ppb.

6.4. What kind of memory is used in the device?

These devices use both registers and Non Volatile Memory (NVM). The NVM can only be burned once.

- NVM = 128 words (registers) x 8 bits, non-volatile write-once, programmed at factory, inaccessible by I^2C.
- RAM = 256 words (registers) x 8 bits, volatile, many registers reserved or inaccessible by I^2C.

The contents of NVM are loaded into the register space when the part boots up. These devices do not contain any flash memory.

6.5. Can I change the default startup frequency or the I^2C address?

No. The startup or power up frequency and I^2C address are programmed into the NVM at the factory. These items must be specified during the part number request process.

6.6. How is speed grading implemented?

Speed grading is implemented through divider restrictions as opposed to directly placing limits on output frequency. See the device data sheet “Ordering Information” section for the various speed grading options.

6.7. What happens if we attempt to program a new frequency outside of the specified speed grade of the device?

The output is squelched.

6.8. What determines whether the DCO needs to be “frozen” when programming a new frequency?

The Digitally-Controlled Oscillator (DCO) must be “frozen” as part of the reconfiguration sequence for large frequency steps. Small frequency steps are defined as frequency changes ≤ ±3500 ppm from the anchor frequency. Large frequency steps are defined as frequency changes > ±3500 ppm from the anchor frequency.

6.9. How does freezing the DCO help?

Freezing the DCO ensures that no one 8-bit register write causes an intermediate RFREQ value to be out of the ± 3500 ppm range (from the anchor frequency). Freezing is necessary when changing the upper 8 bits of RFREQ; otherwise the NVM is recalled asynchronously.

6.10. Why is there a max Unfreeze to NewFreq Timeout spec?

If the Digitally-Controlled Oscillator (DCO) runs out of tuning range, it resets and reloads the NVM. Reloading the NVM causes the device to revert to its originally programmed start-up frequency.

The NewFreq bit asserts an internal self calibration that re-centers the DCO at a newly programmed frequency so that it can meet spec over temperature. The output is squelched until the DCO is tuned to, and centered on, the newly programmed frequency.

6.11. Is the Unfreeze to NewFreq timeout spec being exceeded?

These devices require the DCO to be frozen when changing register values and then "unfrozen" and a calibration initiated by writing the NewFreq bit to restart it properly. If the Unfreeze and NewFreq writes are delayed by 10 ms or more, the internal state machine can timeout and cause the configuration to revert to default values.

This Unfreeze and NewFreq timing requirement is not usually a problem since the writes are done back to back, but if there is an interrupt or other system delay that may cause this 10 ms timing to be exceeded, it should be considered as a possible source of an issue when reprogramming the device.

6.12. Why does the device reset when attempting a large frequency step without properly freezing the DCO?

The DCO runs out of tuning range and cannot reach the new frequency. When this happens, the device resets and reloads the NVM. The output is squelched until the DCO is tuned to, and centered on, the programmed start-up frequency.

6.13. What is the "anchor" frequency?

The anchor frequency is the default start-up frequency or the new frequency obtained after following the large frequency step programming procedure.

6.14. What happens to the output clock when making frequency changes?

The output clock runs continuously during small frequency steps as long as the total frequency change from the anchor frequency is ≤ ± 3500ppm. The output clock will be squelched during a large frequency step for 10 ms or less.

6.15. Does the device respond if every transaction is terminated by a stop before another start is sent?

Yes.

6.16. Should a delay be assumed for RST_REG just as with power up?

Yes. Asserting internal reset RST_REG by writing 0x80 to register 135 resets all internal logic. The reset disrupts the I^2C communication link. It is as if the power has been recycled and the target device (Si57x/9x) is temporarily absent.

Under these conditions, it would be appropriate to implement a soft reset start up delay at least as long as the specified power up delay is ~10 ms. Another approach would be to have the master code loop and repeatedly attempt to communicate until the target is back up.

6.17. What is a good software delay to use after a RECALL or RST_REG?

We typically insert a delay of 15 ms or more after a RST_REG or RECALL to ensure that the I^2C is ready to work on the device.

6.18. What is the difference between RECALL and RST_REG?

Asserting a RECALL <Reg. 135 bit 0> maintains I^2C communication while asserting a RST_REG <Reg 135 bit 7> interrupts I^2C communication.

6.19. If one chooses to assert a RECALL, what is the general sequence of operations?

Here is a sequence that we have used previously:

RECALL → Freeze DCO → <Write New Config> → Unfreeze DCO + NewFreq

6.20. Is there a significant advantage to asserting a RECALL as opposed to a RST_REG?

No. There is a small time advantage to doing a RECALL over RST_REG. However, RST_REG is generally regarded as the safest method to return a register memory + NVM chip back to a known state. There is not a significant or practical advantage to picking one or the other approach for these devices.

7. VCXO Functionality

7.1. What is Absolute Pull Range (APR)?

Absolute Pull Range (APR) of a VCXO is the amount of pull range remaining after subtracting the worst case total stability of the VCXO from the total pull range of the VCXO. APR is useful because it describes the minimum pull range available for tracking a PLL reference clock.

Skyworks is very conservative when calculating both total pull range and total stability for the min APR calculation. All of the specs used to calculate pull range and stability are set to their worst-case tolerances, producing the minimum possible pull range and the maximum possible frequency stability offset. This is how Skyworks can assure minimum APR performance across all parts produced.

If the minimum APR recommendations from the data sheet are properly followed, Skyworks can assure that the VCXO will never run out of voltage control range over the lifetime of the part.

Refer to AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR) for a more in-depth description.

7.2. Why is there no min APR listed for 2.5 V or 1.8 V for certain Kv values?

The calculation of APR relies on both the total pull range of the part and the total stability of the part. Total pull range is directly proportional to the control voltage range and the chosen tuning slope (Kv) value:

$$\pm TotalPullRange = 0.5 \times ControlVoltageRange \times Kv$$

As VDD decreases, the available control voltage range also decreases. Similarly, if the tuning slope (Kv) is decreased, the full range of tunable frequencies dramatically decreases.

When VDD and Kv are low enough, the total pull range can get close to the total stability of the part, causing the min APR to be low. In cases where min APR is less than ± 20 ppm, the VCXO could potentially have difficulty tracking a PLL reference clock as the part ages over time.

7.3. What is the resolution of the VC ADC in these devices?

The analog control voltage is digitized in these devices using a delta-sigma converter with the output truncated to 18 bits.

7.4. What is the input capacitance looking into the control voltage pin of these VCXOs?

The input capacitance looking into the control voltage pin is nominally 50 pF.

8. Revision History

Revision	Date	Description
B	February, 2026	Updated tape and reel information.
A	November, 2025	Initial Skyworks document release.