APPLICATION NOTE

AN1456: Understanding Creepage and Clearance Requirements for Data Centers

1. Introduction

Modern architectures increasingly rely on higher distribution voltages, such as three-phase ac distribution and emerging 400 V_{DC}/800 V_{DC} power architectures to maximize efficiency and power density. However, these elevated voltages, combined with strict space constraints, significantly elevate the risk of electrical arcing and surface tracking.

This application note provides a comprehensive guide to navigating insulation coordination for data center hardware in accordance with the IEC 62368-1 standard. A critical aspect of compliance for modern data center equipment is understanding the paradigm shift in the regulatory landscape. For decades, the design of information technology equipment (ITE) like data centers was governed by IEC 60950-1, while audio/video electronics fell under IEC 60065. Recognizing that modern cloud hardware, telecom infrastructure, and AV devices have largely converged, the International Electrotechnical Commission (IEC) merged these two distinct frameworks into a single, hazard-based standard. As such, this document will discuss the pertinent definitions of IEC 62368-1 and how to align product selection with the requirements found therein.

2. Fundamental Concepts: Creepage vs. Clearance

Creepage and clearance both define the required distance between conductors at different potentials, or between a high-voltage node and an accessible chassis or ground. Despite this similarity, they address fundamentally different physical phenomena. As a result, each parameter is associated with distinct failure mechanisms and must be evaluated accordingly in system design.

3. Clearance

Clearance is defined as the shortest distance through the air between two conductive parts. This is the physical gap that prevents an electrical arc-over in air between these conductors. The primary physical mechanism governing clearance is the electrical breakdown strength of air. Air acts as an insulator until the electric field strength (E) exceeds its dielectric strength capability. Under standard atmospheric conditions, 3 kV/mm breakdown voltage is a common baseline, but this value heavily depends on air pressure and humidity, and can drop to 1 kV/mm in inhomogeneous fields. However, both numbers should be treated merely as rules of thumb. Paschen's law is the equation that gives the breakdown voltage between two conductive parts in air as a function of pressure and clearance.

For equipment supplied from the mains, the clearance distance is not determined solely by the continuous working voltage, as practical systems must also withstand significantly higher transient voltages. Instead, it is designed to withstand transient overvoltages (surges, generated by lightning strikes, grid switching or inductive kickback) that stem from the ac grid. To standardize the severity of these transients, international standards divide electrical systems into four Overvoltage Categories (OVC I to OVC IV) based on the physical location of the equipment relative to the mains power entry point as shown in Figure 1.

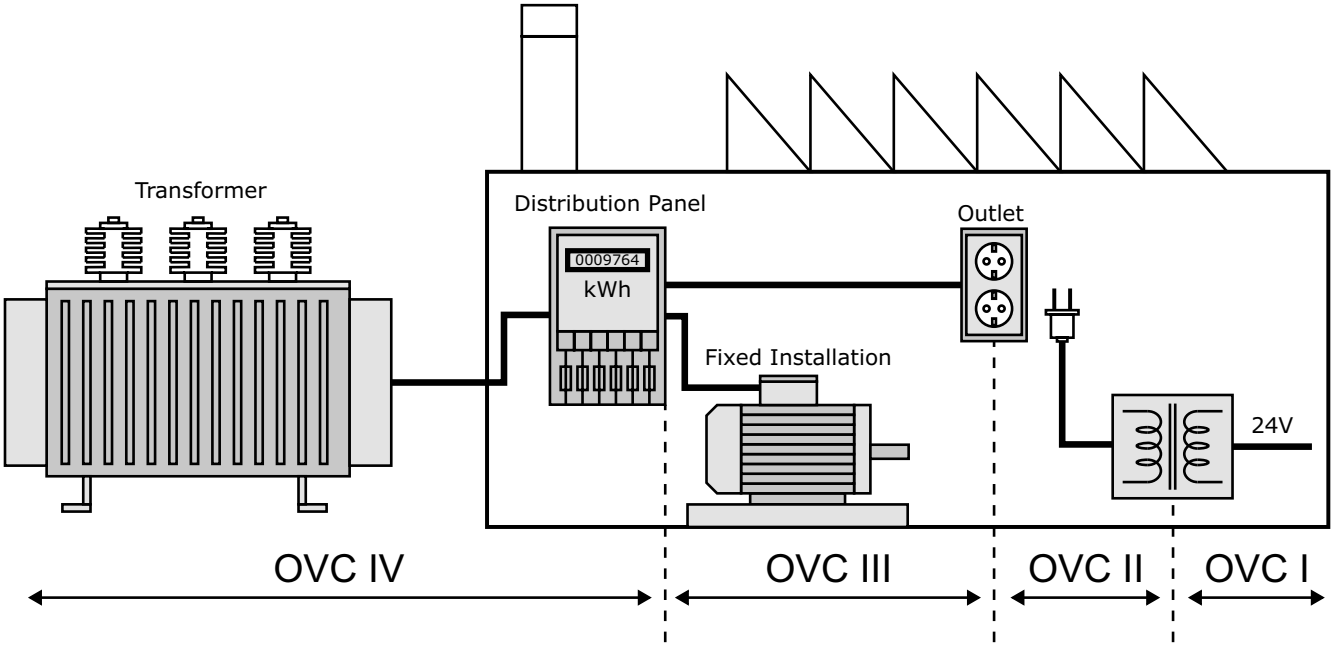

Figure 1. Overvoltage Categories

The corresponding transient withstand voltage must be derived from Table 1. Selecting the appropriate value from this table requires the equipment's nominal ac mains voltage system and the applicable OVC rating. It is a common rule of thumb that IT equipment racks and computing servers are typically deployed in the relatively well-protected Overvoltage Category II (OVC II) zones. For a nominal ac mains voltage up to 300 V_{RMS}, OVC II equipment must withstand transient overvoltages of up to 2500 V_{PK} without air-gap breakdown.

Table 1. IEC62368-1 Mains Transient Voltages

AC Mains Voltage (V_{RMS})	Mains Transient Voltage (V_{PEAK})			
	Overvoltage Category			
	I	II	III	IV
150 (including: U.S. 120 V single-phase, U.S. 120/240 V split-phase, and U.S. 120/208 V three-phase)	800	1500	2500	4000
300 (including: EU 230 V single-phase, EU 230/400 V three-phase, and U.S. 277/480 V three-phase)	1500	2500	4000	6000
600 (including: 400/690 V three-phase)	2500	4000	6000	8000

Moving upstream within the building architecture towards the physical grid entry point (origin of the installation), the electrical environment becomes increasingly severe and exposed to higher transient energy. Equipment at this level is no longer considered plug-in, but instead becomes an integral part of the fixed installation. Due to the proximity to the public supply network and the lower impedance of the connection, such equipment is subject to higher levels of transient overvoltage. Consequently, it must be assigned to a higher overvoltage category. Staying with the previous European example, the required breakdown withstand voltages rise from 2.5 kV_{PK} (OVC II) to 4 kV_{PK} (OVC III), and up to 6 kV_{PK} (OVC IV) at the origin of the installation.

When referencing ac mains voltage in the context of international safety standards (such as IEC 62368-1), the voltage value typically refers to the line-to-neutral (or line-to-earth) voltage, rather than the line-to-line voltage. For a standard European three-phase 400 V system, assuming a solidly grounded neutral (TN or TT distribution system), the line-to-neutral voltage is 230 V. Therefore, such an installation falls under the 300 V_{RMS} classification, resulting in a standard 2500 V_{PK} transient rating for OVC II environments. However, it is critical to note that this assumption only holds true if the neutral point is directly grounded. In systems with an ungrounded or impedance-grounded neutral (IT distribution networks), a single-phase to earth fault can elevate the voltage of the remaining phases to the full line-to-line level relative to earth. In such architectural scenarios, the system must be evaluated under the higher 600 V_{RMS} classification, which increases the required transient voltage rating to 4000 V_{PK} for OVC II.

After selecting the required overvoltage category, the required clearance value (in mm) can be selected from Table 2; however, the final clearance value is also highly dependent on the Pollution Degree of the environment. This quantifies the amount of dry pollution and condensation present in the immediate surroundings of the equipment. For controlled environments like modern data centers, pollution degree 2 (PD2) is the industry standard. This classification assumes that only non-conductive pollution occurs (though occasional temporary conductivity caused by condensation must be expected). Accounting for pollution degree ensures that the chosen air gap (clearance) remains reliable over the product's entire lifespan, preventing premature dielectric breakdown even under fluctuating environmental conditions.

When designing for electrical safety and establishing clearance distances, defining the required insulation level is the next critical step after determining the overvoltage category and pollution degree.

The core philosophy of IEC 62368-1 is built around protecting the user (referred to as the Ordinary Person). The standard operates on the fundamental principle that the immediate environment touched or accessed by a human must be strictly ES1 (touch-safe). To determine how much isolation is required, IEC 62368-1 classifies all electrical circuits into three distinct energy sources (ES) based on the severity of the shock hazard they present:

- **ES1 (Class 1 Energy Source)**
  Safe to touch. The voltage and current levels are low enough that they cannot cause pain or injury under normal or even a single fault condition (e.g., user accessible 24 V supply rail or CAN bus lines).
  Below 60 V_{DC}/2 mA_{DC} or 30 V_{AC}/0.5 mA_{AC}.
- **ES2 (Class 2 Energy Source)**
  Noticeable but not hazardous. The energy level can cause a slight sensation or pain, but it is not sufficient to cause injury under normal or even fault condition. Below 120 V_{DC}/25 mA_{DC} or 50 V_{AC}/5 mA_{AC}.
- **ES3 (Class 3 Energy Source): Hazardous Energy**
  This level can cause severe pain, muscular reaction, or fibrillation. For example an internal 400 V dc bus in a server PSU.

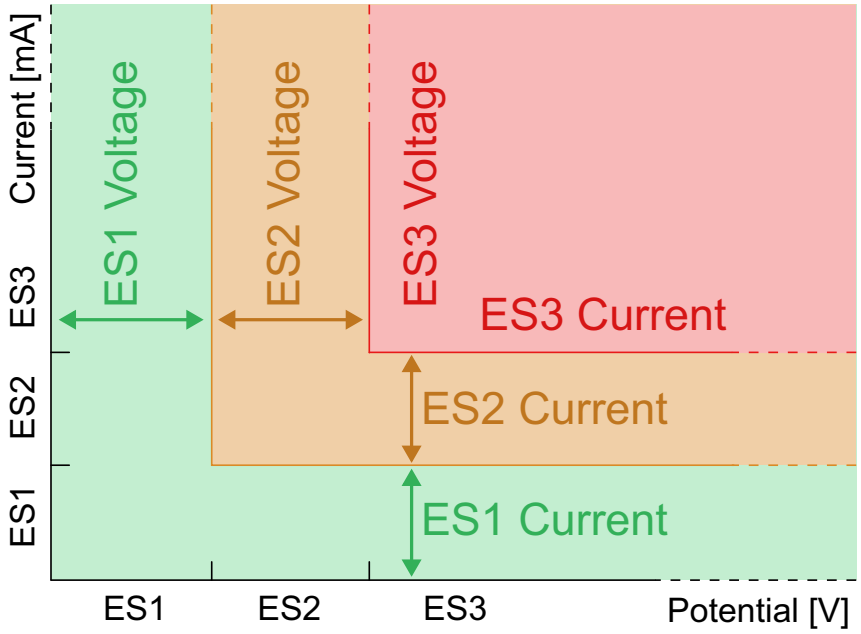

Figure 2. ES Limits for Voltage and Current

In practical layout and design, these safeguard rules translate as follows:

- **Between ES3 and ES1 (Double Safeguard Required)**
  Because ES3 represents a lethal hazard and ES1 must remain completely safe for human touch, a robust double safeguard framework is mandatory. This ensures that, under a single-fault condition (meaning the failure of any single protection layer), the secondary layer of protection remains intact to prevent the hazardous energy from reaching the user. This can be achieved via two distinct engineering methods, both of which provide two layers of protection but in different ways:
  - **Class II Approach**
    This uses only isolating materials either through double insulation or reinforced isolation without relying on a protective earth conductor. Both insulators provide the same level of safety, where double isolation uses distinct, physical basic insulation and supplementary insulation to achieve the same goal.
    Reinforced Insulation unites both of these insulators into a single layer.
  - **Class I Approach**
    The double safeguard requirement is met by combining Basic Insulation and Protective Earth (PE). The first layer of defense is the Basic Insulation that isolates the ES3 nodes from any accessible conductive metal part (such as the metal enclosure). And this conductive metal part is tied to the protective earth (PE) connection, acting as the supplementary safeguard. If the primary insulation fails, the grounded enclosure clamps the touch voltage to safe ES1 levels and forces an overcurrent trip upstream.
- **Between ES3 and ES2 (Boundary Protection)**
  When designing internal circuitry, a safeguard is still required between an ES3 and an ES2 domain. However, instead of a reinforced barrier, a Basic Safeguard (Basic Insulation) is typically sufficient here. Primarily, it prevents the ES2 domain from converting into an ES3 hazard.
- **Between ES2 and ES1 (User Protection)**
  Since an ES2 source possesses enough energy to cause pain and involuntary muscular reactions, user-accessible ES1 domains must be strictly isolated from it. A basic safeguard is also mandatory here to prevent ES2 energy from reaching a touchable surface.

To translate these theoretical safeguard requirements into concrete physical dimensions (millimeters) of clearances, circuit designers rely on the clearance data specified in IEC 62368-1. The following table from the standard converts the required impulse withstand voltage levels into mandatory minimum distances through air at different pollution degree conditions.

Table 2. IEC62368-1 Clearance Requirements

Required Withstand Voltage (V_{PK} or DC)	Basic Insulation or Supplementary Insulation (mm)			Reinforced Insulation (mm)		
	Pollution Degree			Pollution Degree		
	1	2	3	1	2	3
1500	0.5		0.8	1.0		1.5
2500	1.5			3		
4000	3.0			5.5		
6000	5.5			8.0		
8000	8.0			14.0		

The traditional view of data center power distribution assumes a single, uniform environment inside the building and insulation coordination models often limit their scope to indoor, protected environments. However, modern infrastructure designs regularly integrate systems located upstream of the white space or outdoors. To achieve compliance with IEC 62368-1, clearance parameters, whose requirements are detailed in the table below, must be evaluated based on the specific location Zone and Overvoltage Category (OVC) of each functional block.
Data centers are typically divided into these three zones:

- **Zone 1 (Requires OVC IV): Outdoor infrastructure and Renewables**
  Applies to co-located outdoor assets, such as 1500 V dc renewable generation fields. Systems in this zone are directly exposed to atmospheric transients and lightning surges, requiring the highest impulse withstand voltage baselines.
- **Zone 2 (Requires OVC III): Primary Conversion and Energy Storage**
  Applies to the primary, non-isolated low-voltage stages connected directly to the infrastructure's main power distribution system. Depending on the nominal system voltage, insulation coordination within this zone must support mains transient voltage (V_{PEAK}) of either 4000 V for systems rated up to 300 V_{RMS} (such as 277/480 V three-phase systems) or 6000 V for systems rated up to 600 V_{RMS} (such as 400/690 V three-phase systems). Typical hardware applications operating under this category include grid-tied bi-directional inverters, power conversion cells in solid-state transformers (SST), central 800 V or 1500 V dc-links, and primary energy storage system (ESS) controllers.
- **Zone 3 (Requires OVC II)**: **Protected Server Environment (White Space)**
  Applies to indoor, downstream power distribution and localized backup systems where mains transient voltages are already limited by upstream devices to lower baselines, typically to 2500 V. Typical hardware applications operating under this category include 1RU power shelves, server-level battery backup units (BBUs) or capacitor backup units (CBUs). In modern, high-density AI/HPC architectures, these infrastructure elements are typically centralized within a dedicated sidecar rack adjacent to the IT rack.

A typical Skyworks isolator in a wide-body SOIC-16 package provides a physical 8.0 mm clearance and a 6000 V mains transient withstand rating. Under IEC 62368-1 Procedure 2 insulation coordination rules, this package provides the following design capabilities across different overvoltage categories:

- **OVC II Environments (Reinforced Insulation)**
  Fully covers every transient impulse requirement defined within the IEC 62368-1 overvoltage table, including those for reinforced insulation distances. With its 6000 V capability and 8.0 mm physical clearance, it provides an inherent safety margin across all compliant grid-tied and intermediate voltage levels up to the 600 V line-to-neutral ceiling (including 400/690 V three-phase).
- **OVC III Environments (Reinforced Insulation)**
  Fully compliant. For grid-tied systems up to 600 V line-to-neutral (encompassing 230/400 V, 277/480 V, and 400/690 V three-phase systems), the standard dictates a maximum impulse voltage of 6000 V and a reinforced clearance requirement of exactly 8.0 mm. This package hits this boundary condition perfectly, eliminating the need for extended-pitch or custom components.
- **OVC IV Environments (Basic or Reinforced Insulation)**
  Capable of operating in lower-voltage OVC IV zones up to 300 V system voltages, such as 230/400 V three-phase, where the transient requirement is capped
  at 6000 V. For higher-voltage networks up to 600 V system voltages (such as 400/690 V), the physical 8.0 mm package clearance strictly meets the basic insulation requirement. It cannot be used for reinforced insulation in 600 V OVC IV zones, where the clearance demand steps up to 14.0 mm.

The ultimate limiting factor for an 8 mm clearance package in modern data center PSUs is the altitude rating. Data centers frequently require compliance up to 3000 meters (by Open Rack v3) or even 5000 meters above sea level. Because the less dense air has lower dielectric breakdown strength, IEC 62368-1 requires a clearance multiplication factor as listed in Table 3 below.

Table 3. Table 3. IEC62368-1 Altitude Multiplication Factors for Clearances

Altitude (m)	Multiplication Factor
2000	1.00
3000	1.14
4000	1.29
5000	1.48

Therefore, at an altitude of 5000 m, the package effective transient withstand voltage degrades below its nominal 6000 V rating due to the less air density. To evaluate compliance at elevated altitudes (3000 m and 5000 m), the standard sea-level clearance must be scaled up by the IEC 62368-1 multiplication factors of 1.14 and 1.48, respectively.

Table 4 below outlines the required clearances for reinforced isolation across various overvoltage categories and system voltages while evaluating the capabilities of the current Wide-Body (WB) SOIC package against the upcoming Ultra-Wide-Body (UWB) SOIC package.

Table 4. Wide-Body and Ultra-Wide-Body SOIC Package Capabilities

System Voltage (V_{RMS})	Overvoltage Category	Up to 2000 m			Up to 3000 m			Up to 5000 m		
		Required Clearance (mm)	WB SOIC 8.0 mm CLR	UWB SOIC 15.5 mm CLR	Required Clearance (mm)	WB SOIC 8.0 mm CLR	UWB SOIC 15.5 mm CLR	Required Clearance (mm)	WB SOIC 8.0 mm CLR	UWB SOIC 15.5 mm CLR
300 V (e.g., 230/400 V, 277/480 V)	**OVC II**	3.0	Yes	Yes	4.14	Yes	Yes	4.44	Yes	Yes
	OVC III	5.5	Yes	Yes	6.27	Yes	Yes	8.14	No	Yes
	OVC IV	8.0	Yes	Yes	9.12	No	Yes	11.84	No	Yes
600 V (e.g., 400/690 V)	**OVC II**	5.5	Yes	Yes	6.27	Yes	Yes	8.14	No	Yes
	OVC III	8.0	Yes	Yes	9.12	No	Yes	11.84	No	Yes
	OVC IV	14.0	No	Yes	15.96	No	No	20.72	No	No

While extreme altitudes highly increase clearance demands, the standard 8.0 mm wide-body SOIC package remains fully compliant and highly cost-effective up to 3000 m for 300 V systems in both OVC II (4.44 mm) and OVC III (6.27 mm) categories, as well as for 600 V systems in OVC II (6.27 mm). In fact, even at a 5000 m ceiling, this standard package remains competitive for lower-voltage OVC II categories where scaled requirements allow it to stay firmly in play. Looking ahead, the upcoming UWB SOIC package with 15.5 mm clearance will expand this coverage, ensuring compliance at both 3000 m and 5000 m across nearly all overvoltage categories, with the sole exception of the highly stringent OVC IV.

4. Creepage

While clearance (CLR) protects against instantaneous arcing through the air, creepage (CRP) protects against long-term, destructive breakdown along the surface of solid insulation (such as the FR4 PCB substrate or the plastic molding of an IC package). By definition, Creepage distance is the shortest path between two conductive parts measured along the surface of the insulation material, not in air.

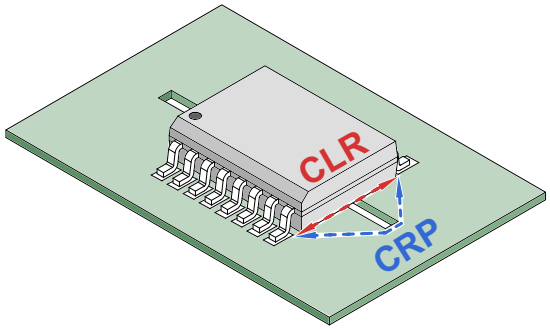

Figure 3. Clearance and Creepage Distances on a PCB

Creepage failure is a slow, environmental process. Over time, the surface of a PCB collects ambient moisture, dust, and microscopic manufacturing residues. Combined with electrical stress, a small leakage current begins to flow across this contaminated layer.

This current creates localized heating, which physically carbonizes the underlying FR4 substrate. Because carbon is highly conductive, this process creates permanent, conductive paths known as tracking. Eventually, the insulation fails completely, resulting in a catastrophic short circuit or fire. In contrast, inorganic materials (such as ceramics or glass) are inherently immune to carbon tracking.

Under IEC 62368-1, the mandatory creepage distance is calculated based on three distinct parameters:

1. **RMS Working Voltage, V_{RMS} or V_{DC}**
   Crucial Difference from clearance: Clearance is dictated by transient voltage peaks because air breaks down instantly at the highest voltage crest. Creepage, however, is a continuous process of thermal degradation. Therefore, you must look up creepage using the continuous RMS or dc working voltage.
2. **Pollution Degree (PD)**
   The dirtier and more humid the environment, the more susceptible the surface is to tracking.
3. **Material Group (CTI Rating)**
   Not all PCB laminates or component packages resist tracking equally. The standard classifies materials into four Material Groups based on their Comparative Tracking Index (CTI), the voltage at which the material starts to carbonize:
   a. **Material Group I**
      600 V < CTI (highly resistant category—most Skyworks isolators are in this group)
   b. **Material Group II**
      400 V < CTI < 600 V (special high-CTI grade PCBs, PA66 housed connectors)
   c. **Material Group IIIa**
      175 V < CTI < 400 V (standard FR4 PCBs and almost all standard IC packages)
   d. **Material Group IIIb**
      100 V < CTI < 175 V (low-grade plastics)

According to IEC 62368-1 creepage requirements table below, for Material Group I compounds in a Pollution Degree 2 environment, a very popular wide-body SOIC package with an 8.0 mm creepage distance supports up to 800 V_{RMS} for reinforced insulation (twice the creepage requirement for basic insulation) and up to 1600 V_{RMS} for basic insulation. However, in practical high-voltage semiconductor applications, such as digital isolators and isolated gate drivers, the continuous working voltage rating, V_{IOWM}, is typically capped around 1000 V_{RMS} to 1500 V_{RMS} by the manufacturers, governed by the internal dielectric reliability and high-frequency partial discharge constraints specified under IEC 60747-17, the component-level safety standard governing magnetic and capacitive isolation barriers.

Table 5. IEC62368-1 Creepage Requirements in Millimeters for Basic or Supplementary Insulation

RMS Working Voltage (V)	Creepage Requirements for Pollution Degree 2 (mm)		
	Material Group		
	I	II	IIIa, IIIb
100	0.71	1	1.4
125	0.75	1.05	1.5
160	0.8	1.1	1.6
200	1	1.4	2
250	1.25	1.8	2.5
320	1.6	2.2	3.2
400	2	2.8	4
500	2.5	3.6	5
630	3.2	4.5	6.3
800	4	5.6	8
1000	5	7.1	10
1250	6.3	9.0	12.5
1600	8.0	11.0	16.0

Table 6 summarizes the mechanical clearance and creepage dimensions for the Skyworks package portfolio. These package-level dimensions are provided to assist designers in selecting the appropriate package option for their specific creepage/clearance safety constraints.

Table 6. Clearance and Creepage Distances for Skyworks Standard Packages

Package	Measured Clearance (mm)	Measured Creepage (mm)
LGA-13/14 (IM), DFN32 (IF)	≥3.5	≥3.5
QSOP-16 (IU)	≥4.2	≥3.6
QSOP-20 (IU)	≥4.8	≥4.6
NB SOIC-8 (IS)	≥4.7	≥3.9
NB SOIC-16 (IS1)	≥4.7	≥3.9
WB SOIC-16 (IS)	≥8.5	≥7.6
WB SOIC-16 (IS2)	≥8.5	≥8
WB SOIC-14 (IS3)	≥8.5	≥8
WB SOIC-20/24 (IS)	≥8.9	≥7.6
SDIP6 (IS)	≥9.6	≥8
WB SSO8 (IS4)	≥9.5	≥8.5
WB SSOP-36 (AU)	≥8.6	≥8.6
Upcoming UWB SOIC	≥15.5	≥15.0

5. Material Group Mismatch

5.1. Isolator-to-PCB Material Group Mismatch

When designing high-voltage isolation barriers, engineers often face a frustrating discrepancy: the isolator package (gate driver or digital isolator) comfortably achieves compliance within a tight 8.0 mm footprint, while the underlying PCB requires significantly larger spacing to meet the exact same safety standard. This is known as the material group mismatch.

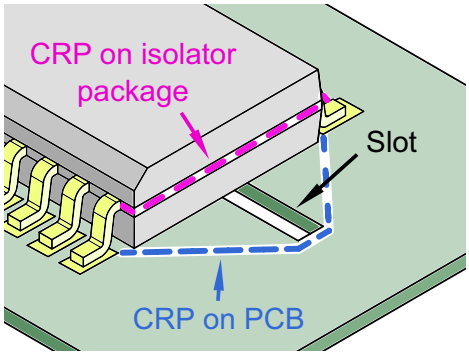

Figure 4. Creepage Distance Enhancement Using a PCB Cutout

The safety standards determine the required creepage distances based on the continuous working voltage, pollution degree, and the material group of the insulation. Material Groups are classified by their resistance to electrical tracking, measured via their CTI rating.

Mismatch occurs because semiconductor manufacturers and PCB fabricators use vastly different insulation mediums:

- **Isolator Package Compound (Material Group I)**
  Most Skyworks high-end isolator ICs utilize premium, high-purity mold compounds engineered to meet Material Group I (>CTI 600).
- **PCB Substrate (Material Group IIIa)**
  Standard, cost-effective base FR4 laminates typically feature a much lower tracking resistance, falling into Material Group IIIa (175 < CTI < 400, usually around 250).

Because the PCB surface is far more prone to moisture absorption, surface contamination, and subsequent tracking than the pristine plastic body of the IC, the safety standards penalize the PCB heavily.

Following is a real-world example:

Consider a system that has to be compliant to IEC 62368-1 having a Reinforced Insulation requirement of 800 V_{DC} in a Pollution Degree 2 environment. Table 7 below summarizes the differing creepage requirement for the two mediums.

Table 7. Clearance and Creepage Distances for Skyworks Standard Packages

Creepage Path	Material Group	Required Creepage
Along the package of the isolator	Material group I (CTI > 600)	8 mm
Along the PCB surface	Material group IIIa (175 < CTI < 400)	16 mm

Even if a wide-body SOIC package provides a perfect 8.0 mm of effective creepage from pin to pin along its package body, placing it onto a standard FR4 board instantly violates the safety standard because the creeping current can track across the inferior PCB surface, which legally demands 16.0 mm. To prevent the low-CTI FR4 board from forcing the use massive, exotic IC packages, power electronics designers use two primary layout strategies:

- **PCB Slotting**
  A process of milling a physical air gap through the FR4 substrate. This is the most effective and cost-efficient layout technique to physically increase the creepage distance on the higher material group FR4 substrate. Under most international standards, the width of the slot must be at least 1.0 mm (or 2.0 mm in highly polluted Pollution Degree 3 environments). If a slot is narrower than 1.0 mm, the standards assume that moisture, dust, or flux residues can easily bridge the gap, meaning the slot is legally ignored, and the full FR4 creepage rules still apply.
- **Applying a Certified Protective Coating**
  Conformal coating over the assembled PCB seals the FR4 surface from environmental dust and moisture. Under the safety standards, a proper coating on the PCB surface effectively decreases the Pollution Degree or invokes specific “printed board coating” clauses and can reduce the strict 16.0 mm requirement down to a level that fits the 8.0 mm component footprint.
  In power electronics and safety compliance (such as IEC 62368-1), conformal coating is treated as much more than just a protective layer against moisture and dust. Its impact on your PCB layout depends entirely on whether it is qualified as a Type 1 (Environmental) or a Type 2 (Insulating) coating.

  A standard Type 1 coating provides environmental reliability but offers no creepage relaxation. Applying this to a standard FR4 board (Material Group III), the Pollution Degree cannot be lower than PD2. Consequently, this coating merely provides an extra safety net against humidity and dust.

  To actually reduce your required pollution degree and creepage distances, you must use a fully certified Type 2 coating. This material undergoes rigorous qualifications (such as UL 746E testing) to prove it can act as true solid insulation. Type 2 coating effectively drops the micro-environment underneath to Pollution Degree 1 (PD1) and cuts the creepage requirement in half. However, achieving Type 2 compliance in production is especially difficult and costly.

6. Topological Workarounds for Overcoming Package Limits in Medium-Voltage SST Designs

In solid-state transformer (SST) applications connected to medium-voltage (MV) grids, a single semiconductor switch cannot directly withstand the full line voltage. To handle these multi-kilovolt levels, the standard architectural approach is to cascade several low-voltage converter cells in a series configuration on each phase input. This modular multilevel or cascaded topology naturally distributes the total grid voltage across multiple individual SST cells and power devices as shown in Figure 5 below.

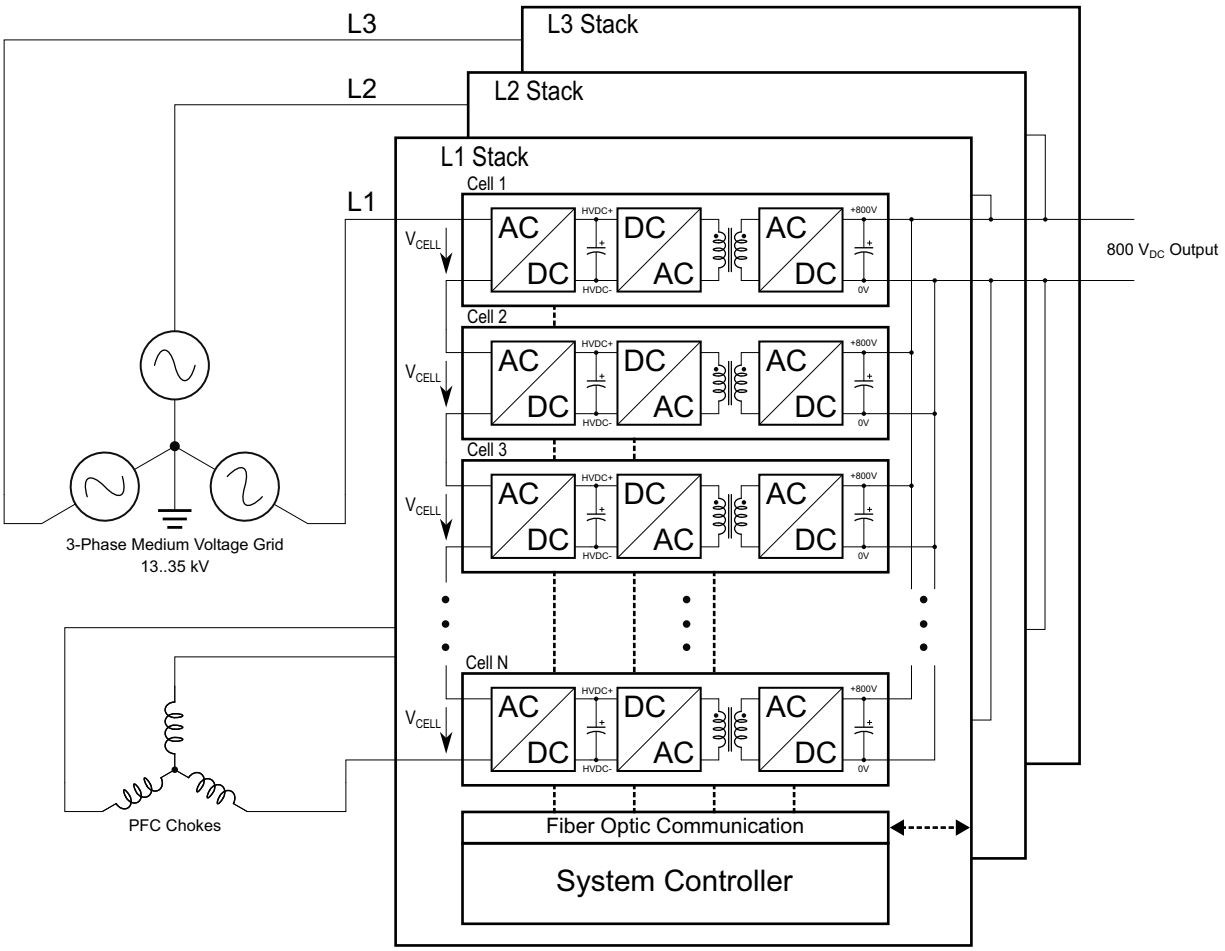

Figure 5. Medium-Voltage SST Block Diagram

However, even with this input-series distribution, when system voltages scale into the medium-voltage range (e.g., 13.5 kV to 35 kV) utilizing 2.3 kV or 3.3 kV Silicon Carbide (SiC) MOSFETs within each individual cell, the insulation coordination requirements under IEC 62368-1 and IEC 60747-17 can easily outgrow even the largest commercially available IC packages. At these extreme levels, relying solely on wider package clearances (such as 14 mm or 20 mm packages) becomes economically and logistically unfeasible, especially when high-altitude multiplication factors are applied. In these scenarios, power electronics designers must shift their focus from component-level compliance to system-level topological workarounds. Instead of trying to find a gate driver package that can withstand the entire 3.3 kV potential, the circuit topology itself can be redesigned to split and clamp the voltage stresses.

6.1. Split DC-Link Midpoint-Grounding Strategy

The easiest way to drive 3.3 kV SiC switches using highly cost-effective, standard V_{IOWM} = 1500 V rated isolated gate drivers is to establish a multi-level dc-link configuration with a grounded midpoint reference. By splitting a total 3 kV dc-link into two series-connected capacitor banks and choosing the midpoint of the capacitors as a reference ground, the isolated gate drivers only need to withstand a maximum continuous static voltage stress of 1500 V_{DC} instead of the full 3 kV_{DC} potential.

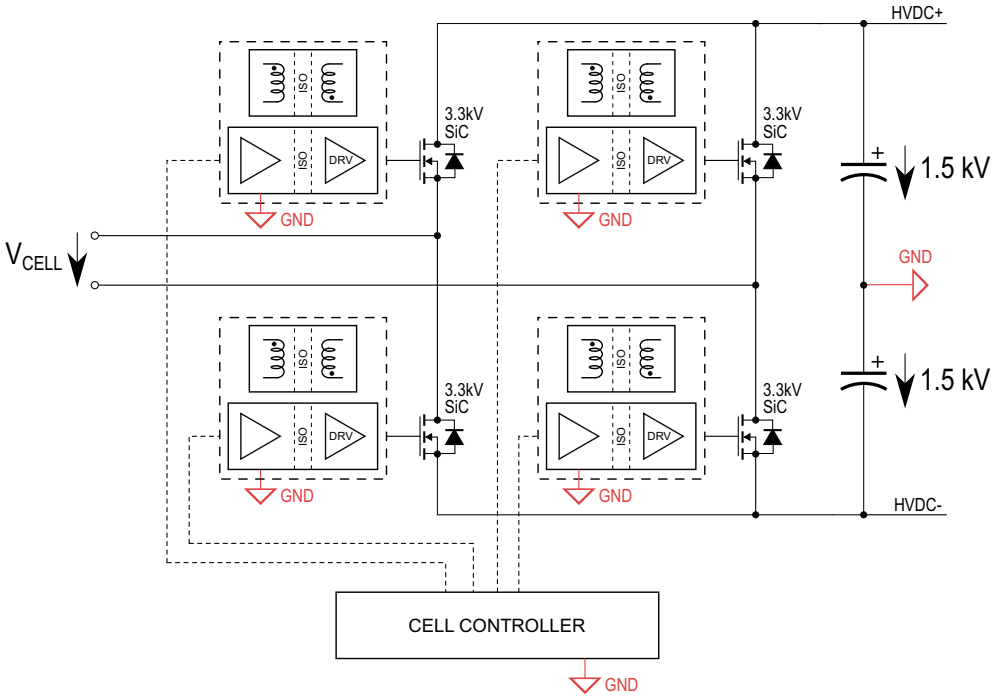

Figure 6. 1st AC/DC Stage of a SST Cell

Because the controller reference ground is tied directly to the high-voltage dc-link midpoint, the gate drivers within the cell do not need to provide safety-critical (basic or reinforced) insulation to the outside world. Instead, they only perform a functional insulation role, acting primarily as high-voltage level shifters to drive the upper and lower switches. Under safety standards like IEC 62368-1, the creepage and clearance requirements for functional insulation are significantly relaxed compared to reinforced limits. This drop in spacing demand ensures that standard, off-the-shelf, wide-body SOIC packages with typically >8.0 mm creepage can easily achieve compliance at 1500 V_{DC}.

Mandatory, safety-critical isolation, such as human touch protection or the galvanic separation between different cascaded SST cells, is decoupled from the gate drivers entirely. This high-voltage safety barrier is implemented externally using inherently immune fiber-optic links for all control and communication signals. By using optical fibers, the physical separation distance can be scaled arbitrarily, effectively enabling an infinite creepage path that assures complete galvanic separation where it actually matters.

This architectural change fundamentally shifts the insulation coordination parameters:

1. **Halved Working Voltage**
   The continuous working voltage across the isolation barrier of any gate driver referencing the midpoint is capped at 1500 V instead of the full 3 kV.
2. **Reduced Creepage Requirements**
   Under Table 4 of IEC 62368-1, dropping the continuous working voltage from 3 kV to 1500 V dramatically relaxes the required creepage. For a Material Group I driver package on a standard FR4 board with a slot, this brings the creepage spacing demand back down to <8.0 mm which can be accomplished easily by a standard Skyworks' wide-body SOIC gate driver.
3. **Standardizing the Gate Driver**
   Instead of sourcing exotic, low-volume 3.3 kV rated isolated gate drivers, designers can leverage mature, high-volume 1500 V digital isolators and gate drivers (such as our
   wide-body SOIC portfolios). This significantly lowers bill of materials (BOM) costs and improves supply chain security.

Design Considerations for Midpoint-Referenced Topologies

While this topological trick solves the creepage and clearance bottleneck, it introduces specific design challenges that must be addressed in the layout:

- **Midpoint Balancing**
  Any mismatch in supply currents or quiescent power consumption between the upper and lower gate drive circuits causes the midpoint potential to drift over time. Active or passive balancing circuits (like bleed resistors) must be integrated to compensate for this small current imbalance and ensure the voltage remains symmetrically clamped to 1500 V.
- **Common-Mode Transient Immunity (CMTI)**
  Although the static voltage stress is halved, the dv/dt slew rates of 3.3 kV SiC devices remain extremely high (often exceeding 100 V/ns. The chosen 1500 V isolated gate drivers must possess high CMTI ratings (typically 150 kV/µs) to prevent latch-up or CMTI-induced spurious switching.

7. Summary and Future Outlook

The main trend in Solid-State Transformer (SST) design is a push toward higher-voltage power devices to boost efficiency and reduce cell count. However, isolation technology for commercial gate drivers struggles to keep pace with these rapidly escalating voltage levels. Today, system designers effectively have two paths to bridge this gap:

1. **Topological Mitigation**
   Redesigning the power stage topology, such as using split dc-link, midpoint-grounded configurations to halve or distribute the isolation stress across gate drivers, enabling the use of proven, cost-effective WB SOIC packages today.
2. **Package-Level Scaling**
   Developing new, wider isolation footprints to natively sustain higher insulation requirements. To directly address this gap, Skyworks is currently developing a new ultra-wide-body (UWB) SOIC package designed to deliver significantly increased creepage and clearance distances for next-generation designs.

Until ultra-wide-body packages become commercially available, combining system-level topological workarounds with existing wide-body SOIC portfolios provides the most immediate and cost-effective path for medium-voltage SST designs.