AN766

UNDERSTANDING AND OPTIMIZING CLOCK BUFFER'S ADDITIVE JITTER PERFORMANCE

1. Introduction

This application note details the various contributions to a clock distribution's buffer's additive phase noise performance and how to optimize performance without increasing costs.

High speed communications requires system designers to optimize clocking performance while adhering to both performance and cost budget restraints. The optimal clock must be selected considering performance, cost, size, and output logic, to name a few; but the focus is on phase noise, for those who work in the frequency domain, or jitter which is the time domain equivalent. Often the reference clock needs to be distributed to a variety of logic inputs and locations on a PC board design which is accomplished by using a distribution buffer. The clock buffer now becomes part of the equation when determining the overall performance and while the clock noise is characterized as phase noise or jitter, the distribution buffer is characterized as additive phase jitter. This application note will show the dependence of additive jitter on i) input rise and fall time at a given amplitude, or slew rate ii) output format and iii) power supply voltage, and how to maximize clock buffer performance.

Engineers working on clocks understand the importance of power supply decoupling and signal integrity. What may get overlooked is that the input rise and fall time has a significant impact on additive phase jitter. While on first glance this is true, what makes the statement even more accurate is to consider both the amplitude versus rise and fall time, which is expressed as Volts/ns—or slew rate. Most engineers would associate slew rate with analog components, such as an op-amp, and it's uncommon to see a slew rate requirement in a digital component data sheet, and while we're still dealing with digital logic levels or inputs, it is just a more accurate way to describe what can really improve or degrade additive phase jitter. Take for example a differential LVDS signal which has a 350 mV single ended amplitude and a 400 ps rise and fall time measured at 20% and 80%, the differential slew rate would be (2 x 350 mV x 0.6) / (400 ps) or 1.05 V/ns. For the purpose of this application note only differential slew rate is used.

As an example shown in Table 1, note the additive jitter specification includes a description of slew rate, output frequency and output logic format as all have an effect on additive jitter.

Table 1. AC Characteristics

(V_{DD}=1.8 V±5%, 2.5 V±5%, or 3.3 V±10%, T_A=–40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall Time	T_R/T_F	LVPECL, LVDS, CML, HCSL, 20/80%			350	ps
		200 MHz, 50Ω, 20/80%, 2 pF load (LVCMOS)			750	ps
Minimum Input Pulse Width	T_W		500	—	—	ps
Additive Jitter (Differential Clock Input)	J	V_{DD}=2.5/3.3 V LVPECL/LVDS, F=725 MHz, 0.6 V/ns input slew rate	—	60	80	fs

A clock distribution IC does not generate a clock but rather regenerates and provides multiple copies. As such phase noise cannot be measured unless an input is applied and *total jitter* is measured — the clock buffer's contribution is referred to as *additive phase jitter*. In order to characterize the phase jitter contribution due to the buffer, the source is first measured, then the source plus DUT is measured and finally phase jitter is calculated by using Equation 1. This fair assumption often made is that the source and buffer noise are not correlated but are rather composed of purely random jitter. It’s also important to note the reference clock must have 3-10 dB lower phase noise than the DUT to accurately characterize the buffer.

$$J_{buffer} = \sqrt{(J_{Total}^2 - J_{source}^2)}$$

Equation 1. Clock Buffer Additive Jitter Formula

Note that when a clock buffer’s additive jitter and the source jitter number (which is typically given as an rms value) are provided, a root sum square value as shown in Equation 2 will be used to calculate total jitter.

$$J_{Total}^2 = J_{source}^2 + J_{buffer}^2$$

Equation 2. Total Jitter Formula

2. What Impacts Jitter Performance?

It is important to know what factors will have an impact on the jitter performance when adding a distribution buffer to a clock tree. This is also very important when reading data sheets, as how the supplier specifies their buffer’s jitter performance can greatly impact the number you see in the data sheet. For example, two buffers with similar performance may show very different additive jitter specifications, if one vendor used a much faster slew rate than the other.

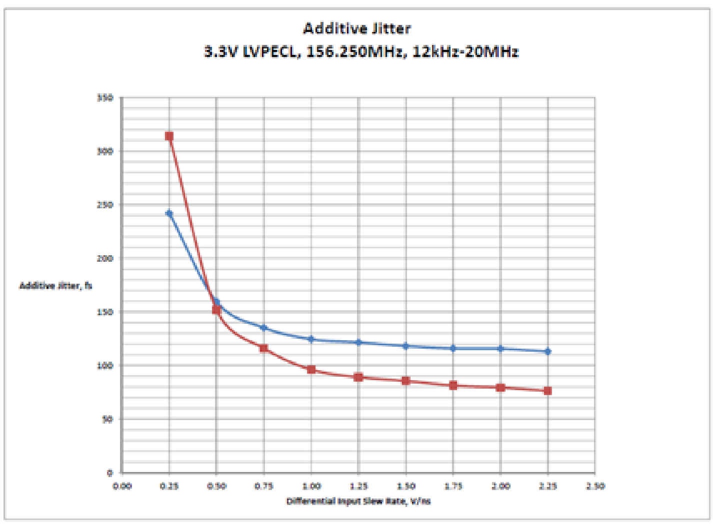

Figure 1. Additive Jitter vs Slew Rate for Two Different Buffer Families

Figure 1 shows the additive phase jitter versus input slew rate for two different clock buffers. In both cases the additive jitter decreases or improves as slew rate increases. What is interesting are the results shown in red can appear to be overall better. However, it’s actually more sensitive and quickly degrades at lower slew rates, such as a low frequency sine wave or CMOS clock. This graph highlights the importance of comparing additive phase jitter using the same slew rate values.

3. Integration Bandwidth

The integration bandwidth used for the jitter calculation also has a great impact on the measured jitter performance. The integration bandwidth of interest will depend upon the application. If in doubt, be sure to use the same bandwidth when making comparisons. The most common bandwidth used is 12 kHz to 20 MHz.

Figure 2 shows the additive phase jitter for an Si53301 using a 156.50 MHz input frequency and three integration ranges; 12 kHz to 20 MHz, 1.875 MHz to 20 MHz and 10 kHz to 1 MHz. This plot shows the optimal results will be achieved with 0.6 V/ns or faster slew rates.

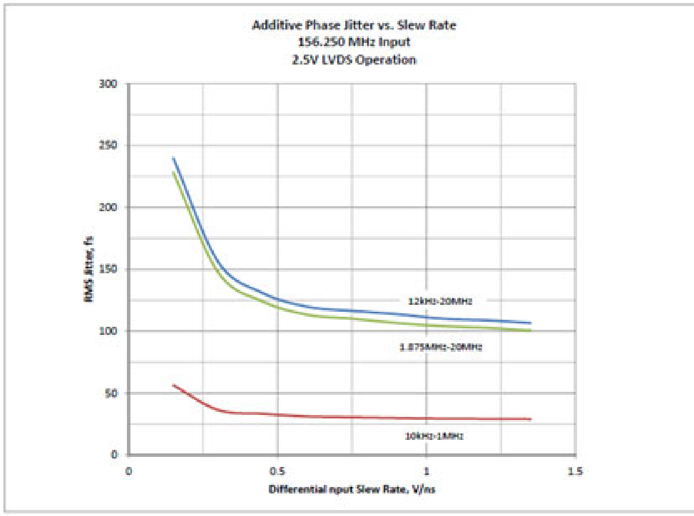

Figure 2. Additive Jitter vs Integration Band

4. Output Frequency

The frequency has a great deal of impact on additive jitter. Higher frequency will typically yield better additive jitter performance. If you know what frequency you will use, it is helpful to look at a data sheet specification that is close to your frequency of interest. Figure 3 shows the additive phase jitter for an Si53311 at three different output frequencies — the additive jitter will generally be lower at higher output frequencies by a factor of 20 log (f1/f2), or 6 dB for a doubling in frequency. While the integrated phase noise power is constant, phase jitter is lower since it's derived by (1/f) times the integrated phase noise.

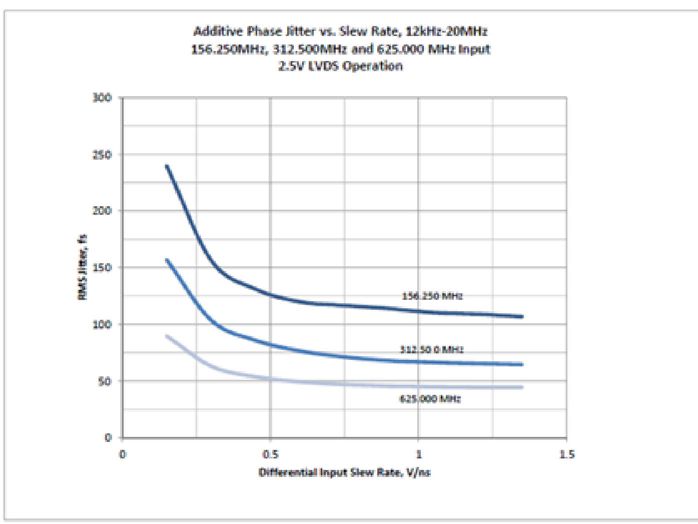

Figure 3. Additive Jitter vs Output Frequency

5. Logic Family

The output logic format can also have an impact on additive phase jitter performance. Skyworks Solutions Si533xx family is a versatile buffer with pin settable output logic formats including LVDS, LVPECL, HCSL, CML and CMOS. Figure 4 shows the various output logic families additive phase noise and phase noise sensitivity to slew rate compares. For this family an LVPECL output would be the best option for applications requiring the lowest additive phase noise performance. Due to this potential difference, it’s best to check the additive jitter phase noise for the output logic format being used.

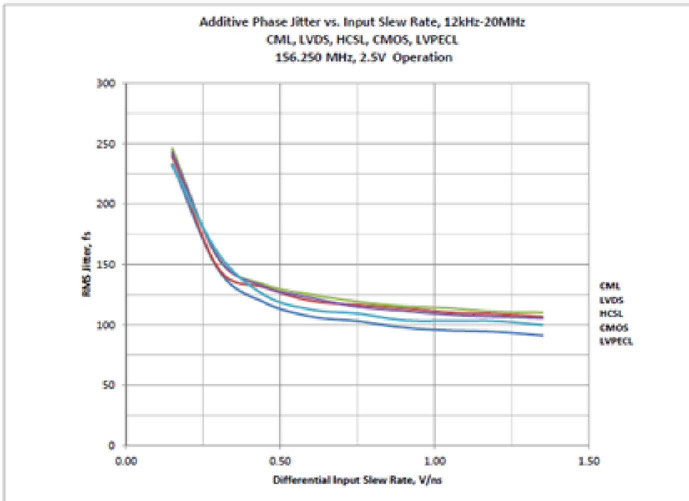

Figure 4. Additive Jitter vs Output Logic

6. Supply Voltage

Figure 5 compares the additive phase noise for the LVDS output logic family at 1.8 V, 2.5 V and 3.3 V operating voltage. Excluding the lower 0.3 V/ns slew rate, this plot shows identical performance, which means that any operating supply can be used to meet tight additive jitter budgets. However, there could be variations in additive jitter performance for another buffer family and is an important consideration in the design and selection.

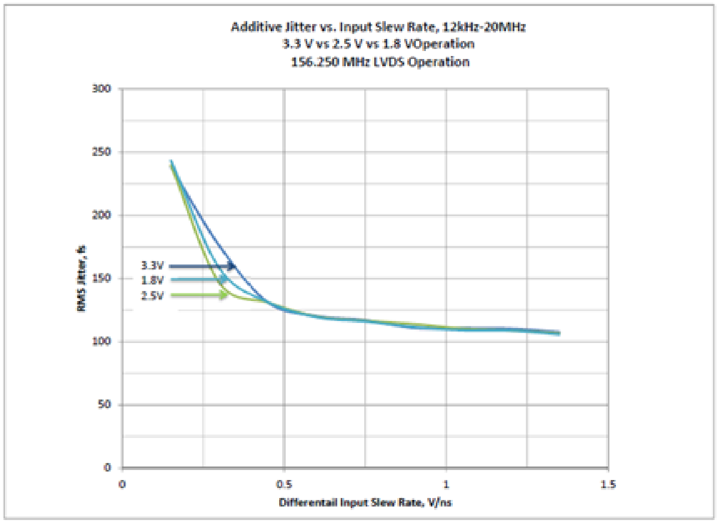

Figure 5. Additive Jitter vs Supply Voltage

Figures 1 through 5 show how phase noise performance can be optimized by increasing the input slew rate. A distribution buffer's input switches at voltage which would ideally be constant but in reality has a narrow window of variation. As such, the edge timing changes due to the variations in threshold resulting in jitter degradation; a faster input slew rate spends less time in this window of variation resulting in less of an impact. Figure 6 shows an exaggerated switching voltage window with 2 slew rates transitioning through it—as can be seen, the faster edge spends less time in a defined window which optimizes performance.

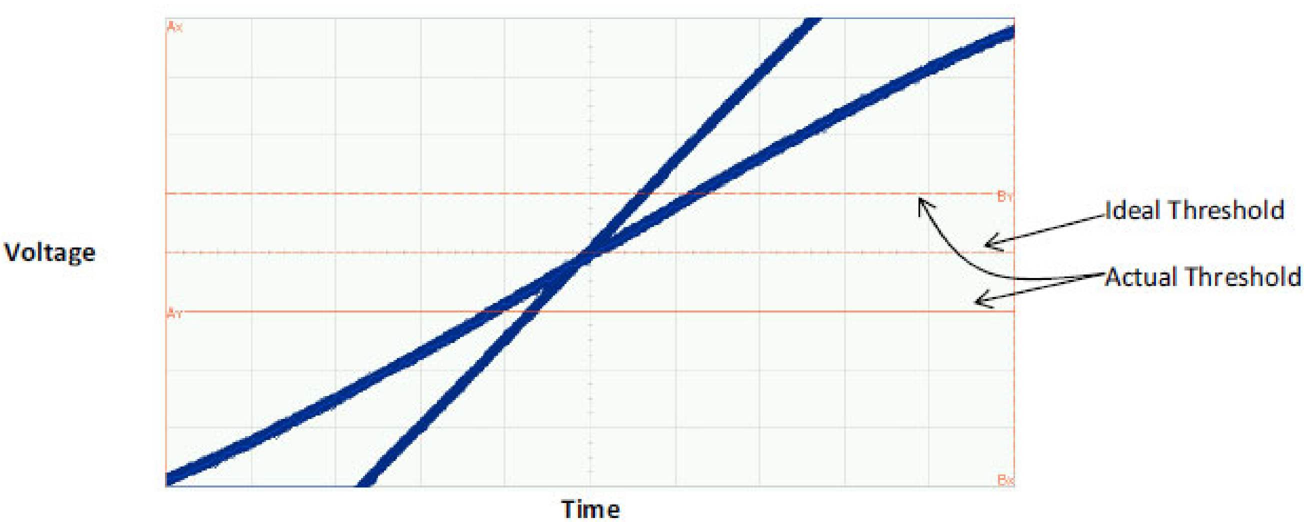

Figure 6. Slew Rate vs Decision Threshold

7. Conclusion and Recommendations

The Si53311 additive phase noise versus slew rate has been characterized by logic family, input frequency and power supply voltage. This is done to aid the designer evaluating overall jitter budget requirements and device selection. While the Si533xx family is less sensitive to variations in the input slew rate compared to other options available, optimal results will be achieved with slew rates greater than 0.6 V/ns. This is not a stringent requirement for most differential clock sources. Take for example a differential LVDS signal which has a minimum 250 mV single-ended amplitude and a maximum 400 ps rise and fall time at 20% and 80% of the amplitude, the differential slew rate would be (2 x 250mV x 0.6) / (400 ps) or 0.75 V/ns.

In order to maximize the Si533xx additive phase noise performance a 0.6 V/ns or higher input slew rate should be used but there is no significant improvement by using costly and power-hungry ultra-fast logic. Most differential clocks, even low output frequency options, will have sufficient slew rate. On the other hand, low frequency sine wave and perhaps CMOS clocks will have slew rate limitations which will potentially degrade overall phase noise and jitter if the edges are not sharpened up; otherwise a designer could spend needless hours chasing down suspected power supply noise, layout issues and other potential sources. In order to maximize the input slew rate it's best to locate the clock buffer driver as close to the source as possible, use a differential input which effectively doubles the slew rate — plus has the advantage of common mode noise rejection, maintain a full level input swing (do not attenuate the input unless maximum levels are exceeded) and optimize impedance matching as reflections will also degrade input slew rate.

Care must be exercised when evaluating clock distribution IC performance by data sheet specifications and when designing a buffer in a circuit as variations in slew rate, test methods and condition, will produce wide differences in performance. Careful consideration and design effort should be spent in order to optimize the input slew rate in addition to minimizing power supply noise and optimizing signal integrity when designing a distribution buffer into a clock tree.

NOTES: