AN1107: Si5332 Power Supply Noise Rejection

This application note explains Power Supply Noise Rejection (PSNR) and why it is an important consideration when designing systems with integral clock sources. PSNR measurement techniques and the superior PSNR capabilities of the Si5332 clock generator are explained.

Clock jitter performance is typically specified in clocking device data sheets under ideal power supply operating conditions. In real-world systems, power supply rails are not always clean and can contain significant noise due to switch mode power supplies and/or switching currents from other onboard circuits. The level of power supply noise that can be tolerated without significantly degrading output clock performance can vary from one device to another. Skyworks timing devices like the Si5332 are designed with internal power supply noise rejection circuits to combat the performance-degrading effects of excessive power supply noise.

KEY POINTS

- Device power supply noise rejection
- PSNR Measurement method
- Switch mode power supplies
- Simple VDD bypass/filtering

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1. Why is Power Supply Noise Important and How Does the Si5332 Address It?

Clocking devices are mixed signal devices in which many of the critical device circuits are necessarily implemented using analog circuitry, which can be more susceptible to the effects of power supply noise than strictly digital circuits. For example, reference clock and crystal oscillator inputs have switching thresholds. Noise on the power supplies of these circuits will cause threshold switching errors, which translates into added noise-induced jitter on these reference inputs. Power supply noise on PLL circuits can induce similar effects which can manifest as random jitter or spurs on the PLL output. These power supply noise effects will ultimately appear on the outputs as unwanted additional jitter, but this can be minimized if the device circuitry is designed to specifically attenuate or filter out the power supply noise. This is the case with the Si5332.

The Si5332 is specifically designed with added circuitry to mitigate the performance degrading effects of power supply noise. This is done by using multiple internal and independent voltage regulator circuits on the power supplies of each critical stage of the device. Separate independent internal voltage regulation circuits are provided on the clock input buffers, the oscillator circuits, the PLL, the internal dividers, and the internal digital circuits. These regulators provide isolation from external power supply noise *and* internal power supply noise isolation between functional blocks within the device. This approach to filtering both external and internal PS noise provides significantly improved device PSNR performance as compared to many competing devices, resulting in consistent jitter performance over a wide range of power supply noise profiles. For more information on PSNR testing and PS noise effects, please see "AN491: Power Supply Rejection for Low-Jitter Clocks".

2. Test Setup for Si5332 PSNR Measurements

The figure below shows the test setup for PSNR measurement. An AWG (Arbitrary Waveform Generator) was used to control the noise amplitude and noise frequency. This noise was coupled into the DUT through a bias-tee arrangement. The output of the setup with AWG off is first measured, and this becomes the zero-noise baseline performance. Then, with AWG on, the effect of injected PS noise on total output jitter was measured, including the peak amplitude of the PS noise output spur using an E5052B signal source analyzer. The resulting data becomes the effective PSNR profile of the device and is presented in 3. Si5332 PSNR Performance.

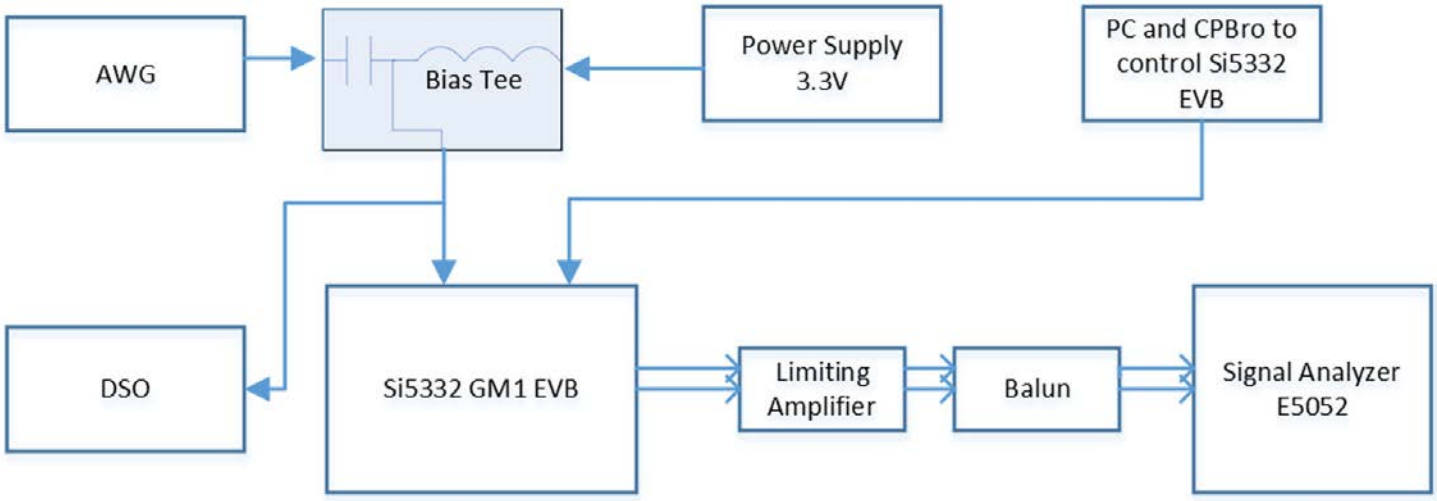

Figure 2.1. PSNR Test Setup Block Diagram

3. Si5332 PSNR Performance

Si5332 PSNR performance, based on an injected 100 mVpp sine wave onto the power supply, is shown in the table and graph below. The spur level is the peak dBc level of the spur appearing in the output clock spectrum due to the injected power supply sine wave "noise". The RMS jitter is the total 12 kHz to 20 MHz RMS jitter of the output including the injected power supply spur. The graph below shows the total RMS output jitter in blue, and peak output spur amplitude in dark orange.

Table 3.1. Total Output Jitter and Peak Spur Power with Power Supply Noise

Output Clock = 156.25 MHz, LVDS 3.3 V, 190.1 fs RMS without Noise			
Sinewave "PS Noise" Frequency (KHz)	Sinewave "PS Noise" Amplitude (mVpp)	Spur Power (dBc)	Output Jitter 12k–20M (fs RMS)
25	100	–105	190.8
50	100	–102	191.4
100	100	–87	201.3
250	100	–108	190.7
500	100	–88	198.9
1000	100	–96	192.0
2000	100	–94	193.3
3000	100	–98	191.2

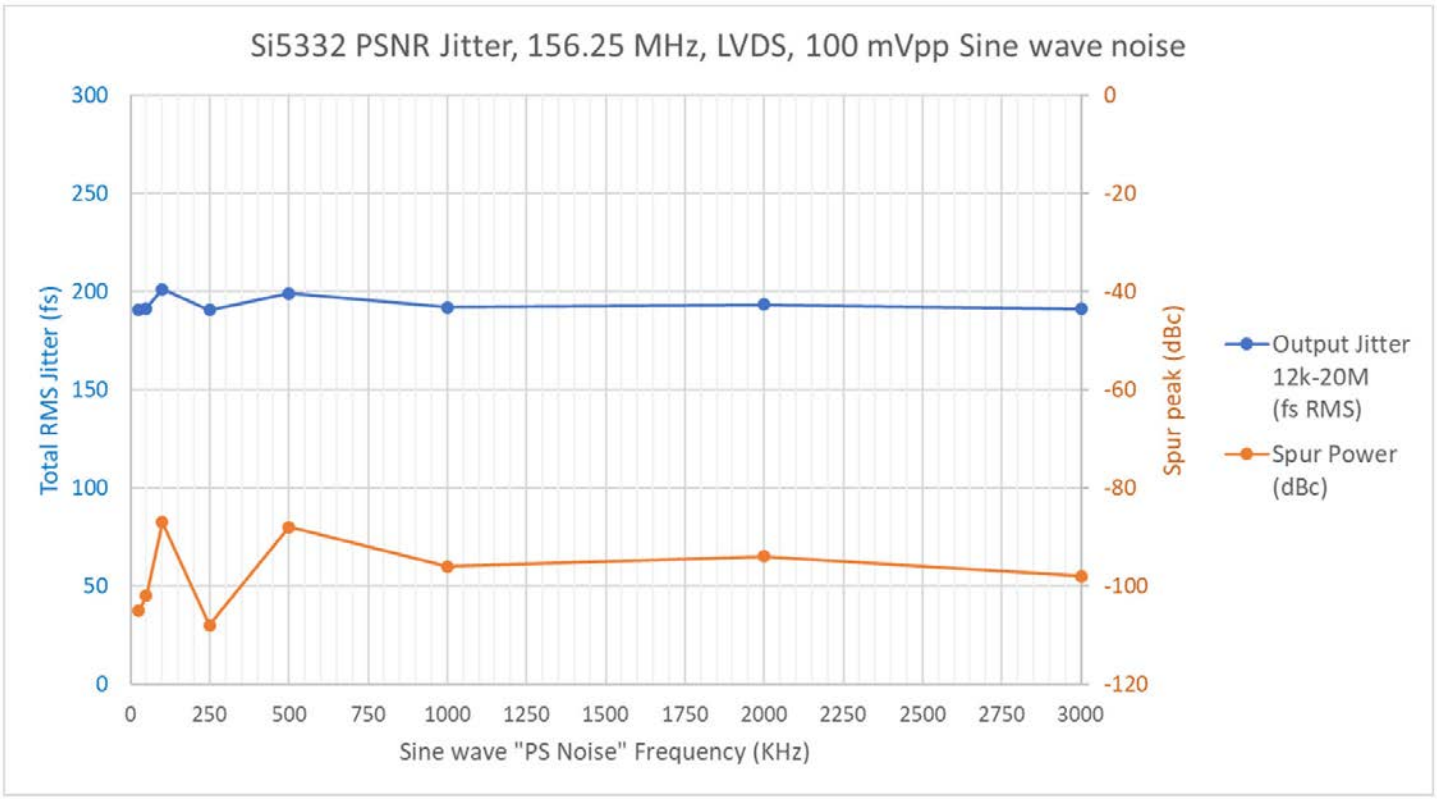

Figure 3.1. Total Output Jitter and Peak Spur Power with Power Supply Noise

4. Conclusion

For power supply noise amplitudes of 100 mVpp or less, the Si5332 PSNR capabilities are excellent over a wide band of potential power supply noise frequencies, including switching frequencies used by most switching power supplies and switching regulators.

Given the excellent PSNR performance of the Si5332, the power supply filtering recommended for most applications are simply a single 0.1 µF and 1 µF, decoupling capacitor on each VDD node (of course, as close to the device VDD node as possible). Use of additional filtering components, such as inductors and/or ferrite beads is only required for very noisy environments or applications requiring extremely low-noise clocks.

As can be seen from the data shown, the Si5332 provides excellent PSNR performance. Since real-world power supply rails are not perfect and noise-free, the ability to get consistent jitter performance in the presence of power supply noise is very valuable and translates into reduced system BERs and increased system operational reliability.

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