AN1110: Si5332 Spread Spectrum and Other EMI Reduction Techniques

Virtually all electronic systems must pass through the gauntlet of EMI/EMC compliance testing. Digital systems tend be the most stubborn in achieving EMI compliance due to the varied frequencies and wide spectrum of harmonics that is characteristic of digital signals. Problematic EMI/RFI frequencies are typically harmonically related to the basic system clocks. Therefore, in many cases, system EMI can be mitigated by using simple EMI reduction techniques in the system clock source. This application note will describe three common EMI mitigation techniques, listed below, which can be employed as part of an EMI mitigation strategy when designing with the Si5332 clock generator.

1. Differential signaling
2. Slew rate control
3. Spread Spectrum Clocking (SSC)

In addition to commercial limits set by the FCC and EU, automotive markets have more stringent requirements. For automotive applications, Skyworks recommends the use of the AEC-Q100 qualified Si5332-AM option. Additional design guidelines and emissions mitigation techniques specific to automotive electronics design are outlined in a companion application note: "AN1237: Si5332 Design Guidelines for Minimizing EMI".

KEY FEATURES OR KEY POINTS

- Electro Magnetic Interference (EMI) reduction
- Electro Magnetic Compatibility (EMC)
- Radio Frequency Interference (RFI) reduction
- Spread Spectrum Clocking (SSC)
- Slew rate control for Si5332 CMOS drivers
- Differential signaling

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1. Differential Signaling

Differential signaling is a powerful method for reducing EMI and RFI in clock signals due to EM field cancellation inherent to balanced differential signals versus using the more common single trace or single-ended (SE) signal. For many applications, use of differential clocks can be a major EMI advantage. The figure below compares the EMI of the fundamental frequency of a 100 MHz clock for both single-ended (left side) and differential clock signal (right side). Notice the marked reduction in peak radiated energy for a differential clock versus single-ended clock at the same frequency.

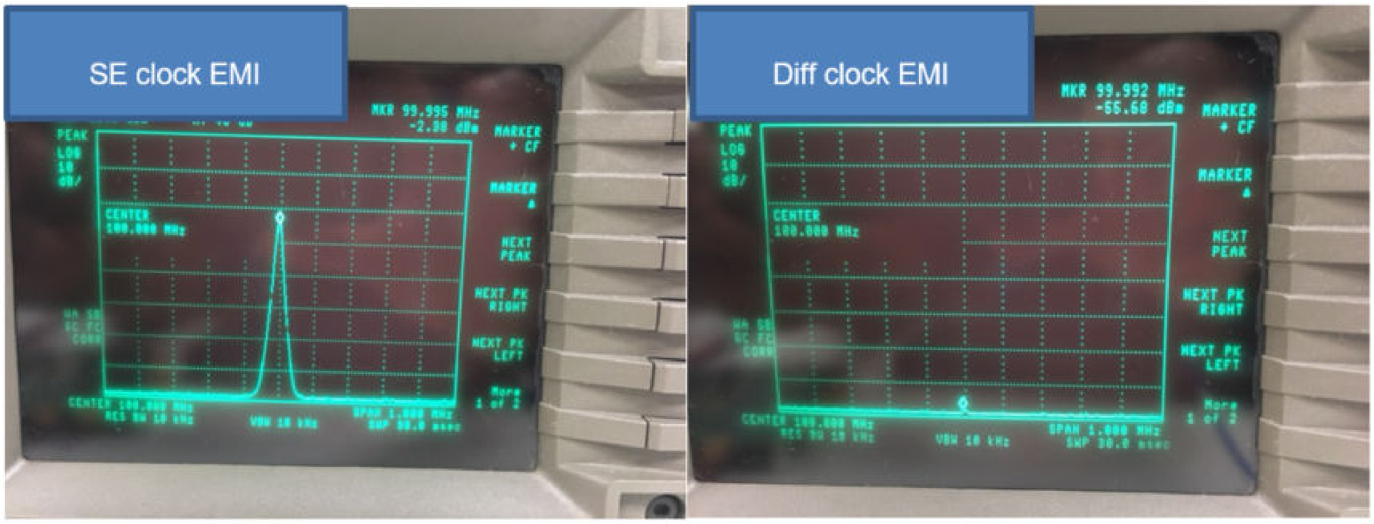

Figure 1.1. EMI Single-ended (SE) Clock vs Differential (Diff) Clock

Wideband EMI is sometimes referred to as Radio Frequency Interference or RFI. One source of wideband RFI can be the harmonics of non-sinusoidal square wave signals, including clocks. Fast rising/falling edges of digital signals are rich with harmonic content. The field canceling effects of using differential clocks will help in reducing wideband harmonic content as well as fundamental frequency energy. The figure below compares the radio frequency interference (RFI) in the 800 MHz – 1 GHz band for the same 100 MHz clock shown in the figure above and shows the potential for RFI improvements when using differential clocks. Single-ended signal harmonic RFI is on left side and differential signal harmonic RFI content on right. Notice the marked RFI improvement when using differential signals.

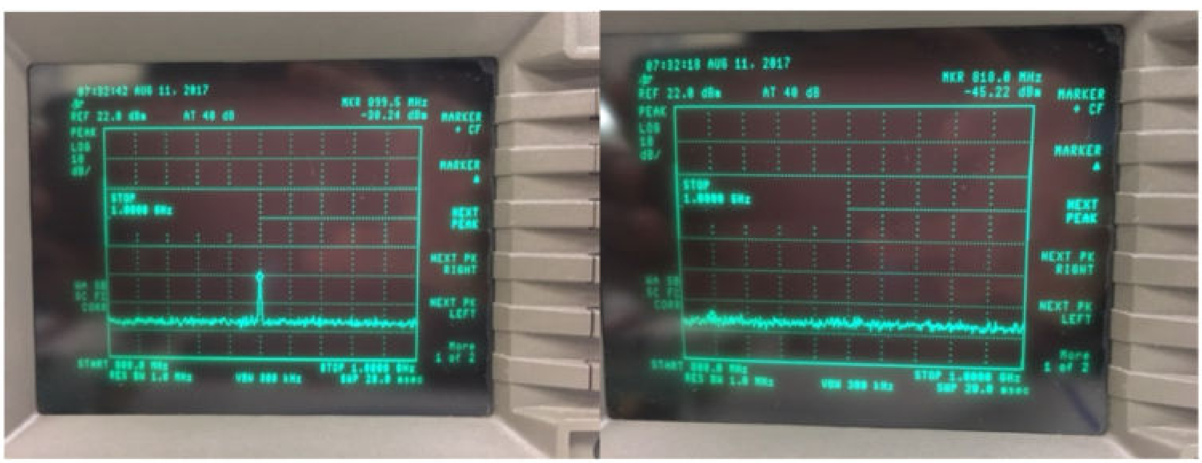

Figure 1.2. RFI Single-ended (SE) Clock vs Differential (Diff) Clock

Figures 1.1 and 1.2 illustrate the potential for dramatic EMI/RFI improvements when using differential clocks versus single-ended clocks.

2. Slew Rate Control for CMOS Clocks

CMOS clocks present a unique EMI/RFI challenge due to their single-ended nature, which is not typically compatible with differential techniques. (However, it is possible to use differential CMOS clocks in some singled-ended applications. For more details on differential CMOS clocks for EMI reduction in single-ended clock applications, see application note, "AN1237: Si5332 Design Guidelines for Minimizing EMI"). For CMOS single-ended signals, an alternative method available in the Si5332 for RFI reduction is edge slew rate control. This EMI/RFI reduction technique is especially applicable to cost sensitive and consumer electronic applications.

The Si5332 has the capability to provide four levels of CMOS slew rate control per output driver. The waveform edge detail shown in the figure below illustrates the four levels of slew rate control. (Refer to the Si5332 Family Reference Manual for details on register settings for CMOS output slew rate control.) The benefit of slowing the rising/falling edges is a reduction of RFI **harmonic** content. Slew rate reductions will only reduce the **harmonic** content of the signal and does not substantially change the **fundamental** frequency energy.

Figure 2.1. CMOS Slew Rate Control in Si5332

The following table shows both the fundamental mode power (EMI) and the harmonic power (RFI in 800 MHz – 1 GHz range) for each of the four slew rate settings shown in the figure above. Notice how slew rate reductions can dramatically reduce the **harmonic** RFI content while barely affecting the fundamental mode (EMI). Of course, any slew rate reductions must be weighed against the system impact of the slew rate change. But in many cases, a slower slew rate will have minimal operational system impact while providing good RFI improvements.

Slew Rate Setting	EMI (dBm)	RFI (dBm)
Fast	10.75	-25
Slow	10.73	-32
Slower	10.5	-37
Slowest	10.4	-39

3. Spread Spectrum Clocking (for EMI Reduction)

Spread spectrum clocking (SSC), which is “low frequency modulation” of a clock, is a very powerful tool for reducing both EMI and RFI. SSC works by spreading out the energy over the modulation frequency range, thus lowering the absolute peak energy. This low frequency modulation is typically in the range of 30-33 kHz. Spread spectrum clocking can significantly reduce EMI/RFI without requiring costly and time-consuming board or system level modifications. The Si5332 can support SSC using a center spread or down spread modulation profile including PCI Express (PCIe)-compliant SSC modulation. The figure below shows EMI before applying SSC (left) and after applying SSC (right) for a 100 MHz PCIe reference clock generated using the Si5332. Notice the spectral peak has been replaced with a lower level “spread out” plateau.

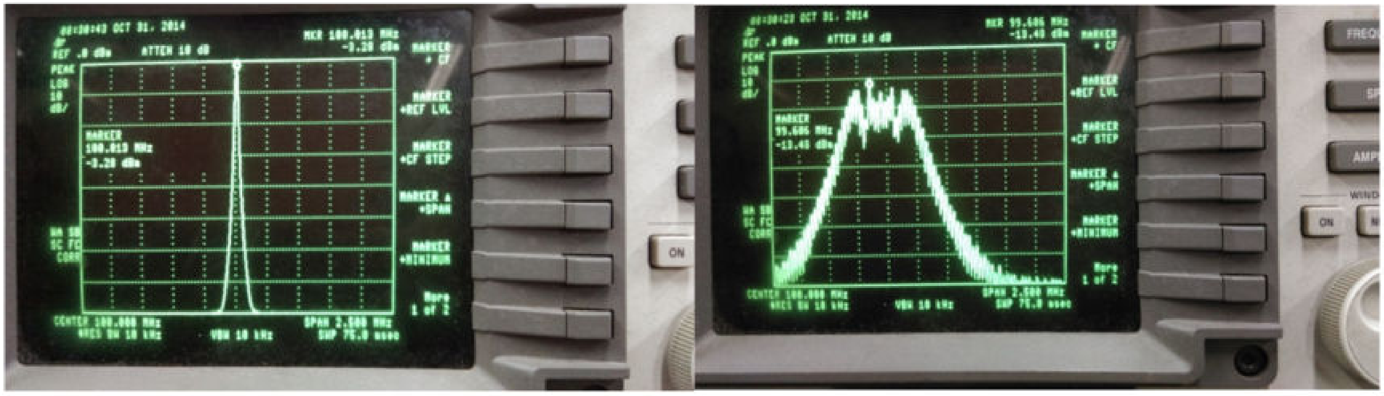

Figure 3.1. EMI Reduction due to -0.5% Down Spread on a 100 MHz Clock Used for PCIE Applications

Configuring a device for spread spectrum is easily done within ClockBuilderPro (CBPro). For the Si5332, SSC is implemented using the Si5332’s Multisynth dividers (N dividers in CBPro). The Si5332 has two N dividers, so the Si5332 can support up to two SSC clock domains. There are two steps within the CBPro configuration creation process specific to configuration of SSC. The first step is when defining output clocks. Any clocks requiring SSC must be explicitly assigned to an available N divider, as shown below.

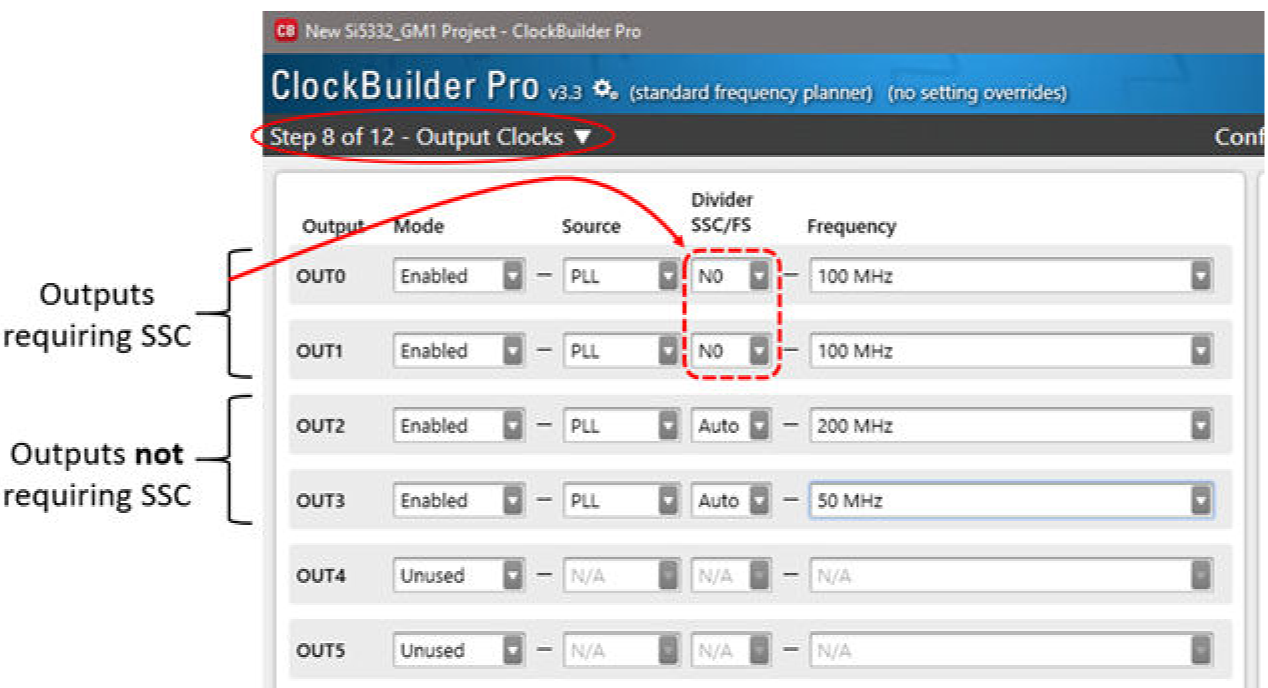

Figure 3.2. Assigning N Dividers for SSC Configuration in CBPro

The second step (shown below) is to set the SSC modulation parameters for those outputs defined as shown above.

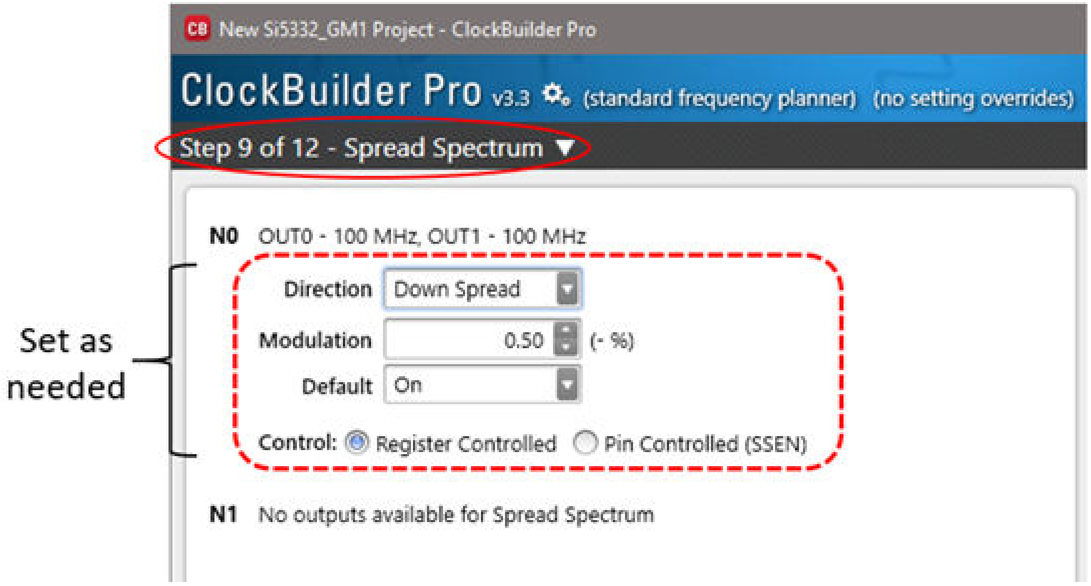

Figure 3.3. Configuring SSC Modulation Parameters in CBPro

Once SSC is configured, continue with any remaining steps in the full device configuration process.

It is recommended to always use CBPro to configure SSC for the Si5332 as this works for over 99.9% of typical SSC configuration requirements. But, if for some reason you require the device register details for configuration of SSC, refer to the Si5332 Family Reference Manual for those details. This document is available on our web site.

4. Conclusion

The Si5332 is a high-performance and versatile clock generator with support for multiple EMI/RFI reduction techniques. The EMI/RFI reduction techniques described in this application note are 1) Use of differential clocks, 2) Variable slew rate adjustment, and 3) Spread spectrum modulation. These techniques can be used independently or combined to give varying levels of EMI/RFI reduction to meet system EMI/RFI goals. While the use of differential clocks is typically an initial design decision, both the slew rate adjustment and spread spectrum modulation can be planned for, and then later enabled only if EMI/EMC compliance results require it. This gives the flexibility of having EMI/RFI reduction techniques available to bring to bear on EMI/EMC compliance issues without necessitating costly or time-consuming redesigns. In closing, careful use of the EMI/RFI reduction techniques described in this application note can potentially shorten the path towards successfully meeting required EMI/EMC regulatory compliance.

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