AN1228: FET Selection Guide for Si347x PSE Families

The Si347x family of Power over Ethernet PSE devices, including the Si3471, Si3472, Si3473, and Si3474, utilizes external FETs to improve thermal performance.

To meet the strict timing requirements demanded by the IEEE 802.3af, 802.3at, and 802.3bt standards, external FETs must meet certain requirements. This application note details the key parameters needed when selecting an external FET and lists the FETs Skyworks has tested with the Si347x family of devices.

For more information on choosing a FET or to review a specific FET, please contact us at www.skyworksinc.com/support.

KEY TOPICS

- Compatible FETs
- Important FET parameters
- Safety considerations

1. FET Parameters and Tested FETs

The table below summarizes the key FET parameters and the target values for compatibility with the Si347x families. It lists the FETs Skyworks has tested to be compatible with the Si347x families. Refer to the data sheets of each FET for the latest specifications.

Drain-source resistance RDS(ON) is a key parameter to ensure thermal performance, particularly in high port count designs. Designs using FETs with a high RDS(ON) and a poor layout may experience thermal issues. Refer to the Si347x EVBs for recommended PCB layout to ensure proper thermal dissipation. In addition, please submit design schematics and layouts for a free, confidential review by visiting www.skyworksinc.com/support.

Table 1.1. FETs Tested with the Si347x Families and Key Parameters

Parameter	Total Gate Charge Q_g	Gate-Drain Charge Q_{gd}	Drain-Source Breakdown Voltage $V_{(BR)DSS}$	Drain-Source On-Resistance $R_{DS(ON)}$ at V_{GS} = 10 V	Safe Operating Area
Target	≤ 30 nC	≤ 11 nC	>100 V	<120 mΩ	See Table 1.2
Fairchild FDMC3612	14.4	3.7	100	110	See Figure 1.1
Infineon IRFHM3911	17	5.4	100	115	See Figure 1.2
Nexperia PSMN075	16.4	5.2	100	71	See Figure 1.3
Nexperia PSMN040-100MSE	30	10.7	100	36.6	See Figure 1.4
Toshiba SSM6K361NU	3.2	1.5	100	69	See Figure 1.5

All FETs have power limitations ($P_{FET} = V_{DS} * I_D$). Use above these limits will damage the FET after a certain amount of time. The Safe Operating Area (SOA) curve represents the V_{DS}/I_D limitations for a given FET. The IEEE 802.3bt standard specifies the amount of time a PD is allowed to draw current above its assigned class. Care must be taken to select a FET with an SOA curve that can withstand the Si347x's implementation of the IEEE 802.3bt standard. These parameters are listed in the table below. The Si347x family of PSEs are always Type 3 or Type 4 and follow the current limit based on PD class.

Table 1.2. Si347x Overcurrent Time and Current Limiting Per Pair Set

PD Class	Si347x Maximum Overcurrent Time	Si347x Current Limit Per Pair Set	Drain to Source Voltage	SOA Curve Point
0, 1, 2, 3	15 ms	425 mA	30 V	Point 1
4, 5, 6, 7, 8	9 ms	1275 mA	15 V	Point 2

The following figures show example SOA curves with the IEEE current limits for classes 0-3 identified as Point 1, and the IEEE current limits for classes 4-8 identified as Point 2.

For a FET to be usable, it must be able to operate on the points indicated on the SOA curves for a time greater than the associated Si347x Maximum Overcurrent Time defined in Table 1.2 Si347x Overcurrent Time and Current Limiting Per Pair Set on page 2. If the FET is not capable of operating for this amount of time at the given points, there is a risk of thermal damage if an overcurrent event occurs.

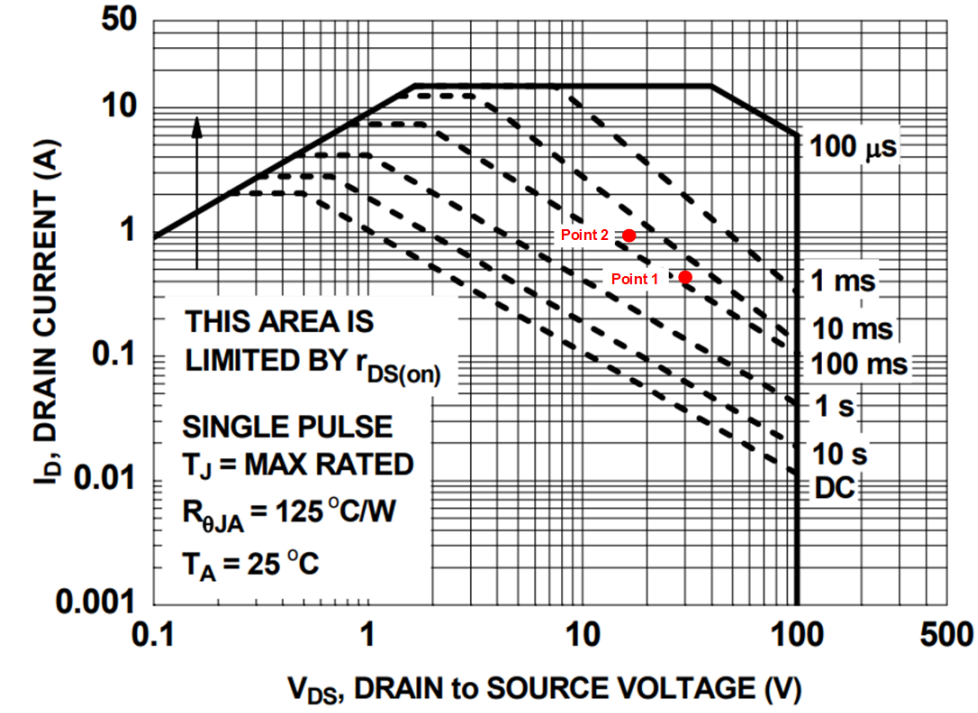

Figure 1.1. FDMC3612 FET SOA Curves with Worst-Case Points Highlighted

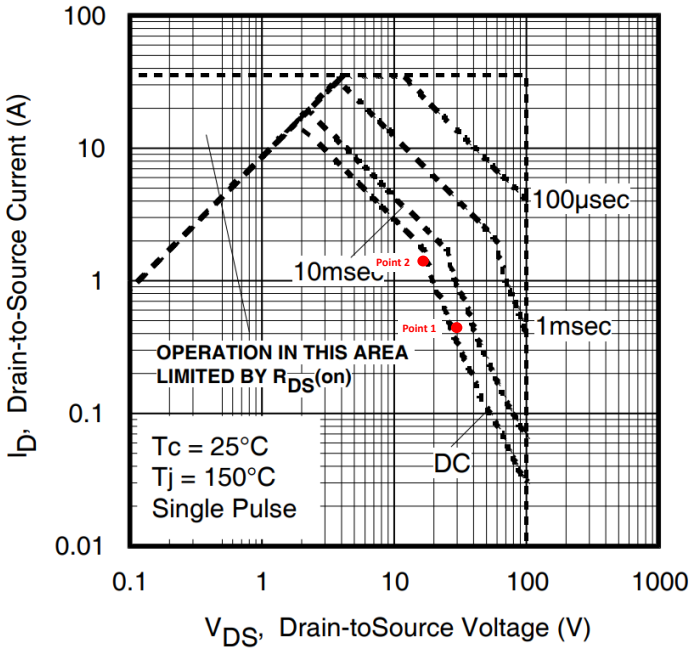

Figure 1.2. IRFHM3911PbF FET SOA Curves with Worst-Case Points Highlighted

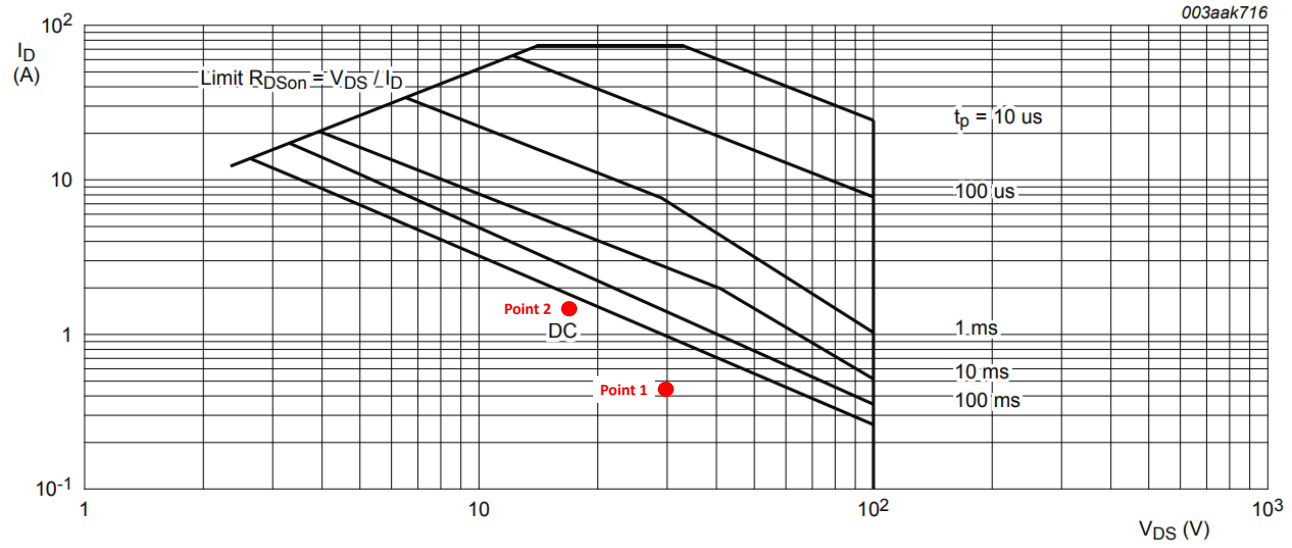

Figure 1.3. PSMN075-100MSE FET SOA Curves with Worst-Case Points Highlighted

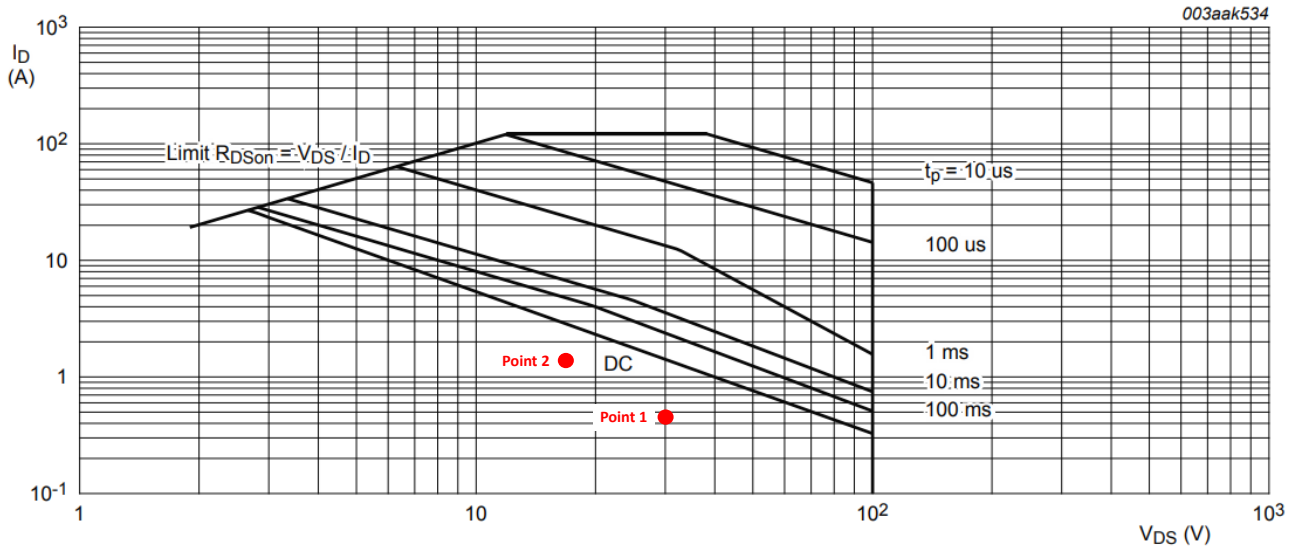

Figure 1.4. PSMN040-100MSE FET SOA Curves with Worst-Case Points Highlighted

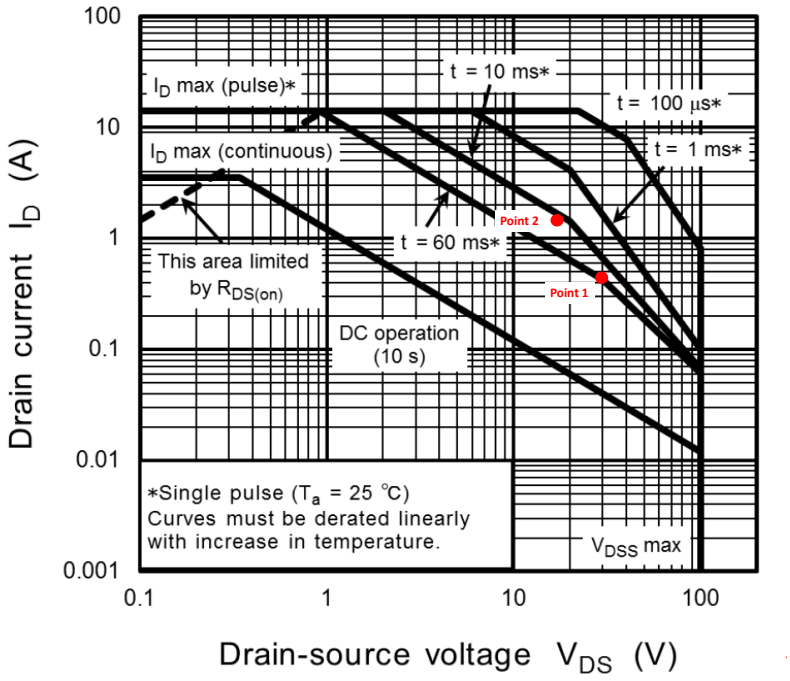

Figure 1.5. SSM6K361NU FET SOA Curves with Worst-Case Points Highlighted

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