APPLICATION NOTE

AN1359: Design Considerations for the Si86Sx Family

Description

This application note describes the Si86Sx family of digital isolators and key factors in transitioning from the Si86xx family of digital isolators.

Typical applications include:

- Industrial automation
- Motor control and drives
- Power supplies, inverters/UPS
- Battery Management System (BMS)
- Solar inverters
- Electric vehicles

Key Points

- Si86Sx and Si86xx comparison
- Bipolar surge voltage: >10 kV
- CMTI Transient Immunity: >100 kV/µs
- Channels deglitch filter: 30 ns
- CMOS threshold inputs
- Low power mode

1. Si86Sx Family Description

The Si86Sx are a new family of robust, high performance, lower power digital isolators offering substantial data rate, propagation delay, power consumption, size, reliability, and external BOM advantages over Si86xx family. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance.

The Si86Sx family provides up to 6 isolation channels with different forward and reverse channel combinations. As Si86xx, the Si86Sx data rates up to 150 Mbps are supported, and most of the options achieve typical propagation delays of less than 10 ns.

Compared with the legacy Si86xx family, the Si86Sx family provides a higher isolation barrier working voltage, which is certified to the latest IEC 60747-17 reinforced specification and can be safely used in higher power applications like inverters and motor drives. The enhanced isolation barrier can extend end-user product lifetime. The lifetime is guaranteed by proof testing and TDDB (Time Dependent Dielectric Breakdown) assessments required by IEC 60747-17. To achieve reinforced rating per IEC 60747-17, a 10 kV peak bipolar surge proof test is required instead of the less stringent 10 kV unipolar surge for the previous VDE 0844-10/-11 standards, which are now supplanted by IEC 60747-17.

The Si86Sx family integrates many noise immunity features in its signal channels for noisy environment applications to enhance end-user system robustness. These enhancements include Schmitt trigger CMOS input interfaces, 30 ns deglitch filters, >100 kV/µs CMTI (Common-Mode Transient Immunity) isolation barrier performance. The anti-noise features are a good fit for industrial automation, motor control and drivers, and power supplies.

The Si86Sx family supports a wide range of features and options for different applications, which include low power mode, sleep mode, inverting output, non-inverting output, SPI and I^2C options. The low power mode (Si86SLx) and sleep mode (Si86SMx) are useful for power critical applications like battery management system and electric vehicle applications. The inverting output option is designed to match optocoupler operation and save inverting logic gates for optocoupler replacements and the applications where a NOT logic gate is needed. The SPI device (Si86SSx) integrates four forward channels for reset signal, SPI chip selection, clock and MOSI signals, and one tri-state channel for MISO signal which allows multiple SPI secondary devices to be directly connected to a host controller. The non-inverting standard and I^2C Si86Sx isolators are pin-to-pin compatible with the legacy Si86xx family. Their improved performance stated above are very attractive for upgrading legacy Si86xx for better lifetime reliability and robustness.

The Si86Sx family provides RoHS-compliant package options, wide body SOIC-16, narrow body SOIC-16 and SOIC-8, wide body stretched SOIC-8, and QSOP-16. For more information concerning the Si86Sx family, refer to the relevant product data sheet from the Skyworks Digital Isolators page.

1.1. Standard Si86S6x for Legacy Si86xx Upgrade

Skyworks legacy Si86xx digital Isolators have been widely used in different markets like automotive, industrial, power supply and telecom for over 10 years. The Si86xx family has 1 to 6 channel options with a full combination of forward and reverse channels in a variety of packages. The new standard Si86Sx isolators with non-inverting output and/or I^2C bidirectional channel have pin-to-pin compatible options with legacy Si86xx family for drop-in replacement and performance enhancement.

1.2. Low Power Mode Si86SLx

Assembled in the same packages and having the same pinouts as found in the Si86S64x, the Si86SLx product options are optimized for lower-power operation rather than more precise timing performance. On a per-channel basis, the Si86SL4x uses 0.25 mA less supply current than the Si86S64x at the expense of slightly degraded timing characteristics and transient immunity. The quiescent current is reduced to 0.7 mA per channel and the active current is ~1 mA per channel at 1 Mbps data rate.

The low power mode is always on.

1.3. Sleep Mode Si86SMx

For applications that do not require continuous operation, the Si86SMx products have a sleep mode to reduce power consumption without compromising on operational performance. Unlike the low power mode Si86SLx, the Si86SMx has the same data rate, channel timing characteristics and transient immunity performance as standard Si86Sx.

Driving the SMB input low will put the Si86SMx into sleep mode. The sleep mode signal is transmitted to the isolated side on its own dedicated always active channel. When the isolated side receives the sleep signal, the isolated side is put into a low power state and tri-states its outputs. In this state, IDD1 draws approximately 0.75 mA and IDD2 draws approximately 1.1 mA

During the sleep state, the Si86SMx disables outputs and leaves just enough circuitry active to monitor the state of the SMB input. To return to full operational state, the SMB pin is driven high and the isolated side wakes up in approximately 1.5µs, which is listed as tWU (SMB to Wake-Up from Sleep Mode) in the Si86Sx data sheet.

When the device is in active mode, it works as a standard Si86Sx device.

1.4. SPI Mode Si86SS51

The Si86SS51 digital isolators have four channels that are specifically designed for isolated SPI bus applications. These devices have three forward channels for SPI which are chip select (MCSB and SCSB), SPI clock (MCLK and SCLK) and SPI MOSI (MO and SI) respectively and another reverse channel for SPI MISO (MI and SO). The MISO output or the MI pin on the non-isolated (or main controller) side is tri-stated for SPI bus sharing and is controlled by the SPI chip select, or the MCSB pin.

A typical connection diagram is shown in Figure 1.

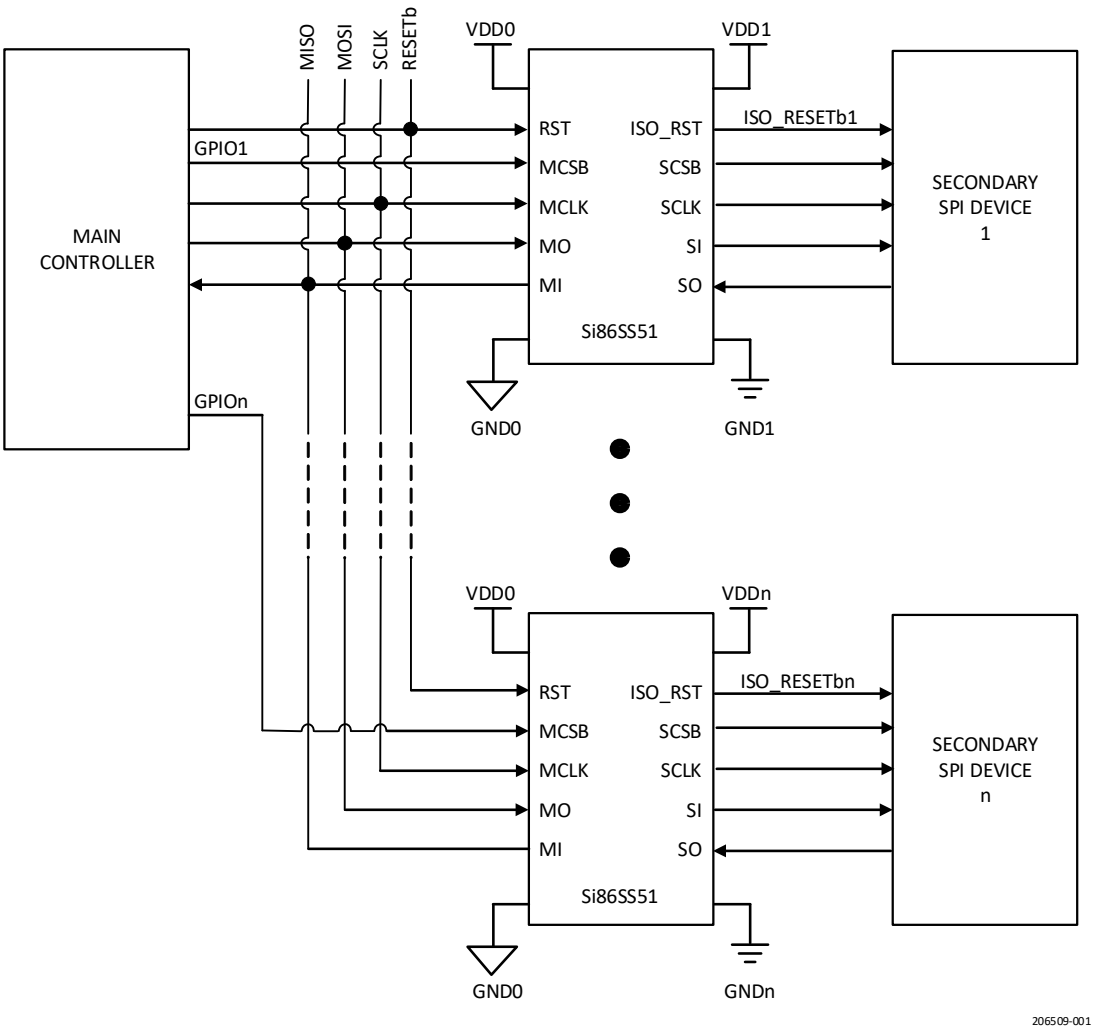

Figure 1. Isolating SPI with Si86SS51

In an isolated SPI transaction, the normal SPI clock signal with ~50% duty cycle generated by the main controller travels to the isolated secondary through a galvanic isolation barrier (digital isolator Si86SS51). Both the main controller and the isolated secondaries use the falling edge of SPI clock signal to transmit data and the leading edge to receive data. In an isolated SPI write transaction, all SPI signals will travel through the same type of isolation barrier exactly once. The result is that channel propagation delays (t_{PHL} and t_{PLH}) become less important, and channel pulse width distortion (PWD) and channel-to-channel skew (t_{PSK}) are crucial. In an isolated SPI read transaction, the secondary uses the falling edge of the isolated SPI clock signal from the main controller to send data onto the isolated MISO bus. The isolated data signal travels back to the main controller through the isolation barrier once again, then finally the main controller uses the leading edge of the same non-isolated SPI clock signal to capture the data. Therefore, there are two additional propagation delays caused by the isolation barrier between the main SPI clock and the secondary MISO data when compared to a non-isolated SPI read operation. The result is that the channel absolute propagation delays become crucial, and the channel PWD and channel-to-channel t_{PSK} are less important. They all together will limit the speed of SPI read operation.

The timing diagram for normal SPI clock is illustrated in the Figure 2. The tpd1 and tpd2 are the propagation delays of the forward channels and reverse channel of the Si86SS51 respectively. The ts1 and th1 are the data setup time and hold time for SPI write cycle, and the ts2 and th2 are the data setup time and hold time for SPI read cycle.

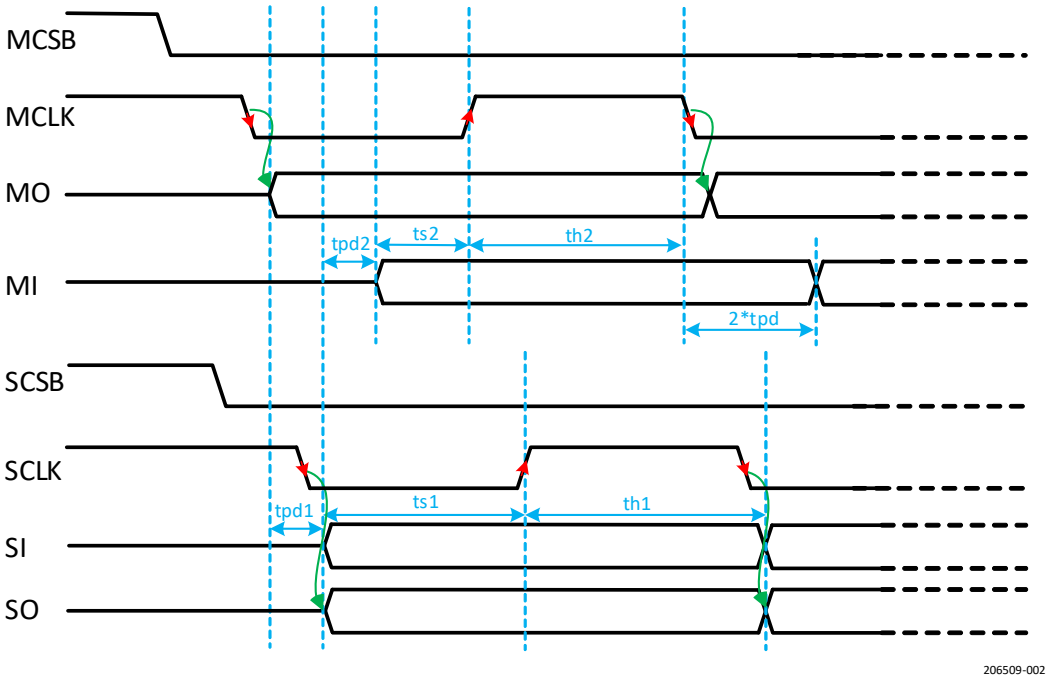

Figure 2. Timing Diagram for Normal SPI Clock

The Si86SS51 has precise channel timing characteristics (<3 ns PWD, <3 ns t_{PSK}, and 9 ns t_{PHL}/t_{PLH}). For an isolated SPI write cycle, the data setup time and hold time will decrease by 6 ns (PWD + t_{PSK}). For an isolated SPI read cycle, the setup time will decrease by 24 ns (PWD + t_{PSK} + t_{PHL}+ t_{PLH}) because two additional channel propagation delays (2 x t_{pd} shown in the above diagram) are consumed by the isolator. Accounting for all these timing delays, the Si86SS51 can support a maximum SPI clock frequency of 10 MHz, or 50 ns half-cycle time.

There are two techniques for an even higher speed SPI clock:

- Asymmetric SPI clock
- Separated SPI clocks

In the asymmetric SPI clock solution, the low-level width of the asymmetric SPI clock is one propagation delay wider than the normal SPI clock, and the high-level width is one propagation delay shorter than the normal SPI clock. This allows the read cycles and the write cycles to share the two additional channel propagation delays (2 x tpd). With the Si86SS51, the data setup time and hold time will decrease by 15 ns: (PWD + t_{PSK} + one propagation delay) for both SPI write and read transactions symmetrically, thus resulting in a maximum SPI clock frequency of up to 20 MHz, or 25 ns half-cycle time for the asymmetric SPI clock configuration.

Figure 3 illustrates the timing diagram for asymmetric SPI clock.

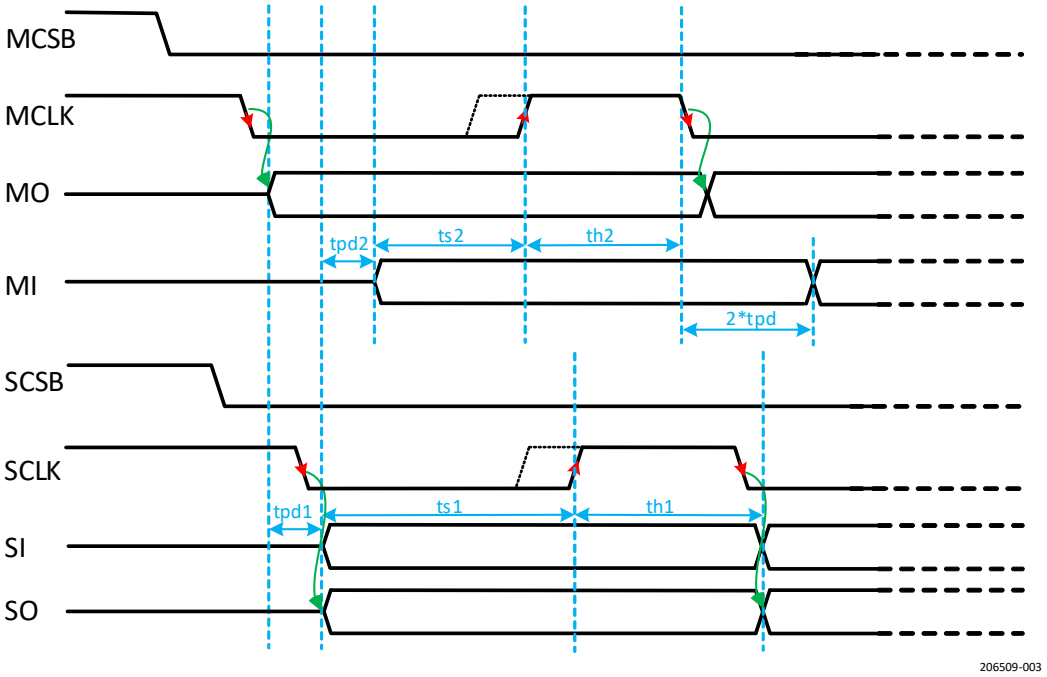

Figure 3. Timing Diagram for Asymmetric SPI Clock

In the separated SPI clocks solution, the SPI controller uses separated clocks to transmit and receive data. One extra reverse isolation channel with the same propagation delay is required to loop back the isolated SPI clock from the secondary to the main. The main controller uses the original non-isolated SPI clock for data transmission and the looped-back isolated SPI clock, with the two consumed propagation delays, for data receipt.

Figure 4 shows the application diagram.

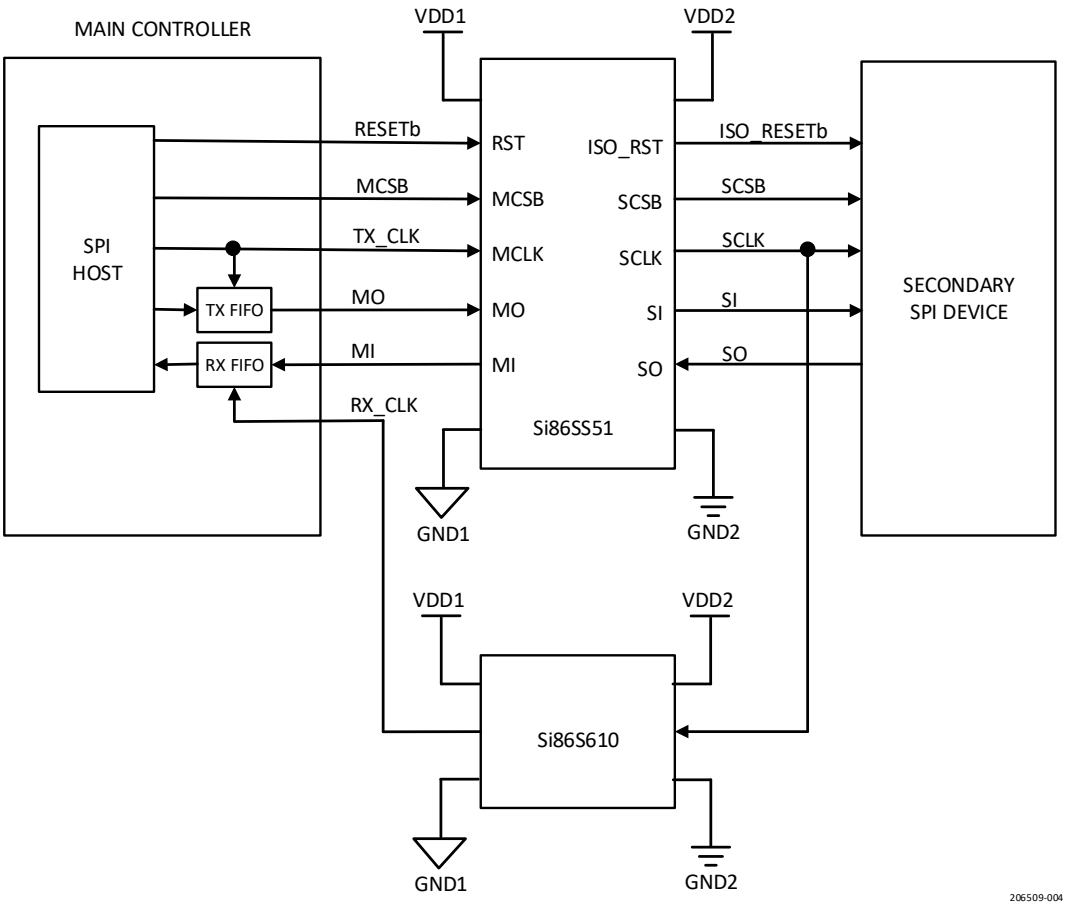

Figure 4. High-Speed SPI Application with Separated SPI Clocks

With this separated SPI clocks technique, the absolute channel propagation delay doesn't matter. With the Si86SS51 and Si86S610, the data setup time and hold time will decrease by 6 ns (PWD + t_{PSK}) for both SPI read and write transactions. Therefore, the SPI clock can reach up to 40 MHz, or 12.5 ns half-cycle time.

Figure 5 illustrates the timing diagram for the separated SPI clocks.

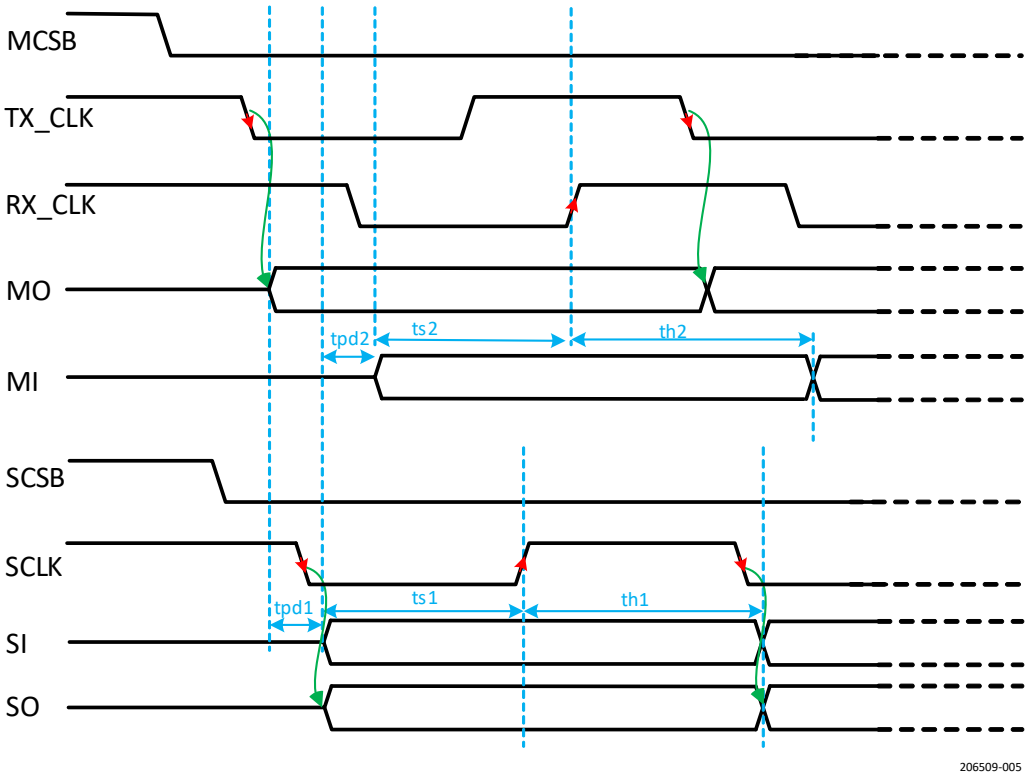

Figure 5. Timing Diagram for Separated SPI Clocks

1.5. QSPI Mode Si86SQ44

The Si86SQ44 digital isolators have four reversible channels whose direction is controlled by one forward direction channel pin (DIR). When the DIR pin is driven high, the signal transmits from Side A to Side B. When it is driven low, the signal transmits from Side B to Side A. The ISO_DIR pin provides an isolated copy of the DIR pin to inform the isolated side host to switch the direction of the channels for half-duplex data transfer. Each side of the device also has an enable pin (EN_A, EN_B) to configure the output as either high-Z or normal CMOS output.

The Si86SQ44's four reversible channels have up to 150 Mbps data rate and a low propagation delay of 10 ns. The systems design engineer can combine the DIR pins and enable pins to implement high speed isolated half-duplex data transfer.

The simple main-secondary 4-bits half-duplex application, with one Si86SQ44, is shown in Figure 6. In this configuration, only the main controller has the capability to change the isolation channels' direction.

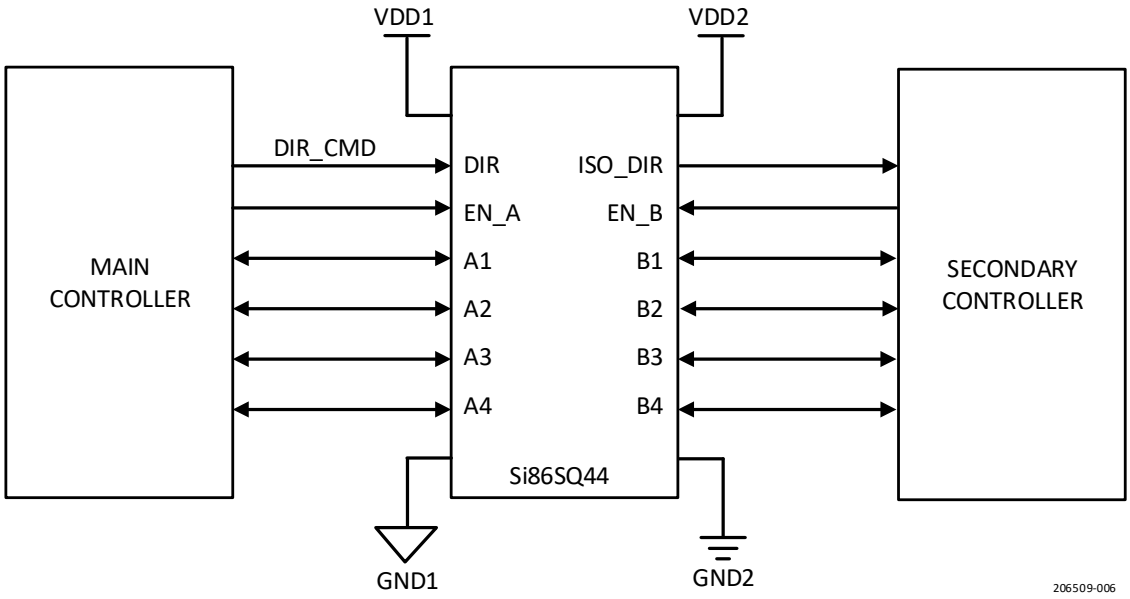

Figure 6. Main-Secondary Half-Duplex 4-bits Data Transfer

The systems design engineer can also use two Si86SQ44s to implement a main-main 8-bits half-duplex application. In this configuration, either one of the main controllers can initialize a data transfer request by sending a bus request signal (BUS_REQ_X, here X can be A or B) through the DIR channel and wait for an acknowledge response from the opposite. If the two main controllers agree with each other or the request signals (BUS_REQ_A, BUS_REQ_B) are either (0,1) or (1,0), then they enable both sides of the isolation barrier and start data transfers.

The main-main 8-bits half-duplex application is shown in Figure 7.

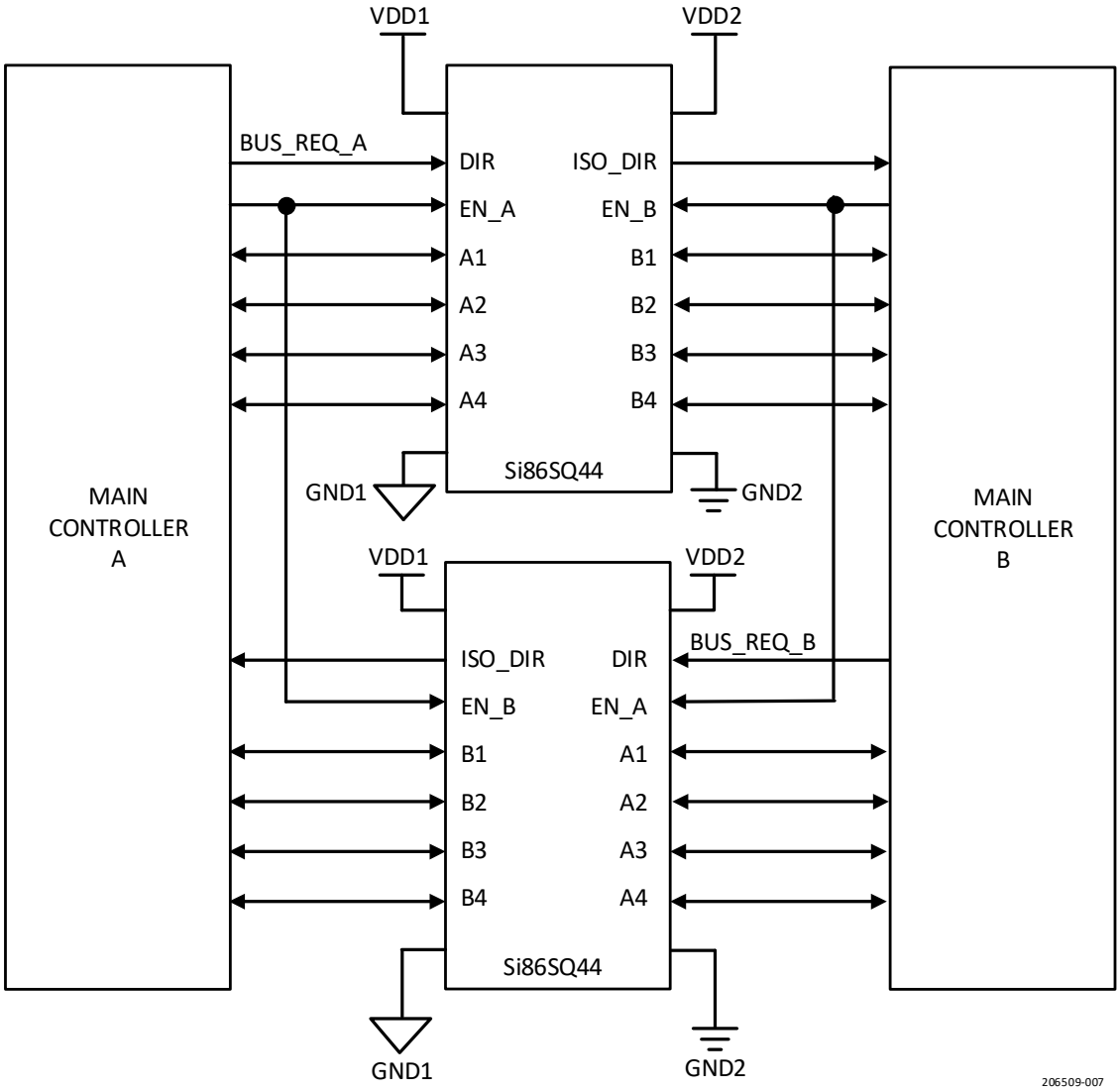

Figure 7. Main-Main Half-Duplex 8-bits Data Transfer

The Si86SQ44s can also be configured with two-mains and multiple-secondaries to create a half-duplex redundancy communication system, as illustrated in Figure 8. The data can be exchanged between two mains, or between the mains and the secondaries. All the controllers (the two mains and the secondaries) share the same 8-bit width bus for data exchange. The two mains use the request signals (BUS_REQ_A, BUS_REQ_B) to indicate the data transfer direction and send a formalized packet which could include commands, address, and data onto the bus. The secondaries monitor the request signals, process the contents in the packet, and respond to the mains if they are called by the mains.

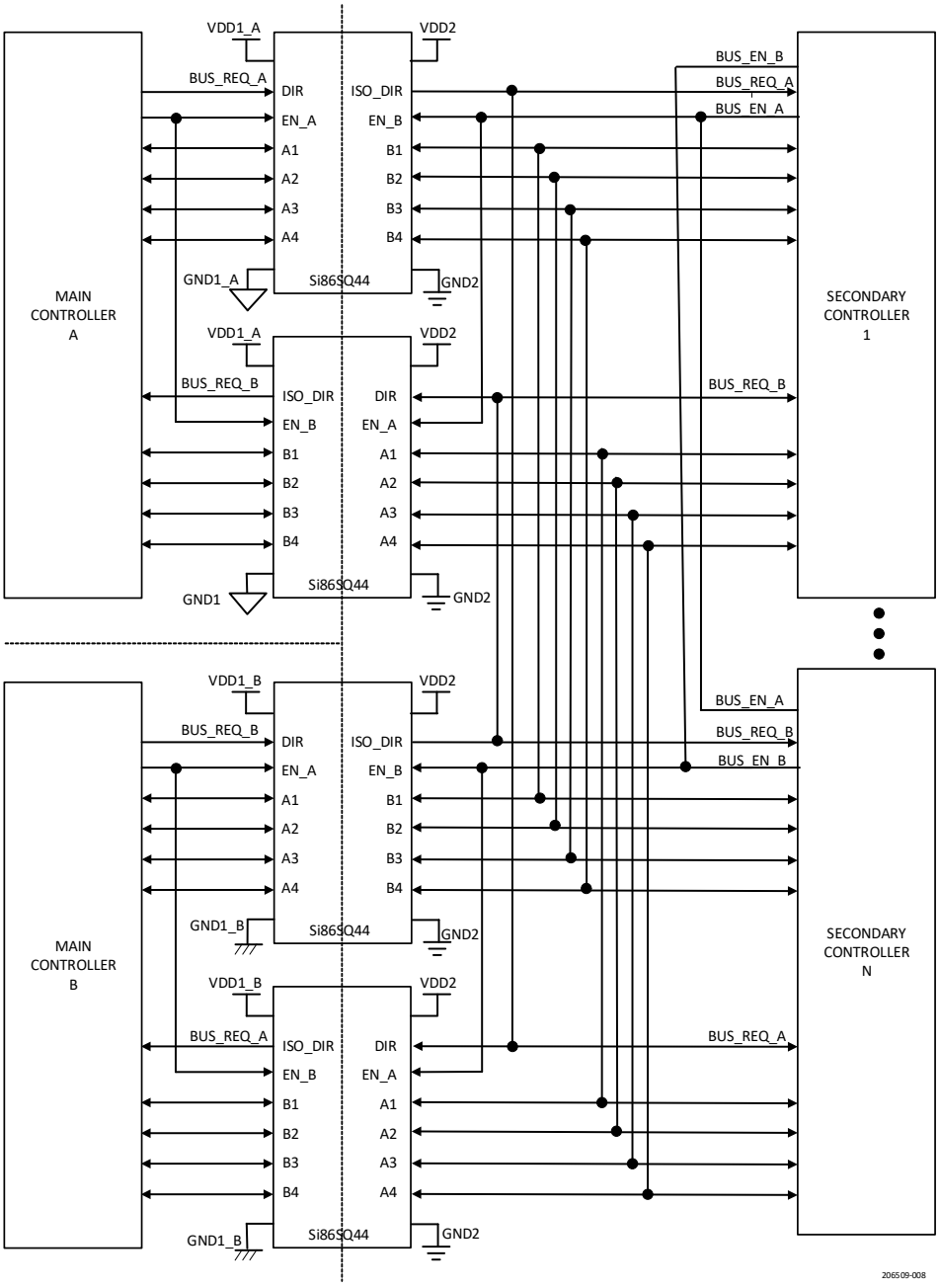

Figure 8. Two-Mains and Multiple-Secondaries Half-Duplex Redundancy System

1.6. Si86SO2x with Inverting Output

The Si86SO2x digital isolators provide two inverting channels with combinations of forward channels and reverse channels. When the input is driven low, the output goes high and when the input is driven high, the output goes low. This inverting logic is very useful in some applications where a NOT gate is needed, like optocoupler replacement, signal inverting for INT, RESET, and FAULT.

This built-in inverting logic in the Si86SO2x can be used in numerous other ways saving application system costs. For instance, the Si86SO2x inverting logic can be used in a low-cost dc/dc converter design where the low-cost power controller doesn't have enough PWM output pins or logic capability to generate enough complementary PWM signals to control the power FET switches. With the Si86SO2x, the systems design engineer can use one PWM signal to generate one or two pairs of complementary signals.

An application example for a full-bridge topology is shown in the Figure 9. In this application, the dc/dc controller generates two phase PWM signals (PH1 and PH2) to control four power switches with the support of one inverting isolator and another non-inverting isolator.

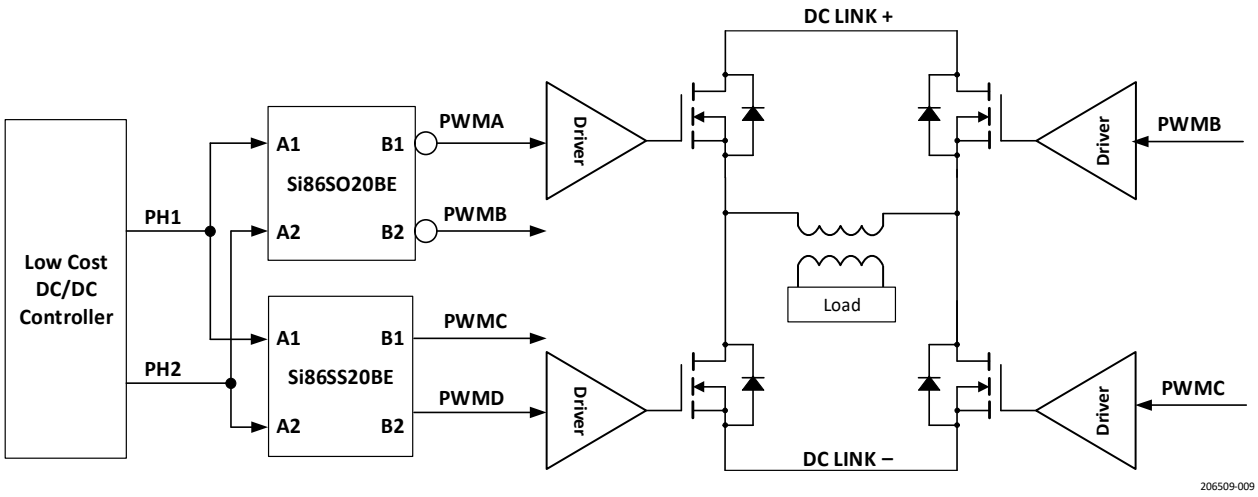

Figure 9. Full-Bridge Power Converter with Low-Cost DC/DC Controller

1.7. Si86SxxxHx-Fx with Deglitch Filter

The Si86SxxxHx/Fx deglitch digital isolators have a deglitch filter with 30 ns delay time for each channel. Any undesirable pulses that are shorter than the deglitch time will not be passed through the filter, making the Si86SxxxHx/Fx a good fit for noisy applications such as industrial automation and power supplies.

With the additional 30 ns time delay, the total propagation delay of the deglitch digital isolators is around 36 ns typical, which matches competitor parts, such as the ADuM3210 and ISO722xC. The similar propagation delay time makes Si86SxxxHx/Fx a good replacement candidate for competitor's legacy parts with upgraded isolation performance in timing-sensitive applications, such as PWM signal isolation in a digital dc/dc converter.

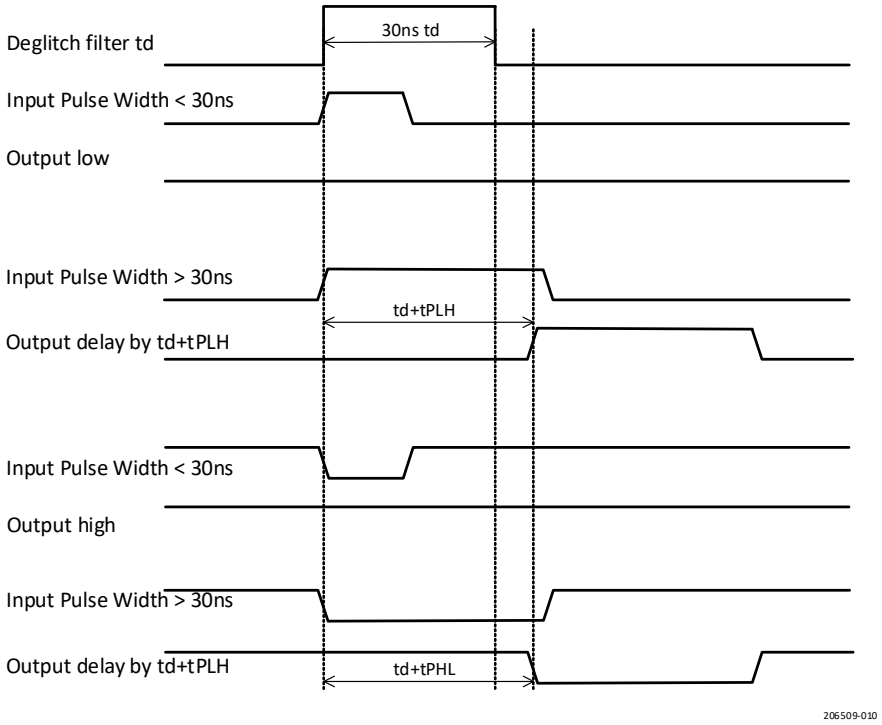

Figure 10. Deglitch Filter for Single Pulse Noise

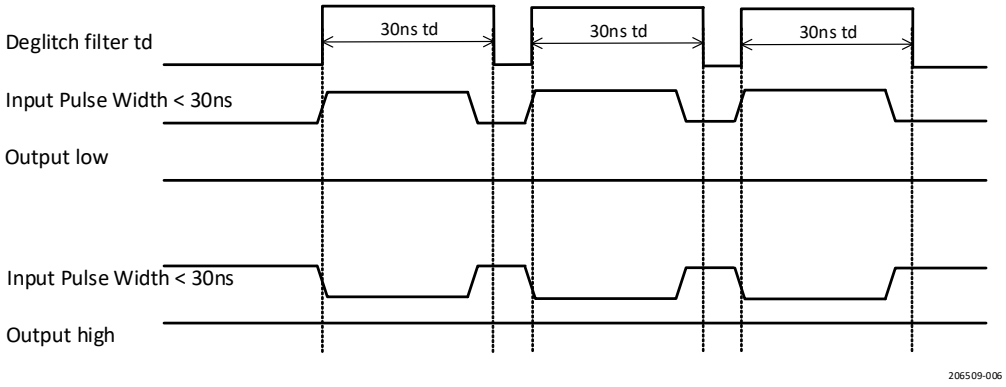

Figure 11. Deglitch Filter for a Series of Pulse Noise

1.8. Si86SWx for Wi-Fi and DECT Applications

For Wi-Fi and DECT applications, Skyworks provides Si86SWxx product options that have a fine tuned internal OOK carrier frequency to specifically avoid interference with 2.4 GHz/5 GHz Wi-Fi and 1.9 GHz DECT frequency bands. There are two product options available, the four-channel Si86SW41BC-IS1 and the six-channel Si86SW62BC-IS1.

Electrical characteristic parameters, such as CMTI and Propagation Delay, are not significantly different compared to the Si86S64/66x options. For more information, please refer to the Skyworks Digital Isolators page.

2. Si86Sx New and Improved Features

The Si86Sx family has several improvements over their drop-in compatible Si86xx counterpart. Specifically, the Si86Sx family offers a higher working voltage isolation barrier, low power and sleep mode options, and higher noise immunity.

Improved Isolation Barrier

- Maximum working insulation voltage: 2121 V_{peak}
- Bipolar surge voltage: >10 kV_{peak}
- Isolation rating: 6.0 kV_{RMS}
- 8 kV contact ESD over isolation barrier
- IEC 60747-17 reinforced insulation compliance

Low Power Design

- Low power mode Si86SLxx: 0.7 mA/ch. quiescent current and 1 mA/ch. active current for 1 Mbps
- Sleep mode Si86SMxx: 0.75 mA per side when sleep mode is enabled.

High Noise Immunity

- Improved CMTI: >100 kV/µS or 150 kV/µS with deglitch filter
- Channel deglitch filter to prevent false trigger due to noisy inputs: 30 ns
- CMOS input thresholds with Schmitt trigger: V_{IL} = 0.3 x VDD V_{IL} and V_{IH} = 0.7 x VDD

Low Radiated Emission

- Low radiated emission: better than Si86xx

Note: The Si86Sx is a good fit for emission sensitive applications, like BMS and automotive. The Si86Sx family employs several techniques (spread-spectrum, minimized current loop, and better matching between differential channels) to achieve lower emissions. For more details on optimizing emissions levels in end systems, see AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks' Isolators.

Figure 12 summarizes additional enhancements over the previous generation.

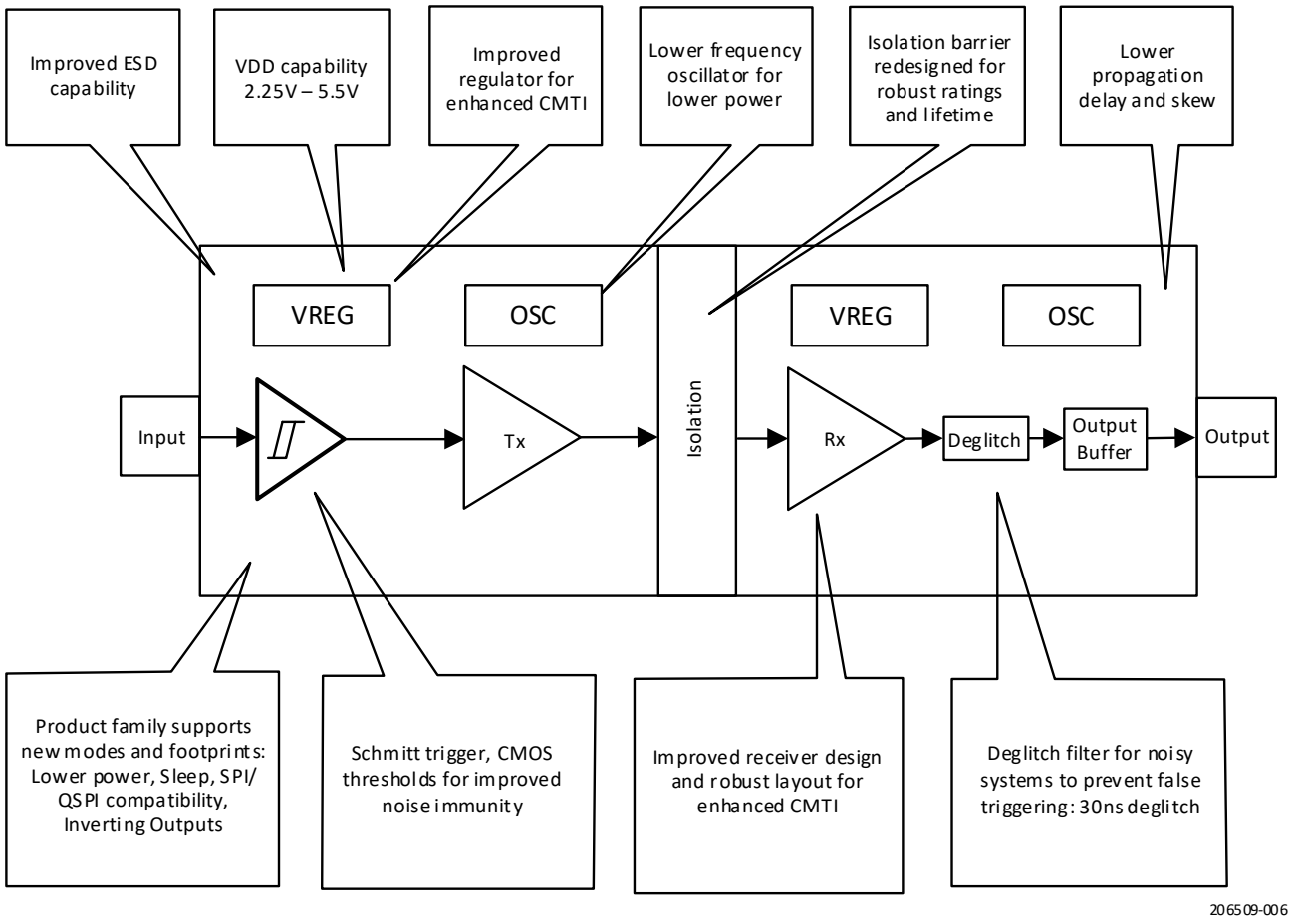

Figure 12. Si86Sx Enhancements

3. Si86Sx Design Considerations for Si86xx Drop-In Replacement

Table 1 lists most of the electrical parameters that need to be considered for the Si86Sx to replace legacy Si86xx.

Table 1. Electrical Characteristics Comparison

Parameter	Symbol	Si86xx	Standard Si86Sx	Unit
Supply voltage	VDD1, VDD2	2.375 – 5.5	2.5-5.5	V
High level input voltage[1]	V_{IH}	2.0 min.	0.7 x VDDx min.	V
Low level input voltage[1]	V_{IL}	0.8 max.	0.3 x VDDx max.	V
Input hysteresis	V_{HYS}	0.38 min.	0.15 x VDDx min.	V
Output impedance	Z_O	50 typ.	50 typ.	Ω
Maximum data rate		150 max.	150 max.	Mbps
Minimum pulse width		5.0 max.	6.7 min.	ns
Propagation delay	t_{PHL}, t_{PLH}	8.0 typ.	9.0 typ.	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	4.5 max.	2.0 max.	ns
Propagation delay skew	$t_{PSK(P-P)}$	4.5 max.	4.5 max.	ns
Channel-channel skew	t_{PSK}	2.5 max.	2 max.	ns
Output rise time	t_r	2.5 typ.	2.5 typ.	ns
Output fall time	t_f	2.5 typ.	2.5 typ.	ns
Peak eye diagram jitter	$t_{JIT(PK)}$	350 typ.	350 typ.	ps
Enable to data valid	ten1	6.0 typ.	12.0 typ.	ns
Enable to data tri-state	ten2	8.0 typ.	11.0 typ.	ns
Input power loss to valid default output	t_{SD}	8.0 typ.	8.0 typ.	ns
Start-up time[2]	t_{SU}	40 max.	300 max.	µs
Supply voltage ramp-up[3]	VDD1, VDD2	50 max.	1 max.	V/µs
Isolation rating	VISO	5.0	6.0	kVRMS
Maximum working insulation voltage	VIORM	1200	2121	Vpeak
Surge voltage	VIOSM	Si86xxxT: >10000 unipolar Si86xxxx: >4000 unipolar	>10000 bipolar	Vpeak
Impulse voltage[4]	VIMP	-	8000	Vpeak
Input to output test voltage	VPR	2250	3977	Vpeak

Table 1. Electrical Characteristics Comparison (Continued)

Parameter	Symbol	Si86xx	Standard Si86Sx	Unit
IEC 61000-4-2 ESD isolation barrier[5]	Contact ESD	Si86xxxT: >6 Si86xxxx: >4	>8	kV
Common Mode Transient Immunity	CMTI	Si86xxxT: >60 Si86xxxx: >35	No deglitch: >100 deglitch: >150	kV/µs

1. Both Si86Sx and Si86xx have similar V_{IH} and V_{IL} thresholds for I^2C channels.
2. The startup time of the Si86Sx family is longer than the Si86xx because of longer initialization.
3. It is a system requirement that supply voltage ramp is less than 1 V/µs for the Si86Sx. The systems design engineer can insert a small resistor (2 to 10 Ω) into the supply pin path, along with the supply bypass capacitors to slow the supply ramp to meet 1 V/µs requirement.
4. Impulse voltage is defined by IEC 60747-17 and tested in air.
5. With Skyworks' new isolation technology, the Si86Sx family can pass 8 kV contact ESD across isolation barrier without external supporting component, which is helpful in ESD demanding applications, like BMS (battery management system) and metering.

3.1. Si86xx Drop-In Replacement Considerations

With the improved isolation barrier and higher noise immunity performance, two electrical parameters (Start-up time and Supply voltage ramp-up) should be taken care of for the drop-in replacement. To successfully replace legacy Si86xx digital isolators with new enhanced Si86Sx family, the following two differences should be considered:

- Start-up time: Si86Sx 300 µs max. vs Si86xx 40 µs max.
- Supply voltage ramp-up rate limit: Si86Sx 1 V/µs vs. Si86xx 50 V/µs.