DATA SHEET

Si5360 18-Output, Any-Frequency, Any-Output Clock Generator with Ultra-Low Jitter

Applications

- 56G/112G/224G PAM4 serializer/deserializer (SerDes) clocking
- OTN muxponders and transponders
- 100/200/400/600/800G networking line cards
- Synchronous Ethernet
- Data center switches
- 100G/200G/400G optical transceivers
- Medical imaging
- Test and measurement

Features

- Utilizes fifth-generation DSPLL® and MultiSynth™ technologies
  - One DSPLL, two MultiSynth
- ANY input to ANY combination of output frequencies up to 1.3 GHz
- Ultra-low phase jitter
  - 55 fs RMS typ (integer mode)
  - 100 fs RMS typ (fractional mode)
- Up to six differential/single-ended Inputs
- Input frequency range
  - External crystal: 48 MHz to 61.44 MHz
  - Differential: 30.72 MHz to 750 MHz
  - LVCMOS: 30.72 MHz to 250 MHz
- 18 Outputs
- Output frequency range
  - Differential: 8 kHz to 1.3 GHz
  - LVCMOS: 8 kHz to 250 MHz
- Fixed or user-adjustable output formats
- Programmable delay at each output
- Simplified API interface
- Pin compatible with Si5361/2/3 jitter attenuators and Si5401/02/03 IEEE 1588 PTP network synchronizers
- 72 QFN 10x10 mm
- ClockBuilder® Pro Configuration Software

Description

The Si5360 Clock Generator combines fifth-generation DSPLL and MultiSynth technologies with an ultra-low jitter VCO to deliver ultra-low jitter (<55 fs) for high-performance applications like 112G and 224G SerDes and coherent optics.They are used in applications that demand the highest level of integration and jitter performance. All PLL components are integrated on-chip, eliminating the risk of noise coupling associated with discrete solutions.

The Si5360 supports free-run and synchronous operation by locking to an external crystal or oscillator or any one of the six input clocks. The Si5360 is quickly and easily configured using Skyworks ClockBuilder® Pro (CBPro) software. ClockBuilder Pro assigns a custom part number for each unique configuration. Devices ordered with custom part numbers are factory-programmed, making it easy to get a custom clock configuration uniquely tailored for each application. Custom part numbers which are factory-programmed will power up with a known frequency configuration.

Using the Si5360 serial interface, the device may be user-configured at power up or internally-configured non-volatile memory (NVM) with new configuration using the ClockBuilder Pro Field Programmer.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

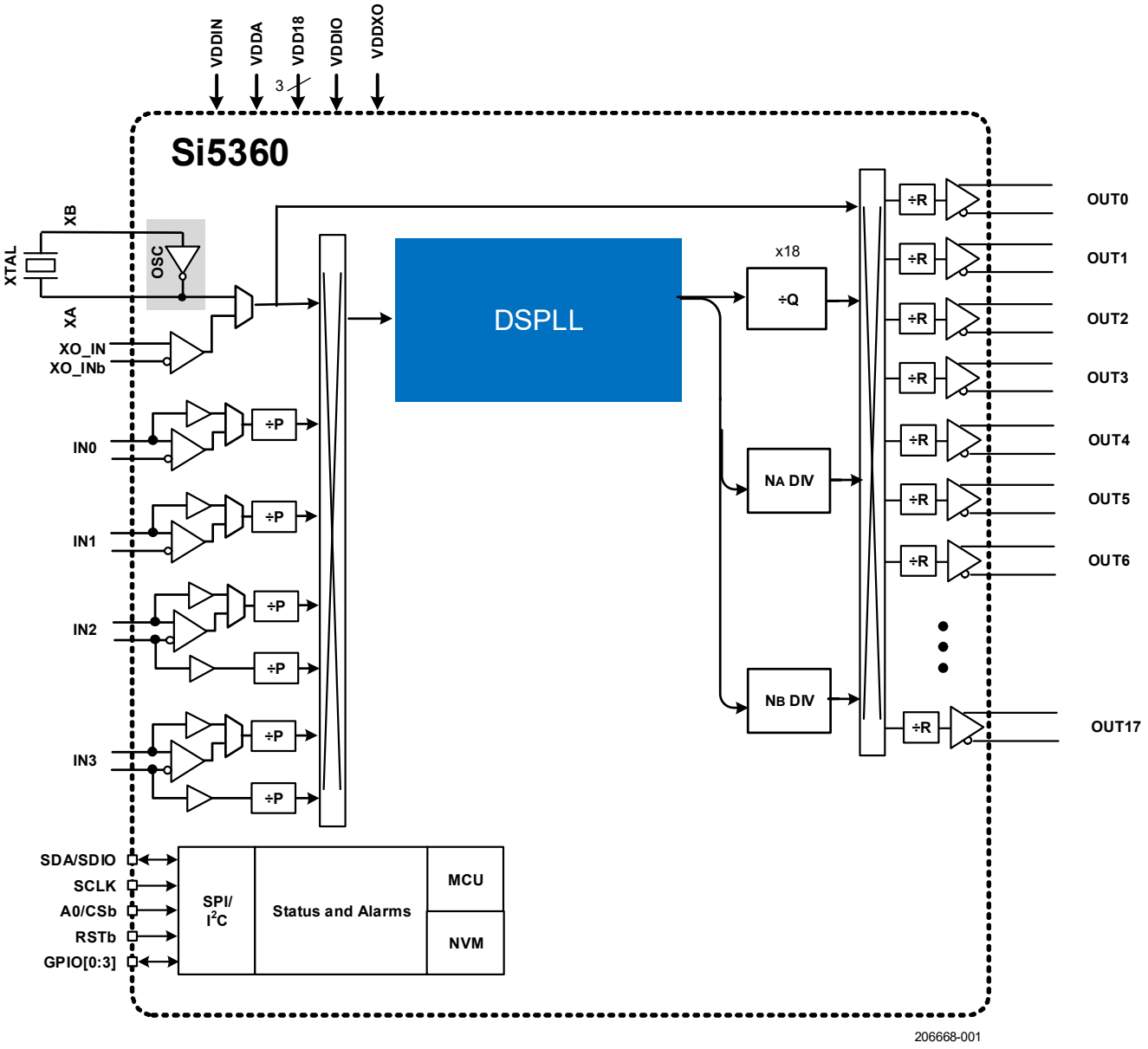


Figure 1. Si5360 Simplified Block Diagram

1. Feature List

- Generates any output frequency in any format from any input frequency
- Ultra-low jitter performance
  - <55 fs RMS typ. in integer mode
  - 100 fs RMS typ. in fractional mode
- Up to 6 differential/single-ended inputs
  - External crystal: 48 MHz to 61.44 MHz
  - Differential:
    - INx: 30.72 MHz to 750 MHz
    - External XO: 30.72 MHz to 983.04 MHz
  - CMOS:
    - INx: 30.72 MHz to 250 MHz
    - External XO: 30.72 MHz to 250 MHz
- 18 programmable clock outputs
  - Integer divider
    - Differential: 8 kHz to 1.3 GHz
    - CMOS: 8 kHz to 250 MHz
  - Fractional divider
    - Differential: 8 kHz to 650 MHz
    - CMOS:8 kHz to 250 MHz
- Highly configurable outputs:
  - Fixed formats LVDS, S-LVDS, LVPECL, LVCMOS, CML, and HCSL
- User-programmable signal amplitude
- Glitchless on-the-fly output frequency changes
- DCO Mode: as low as 0.001 ppb steps
- Status monitoring (LOS and LOL)
- Core voltage: 3.3 V, 1.8 V
- Output supply pins: 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^2C or SPI (3- or 4-wire)
- ClockBuilder Pro software tool simplifies device configuration
- Package: 72-Lead QFN, 10 x 10 mm
- Extended temperature range
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications on this page are for reference only. Refer to Electrical Specifications for device performance.

Pinout Diagram

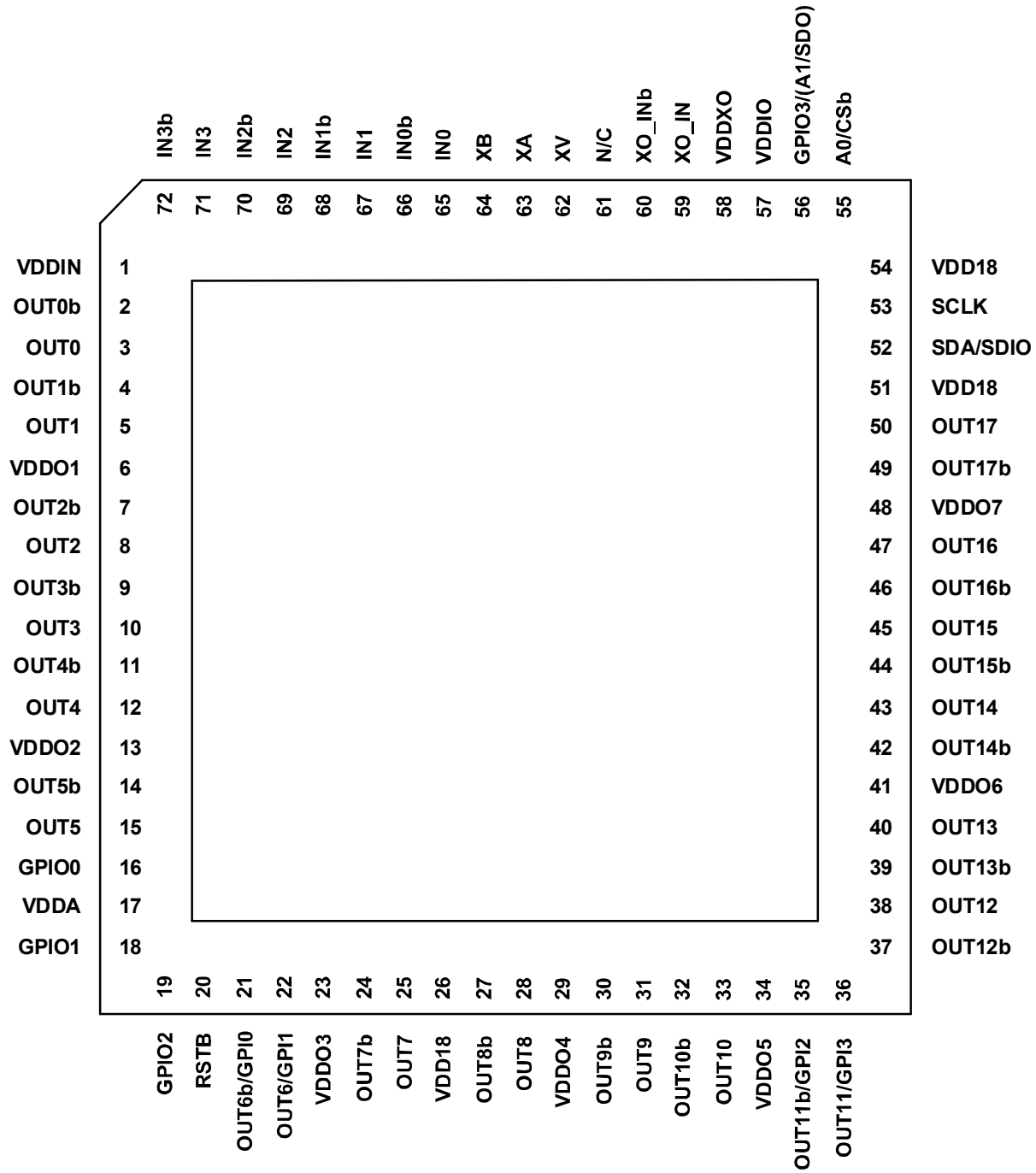


Figure 2. Si5360 Pinout (Top View)

Table 1. Si5360 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
XO_IN	59	I	Input for low phase noise (XO)
XO_INb	60		
XV	62	I	**XTAL Shield** Connect this pin directly to the XTAL and capacitor ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. Refer to the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide" for layout guidelines.
XA XB	63 64	I	**Crystal Input** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
IN0	65	I	**Clock Inputs** IN0-IN3 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. When operating in single- ended mode, inputs IN2 and IN3 can provide two SE inputs each for a total of six inputs. Refer to the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide" for input termination options. These pins are high-impedance and must be terminated externally. IN0-IN3 can be disabled in CBPro and the pins left unconnected if unused.
IN0b	66		
IN1	67		
IN1b	68		
IN2	69		
IN2b	70		
IN3	71		
IN3b	72		
Outputs			
OUT0b	2	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide". Unused outputs should be left unconnected.
OUT0	3		
OUT1b	4		
OUT1	5		
OUT2b	7		
OUT2	8		
OUT3b	9		
OUT3	10		
OUT4b	11		
OUT4	12		
OUT5b	14		
OUT5	15		
OUT6b/GPI0	21	I or O	**Output Clocks with Input Option** Output 6 can alternatively be assigned as two General Purpose Inputs (GPI0, GPI1) that can be programmed to have any of the input control functions listed in 5.10 GPIO Pins General Purpose Input or Output. Regardless of whether Output 6 is functioning as a clock output or GPI, the power supply will be VDDO3.
OUT6/GPI1	22		
OUT7b	24	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. The desired out- put signal format is configurable in CBPro. Termination recommendations are provided in the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide". Unused outputs should be left unconnected.
OUT7	25		
OUT8b	27		
OUT8	28		
OUT9b	30		
OUT9	31		
OUT10b	32		
OUT10	33		
OUT11b/GPI2	35	I or O	**Output Clocks with Input Option** Output 11 can alternatively be assigned as two General Purpose Inputs (GPI2, GPI3) that can be programmed to have any of the input control functions listed in GPIO Pin Descriptions. Regardless of whether Output 11 is functioning as a clock output or GPI, the power supply will be VDDO5.
OUT11/GPI3	36		

Table 1. Si5360 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
OUT12b	37	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide". Unused outputs should be left unconnected.
OUT12	38		
OUT13b	39		
OUT13	40		
OUT14b	42		
OUT14	43		
OUT15b	44		
OUT15	45		
OUT16b	46	O	**Output Clocks with Programmable LVCMOS Slew Rate** When outputs 16 and 17 are configured as LVCMOS outputs, they can also have the slew rate adjusted.
OUT16	47		
OUT17b	49		
OUT17	50		
Serial Interface			
SDA/SDIO	52	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^2C interface. This pin must be pulled high to VDDIO using an external resistor of at least 1 kΩ.
SCLK	53	I	**Serial Clock Input Interface** This is the bidirectional I^2C clock pin. Clock stretching (i.e., driving SCL low to insert wait-states) will be utilized when operating at rates greater than 100 kHz. This pin must be pulled up to VDDIO using an external resistor of at least 1 kΩ.
A0/CSb	55	I	**I^2C Address Select** This pin functions as the optional A0 I^2C address input pin. Attach a 4.7 kΩ pull-up resistor to V_{DDIO}, or a 4.7 kΩ pull-down resistor to ground to select the I^2C slave address. This pin can be left floating if unused.
GPIO3 (A1/SDO)	56	O	**Serial Data Out Pin when Operating in 4-wire SPI Mode** This can also function as the GPIO3 pin when operating in 3-wire SPI mode.
Control/Status			
GPIO0	16	I or O	**Programmable General Purpose Input or Outputs** These pins can be programmed to the functions defined in GPIO Pin Descriptions. See "Si5360 Reference Manual" for more details.
GPIO1	18		
GPIO2	19		
RSTb	20	I	**Device Reset** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to V_{DDIO}. AN1357: Si5360/1/2/3 Schematic Design and Board Layout Guide" for more details on RSTb pin circuitry
Power			
VDDIN	1	P	**Input Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.
VDDO1	6	P	**Output Clock Supply Voltage 1 to 7** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave V_{DDIO} pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins. V_{DDIO} may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 - OUT[0:3] VDDO2 - OUT[4:5] VDDO3 - OUT[6:7] VDDO4 - OUT[8:9] VDDO5 - OUT[10:11] VDDO6 - OUT[12:15] VDDO7 - OUT[16:17] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	13		
VDDO3	23		
VDDO4	29		
VDDO5	34		
VDDO6	41		
VDDO7	48		

Table 1. Si5360 Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
VDDA	17	P	**Core Analog Supply Voltage** This core supply can operate from a 3.3 V or 1.8 V power supply for low power mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin so in low power mode no other supply can exceed 1.8 V. See the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide" for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	26	P	**Core Supply Voltage 1.8 V** The device core operates from a 1.8 V supply. See the "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide" for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	51		
VDD18	54		
VDDIO	57	P	**Control, Status IO Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, Control, and Status inputs and outputs.
VDDXO	58	P	**Reference Supply Voltage** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDXO should be the same voltage as the VDD_XO.
GND PAD	Package bottom	P	**Exposed Die Attach Pad** The exposed die attach pad (ePAD) on the bottom of the package must be connected to electrical ground.
No Connect			
N/C	61	N/C	Leave this pin floating.

1. I = Input, O = Output, P = Power, N/C = No Connect.

2. Functional Description

The Si5360 fifth generation DSPLL provides any-frequency multiplication of the reference or selected input frequency. Input switching is controlled manually via API command. The output frequency stability and accuracy is determined by the crystal and oscillator circuit (OSC) or the selected input reference. The integer dividers (Q) and MultiSynth dividers generate integer or fractionally related output frequencies for the output stage.

A cross point switch connects any of the integer dividers (Q) and MultiSynth generated frequencies to any of the outputs. Additional integer (R) determines the final output frequency for the MultiSynth generated outputs. Integer divider (R) is not used for integer (Q). For best jitter performance, the integer Q divider is preferred.

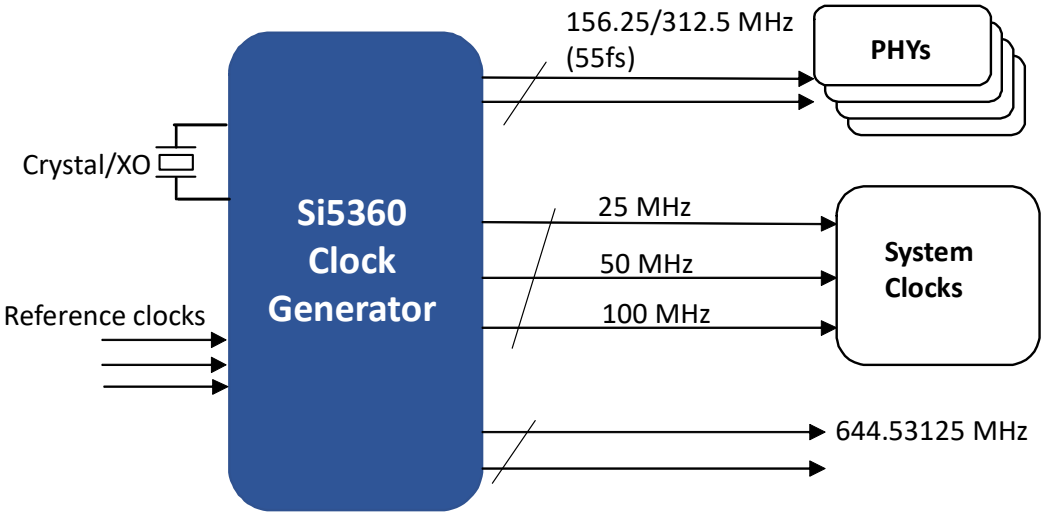


Figure 3. Si5360 Typical 56G/112G SerDes Application (Up to Three Domains)

2.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of input dividers (P), fractional frequency multiplication (M), integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the CBPro utility.

2.2. Inputs

2.2.1. XA/XB Crystal Inputs

An internal crystal oscillator exists between pin XA and XB. When this oscillator is enabled, an external crystal connected across these pins will oscillate and provide a clock input to the PLL. A crystal frequency of 48 MHz can be used although crystals in the frequency range of 48 MHz to 54 MHz are recommended for best jitter performance. The device includes internal XTAL loading capacitors which eliminate the need for external capacitors and also has the benefit of reduced noise coupling from external sources.

The AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for crystal specifications and recommended crystals.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB crystal input. A clock (e.g., XO) may be used through the XO_IN input, but it may result in higher output jitter unless the phase noise of the XO is extremely low. When using an external XO, it is important to select one that meets the jitter performance requirements of the end application. Selection between the external XTAL or input clock is controlled by API command.

2.2.2. XO_IN Inputs

An alternative to using an external XTAL is to connect a crystal oscillator (XO) directly to the XO_IN input. The XO_IN inputs accommodate both single-ended CMOS as well as differential XOs. Note that XO phase noise below the PLL loop bandwidth of approximately 1 MHz will pass through to the output. In addition to selecting XOs with appropriate noise in this frequency band, be sure to filter the VDD supplying power to the XO since many XOs have poor supply rejection.

2.2.3. Input Clocks (IN0, IN1, IN2, IN3)

In addition to the XO_IN input, there are four additional differential inputs which can also be configured as single-ended CMOS inputs. Both IN0 and IN1 can support a single CMOS input, while IN2 and IN3 can be configured as dual CMOS inputs. This allows support for up to six CMOS inputs, or any combination of differential and CMOS inputs.

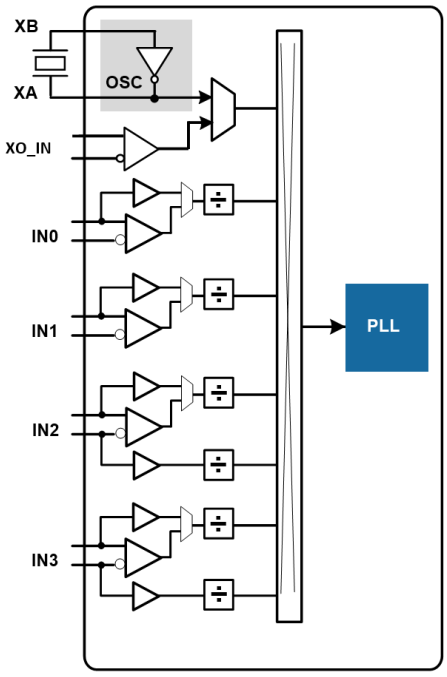


Figure 4. Input Structure

2.2.4. Input Terminations

Refer to "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guidelines" for guidance on input terminations.

2.2.5. Input Selection

Input selection to the PLL can be controlled manually through API command only.

2.2.6. Unused Inputs

Unused inputs should be configured as "Unused (Powered Down)," and the pins may be left unconnected or ac-coupled to ground. Refer to "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guidelines" for recommendations on how to minimize system noise on any CMOS input or any differential input configured as "Enabled" but not actively being driven by a clock.

2.3. Outputs

The Si5360 supports 18 differential output drivers with configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to preset differential levels such as LVPECL, LVDS, S-LVDS, CML and HCSL, the Si5360 can also be programmed to a custom differential threshold that allows the signal to be sent directly to other chipsets without complicated termination circuits, simplifying the complexity of the board layout.

The outputs can also be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 36 single-ended outputs, or any combination of differential and single-ended outputs. Two of the output drivers (OUT16 and OUT17) have slew rate control when in LVCMOS mode. This allows limiting the rise time of the output signal to reduce the possibility of crosstalk to adjacent output drivers. The outputs have power supply pins (VDDOx) for output driver groups of 4-2-2-2-2-4-2, which can be powered at 3.3, 2.5, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to Table 1, "Si5360 Pin Descriptions," on page 5.

2.3.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with the PLL, reference input, or any NA/NB MultiSynth output. A digital output delay adjustment is possible on each of the Q divider outputs to provide output-to-output alignment for the same output source. The crosspoint configuration and delay adjustments are programmable and are stored in NVM so that the desired output configuration is ready at power up.

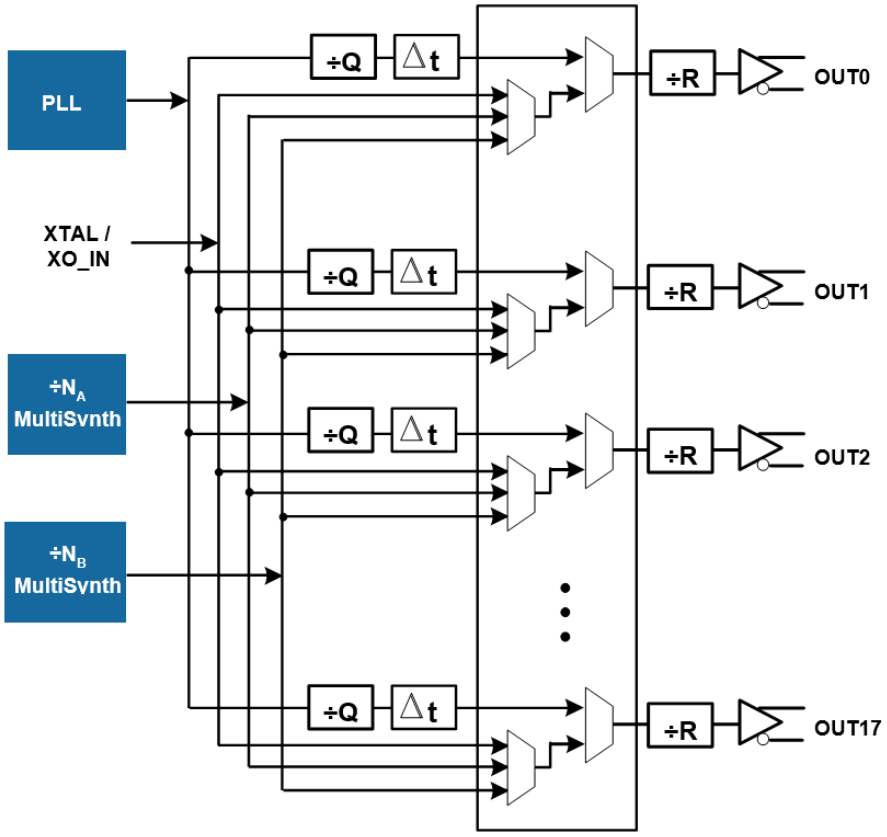


Figure 5. Output Structure

2.3.2. Differential and LVCMOS Output Terminations

Refer to "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guidelines" for guidance on output terminations.

2.3.3. Slew Rate Limited (SRL) LVCMOS Outputs

The swing of LVCMOS and SRL LVCMOS outputs is rail-to-rail; so, the swing is determined by the voltage of the corresponding VDDO pin of the LVCMOS or SRL LVCMOS output. Each output driver configured as LVCMOS or SRL LVCMOS has two outputs, OUTx/OUTxb. The polarity of each of the two outputs may be independently configured as a non-inverted or inverted output as well as enabled or disabled. If the phase between LVCMOS outputs is not critical, it is suggested to configure the pair with one non-inverted and one inverted to reduce noise coupling and noise generated on the supply.

OUT16/16b and OUT17/17b may be configured as SRL LVCMOS outputs, which have a lower slew rate and significantly less crosstalk than conventional LVCMOS outputs.

2.3.4. Output Enable Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are two output enable groups, OE0 and OE1, which are logically ORed together to determine which outputs are enabled at any point in time. CBPro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. If an output is assigned as GPIO controlled, it cannot be controlled via the API. The API controlled output enable allows for more flexibility than the GPIO control as any of the outputs can be individually enabled/disabled via an API command.

2.3.5. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs <2 MHz can also be configured as Hi-Z with weak internal pullup/down.

Differential outputs, when disabled, will maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

2.3.6. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

A summary of each class of divider is listed below:

1. Output Q Divider: Q17-Q0
   a. Integer Only Divide Value
2. Output N Divider: NA, NB
   a. MultiSynth Divider, Integer or Fractional Divide Value
3. Output Divider: R17-R0
   a. Integer Only Divide Value

2.3.7. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase adjusted in steps of 1/fvco or 1/(4*fvco) when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control Tab of the CBPro Wizard.

2.3.8. Dynamic Phase Adjust

Output skew can also be controlled dynamically by API command during operation using OUTPUT_PHINC and OUTPUT_PHDEC. The parameter settings for API control can be found on the ClockBuilder Pro tab of Dynamic Phase Adjust (DPA) Outputs.

2.4. DSPLL®

The DSPLL controls the central VCO which provides many of the essential functions for the device such as generating ultra-low phase noise clocks and maintaining frequency accuracy. It operates by referencing one of many external frequency sources. In crystal mode, a simple low-cost fixed frequency crystal (XTAL) may provide the low

phase noise reference or the DSPLL may lock to a clock input. The option of using a crystal oscillator (XO) is also available.

2.5. MultiSynthA (NA), MultiSynthB (NB)

In general, both MultiSynthA and MultiSynthB have identical performance and flexibility and can be independently configured and controlled through the serial interface. Each of the MultiSynths support an optional DCO mode.

2.5.1. DCO Mode

The DCO in the DSPLL can be frequency controlled in predefined steps ranging from <1 ppt to several ppm. The DCO can be controlled when the DSPLL is locked to an external input. The frequency adjustments are controlled through the serial interface by triggering a Device API command, or by pin control using frequency increments (FINC) or decrements (FDEC). Both the FINC and FDEC pins are available through the configurable GPIO pins. The DSPLL can be assigned to the FINC and FDEC pins. An FINC will add the frequency step word to the DSPLL output frequency, while an FDEC will decrement it.

The PLL feedback divider may also use FINC/FDEC DCO, adjusting all output frequencies simultaneously. This mode is available using API commands only.

2.6. GPIO Pins General Purpose Input or Output

There are four GPIO pins which have programmable functions. They can be assigned as either an input or an output from one of the functions shown in the table below. OUT6/11 can be re-purposed as GPIs when they are not being used as clock outputs.

The GPI are programmable as either active high or active low via ClockBuilder Pro. Active low GPI are indicated by adding a “b” at the end of the function name for example “OEb” as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always de-asserted except for OEx which is asserted by default to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPO) are push-pull and do not require any external pull-up or pull-down resistors.

Table 2. General Purpose Input or Output

Function	Description
GPIO Selectable Control Inputs (GPI)	
FINC	DCO Frequency Increment.
FDEC	DCO Frequency Decrement.
OE0–OE1	Output enable for specific outputs or group of outputs as defined by the grouping assigned in CBPro.
GPIO Selectable Status Outputs (GPO)	
REF_LOS	Loss of signal at XA/XB or XO_IN/XO_INb pins.
INTR	Interrupt pin for the device. Programmable Boolean combination of PLL_LOL, REF_LOS
Serial Interface (I^2C/SPI)	
A1/SDO	A1/SDO of serial interface. Assignable to GPIO3 only.
A0/CSb	A0/CSb of serial interface.
SDA/SDIO	SDA/SDIO of serial interface.
SCLK	SCLK of serial interface.

2.6.1. Device Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads pre-configured register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by API command. The global soft reset API restarts all PLLs without updating register values. Output clocks do not toggle in either type of reset.

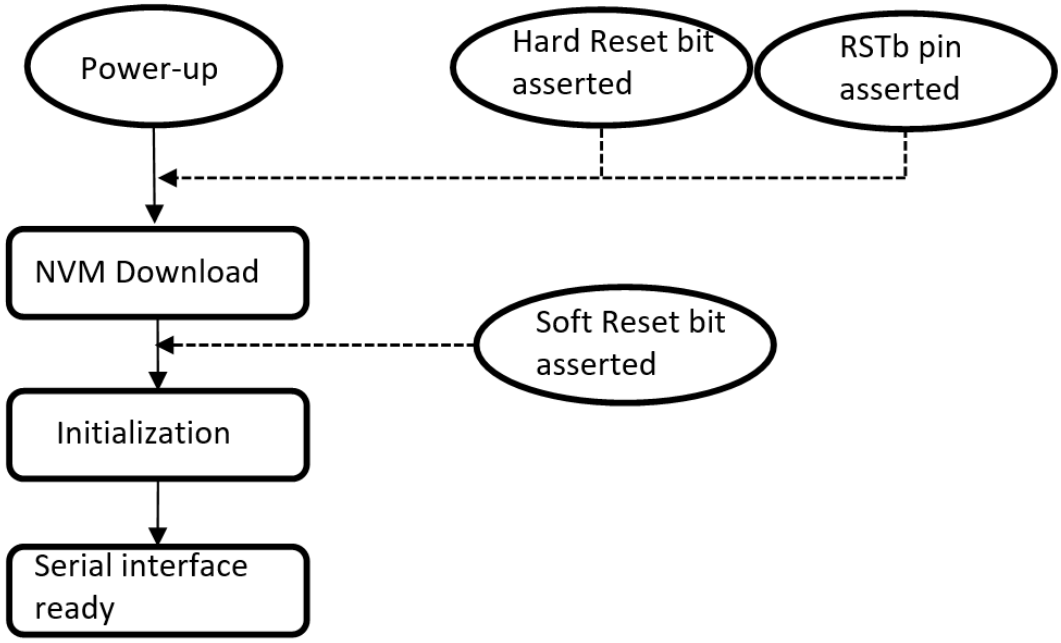


Figure 6. Modes of Operation

2.6.2. Locked Mode

Once locked, the PLL will generate clock outputs that are frequency and phase locked to the selected input clock. Any frequency or phase variation on the input will also appear on the outputs. This includes thermal drift of XO or XTAL inputs.

2.7. Status and Alarms

The Si5360 has monitors for the PLL and input/output clocks. See the "Si5360 Reference Manual" for more information.

2.7.1. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Pin page in CBPro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically ORed together so that the assertion of any of these status indicators will cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin will stay asserted until the sticky status indicators are cleared.

2.8. Serial Interface

Configuration and operation of the Si5360 is controlled by reading and writing API commands using the I^2C or SPI interface. The SPI mode operates in either four-wire or three- wire modes. The following table defines the GPIO pins assigned to the SPI port. For more information, see "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices."

Table 3. Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I^2C
55	CSb	CSb	A0
52	SDIO	SDI	SDA
53	SCLK	SCLK	SCK
56	Unused	SDO	A1

2.9. NVM Programming

At power-up, the device downloads its default configuration and settings from internal one-time-programmable (OTP) non-volatile memory (NVM). The NVM can be pre-programmed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up, or the NVM can be programmed in the field using the API command set. NVM programming in the field must be done with VDDA set to 3.3 V. NVM programming in the field is not supported in Low-Power mode. The NVM can only be burned one time, either at the factory or in the field. For more details on NVM programming, refer to "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices."

2.10. Application Programming Interface API

Communication between the customers' HOST processor and the Si5360 internal microcontroller (MCU) is accomplished through the serial interface. The Si5360 MCU contains API firmware that allows users simple command level access to the device registers. For more details on the Device API and for instructions on programming the clock device, see "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices" and the "Si5360 Reference Manual."

2.11. Power Supplies

The Si5360 has 14 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. Refer to "AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide" for more details on power management and filtering recommendations.

2.11.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA and VDD18 should be powered up before releasing RSTb. VDDA must be equal to the highest voltage supply.

2.11.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 8 on page 20.

2.11.3. Low-Power Mode

In Low-Power Mode, the analog core supply voltage (VDDA) of the Si5360 is set to 1.8 V in order to reduce power consumption. Since VDDA must be equal to the highest voltage applied to the Si5360, in Low-Power Mode, all voltage supplies including VDDO must be 1.8 V. A 1.8 V VDDO restricts the output format to S-LVDS, LVCMOS, or HCSL. If standard LVPECL / LVDS common- mode voltages are required, Low-Power Mode cannot be used.

NVM programming in the field is not supported in Low-Power Mode since NVM programming requires VDDA to be 3.3 V. Refer to “AN1357: Si5360/61/62/63 Schematic Design and Board Layout Guide” for VDDXO and XO/XTAL connections and terminations for Low-Power Mode.

3. Electrical and Mechanical Specifications

All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temp of 25 °C unless otherwise noted.

Table 4. Si5360 Absolute Maximum Ratings[1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	VDDIN		–0.5 to 3.8	V
	VDDXO		–0.5 to 3.8	V
	VDD18	<10 s	–0.5 to 2.4	V
	VDDA	<10 s	–0.5 to 3.8	V
	VDDO	<10 s	–0.5 to 3.8	V
	V_{DDIO}	<10 s	–0.5 to 3.8	V
Input voltage range	V_{I1}	XO_IN/XO_INb, INx/INxb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/SDIO, A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up tolerance	LU		JESD78 Compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage range	TSTG		–55 to 150	°C
Maximum junction temperature in operation	T_{JCT}		125	°C
Soldering temperature (Pb-free profile)[4]	TPEAK		260	°C
Soldering time at TPEAK (Pb-free profile)[4]	TP		20 to 40	s

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. RoHS-6 compliant.
3. For more packaging information, go to https://www.skyworksinc.com/Product_Certificate.aspx
4. The device is compliant with JEDEC J-STD-020.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 5. Si5360 Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC[1]	CEVB[2]	
Thermal Resistance Junction to Ambient	θ_{JA}	Still air	16.15	11.17	°C/W
		1 m/s	10.77	8.10	°C/W
		2 m/s	9.63	7.53	°C/W
Thermal Resistance Junction to Board	Ψ_{JB}[3]	Still air	3.33	3.08	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JC}	Still air	0.03	0.05	°C/W

1. Based on PCB dimension: 4" x 4.5", PCB thickness: 1.6 mm, number of Cu layers: 2.
2. Customer EVB: 8-layer board, board dimensions: ~9 x 9", all 8-layers are copper poured.
3. ΨJB can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan, $T_J = T_{PCB} + \Psi JB * PD$. T_{PCB} should be measured as close to the Si5360 DUT as possible since temperature may vary across the PCB.

Table 6. Si5360 Recommended Operating Conditions

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature	T_A		–40	25	95	°C
Board temperature	T_B		–40	65	105	°C
Junction temperature	TJ_{MAX}[1]		—	—	125	°C
Core supply voltage	V_{DD18}		1.71	1.80	1.89	V
	VDDA[2]		3.14	3.30	3.47	V
		Low-power mode	1.71	1.80	1.89	V
	VDDXO		3.14	3.30	V_{DDA}[2]	V
		Low-power mode	1.71	1.80	1.89	V
Input supply voltage	VDDIN		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
GPIO supply voltage	VDDIO		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
Clock output driver supply voltage	VDDO		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. T_J cannot exceed a max of 125 °C.
2. V_{DDA} must be greater than or equal to the highest voltage applied to the device. In Low-Power Mode, all voltage supplies must be set to 1.8 V.

Table 7. Si5360 Performance Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Comment	Min	Typ	Max	Units
Initial start-up time	t_{START}[1]	Time from POR to when the device generates output clocks from NVM frequency plan	—	25	40	ms
	t_{RDY}	POR to API ready	—	25	30	ms
PLL re-lock time[2]	t_{ACQ}		—	25	40	ms
Output delay adjustment (typical T_{VCO}= 90 ps)	t_{QDIV}	Range[2, 3]	–TVCO x 127	—	+T_{VCO} x 127	ps
		Resolution		TVCO	—	ps
		Resolution (fine delay enabled)		TVCO/4	—	ps
Pull-in range	ω_P		—	±100	—	ppm
RMS jitter crystal reference[4, 5, 9]	Q Div	644.53125 MHz	—	52	70	fs
		625 MHz	—	53	82	fs
		390.625 MHz	—	52	70	fs
		322.265625 MHz	—	52	70	fs
		312.5 MHz	—	54	70	fs
		156.25 MHz	—	55	74	fs
		125 MHz	—	60	80	fs
		100 MHz	—	65	85	fs
	MultiSynth NA/NB Div	644.53125 MHz	—	57	75	fs
		322.265625 MHz	—	58	80	fs
		156.25 MHz	—	64	85	fs
		125 MHz	—	70	96	fs
		100 MHz	—	112	130	fs
		25/50 MHz	—	130	155	fs
RMS jitter clock input (INx/INxb)[4, 6, 9]	Q Div	644.53125 MHz	—	102	135	fs
		390.625 MHz	—	105	145	fs
		312.5 MHz	—	100	124	fs
		156.25 MHz	—	98	121	fs
		125 MHz	—	112	140	fs
		100 MHz	—	106	132	fs
		25/50 MHz	—	109	140	fs
	MultiSynth NA/NB Div	644.53125 MHz	—	104	135	fs
		322.265625 MHz	—	102	132	fs
		156.25 MHz	—	103	125	fs
		125 MHz	—	120	146	fs
		100 MHz	—	140	162	fs
Buffered output jitter performance 12 kHz to 20 MHz		Crystal mode[7]	—	78	—	fs
		XO_IN additive jitter[8]	—	39	—	fs

1. Assumes crystal, XO or clock input is available at power up.
2. Time between manual input clock selected and PLL re-locked
3. Output delay adjustment range will vary depending on frequency plan. Output delay adjust range (ns) is displayed in the “Output Skew Control” step of the CBPro Wizard.
4. Added jitter and spurs due to crosstalk is frequency plan dependent and can be determined using the ClockBuilder Pro Spur Analysis tool.
5. Jitter generation conditions: XTAL = 54 MHz TXC 7M54072006, LVPECL and HCSL output formats.
6. Jitter generation conditions: fin = 156.25 MHz from a low noise differential clock input, LVPECL and HCSL output formats.
7. Jitter generation conditions: fout=54 MHz, XTAL = 54 MHz TXC 7M54072006, LVPECL and HCSL output formats.
8. Jitter generation conditions: fout =122.88 MHz output, 3.3 V LVCMOS input, LVPECL and HCSL output formats.
9. Jitter generation conditions: fout >= 100 MHz using 12 kHz to 20 MHz, <100 MHz using 10 kHz to 5 MHz integration ranges.

Table 8. Si5360 DC Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current (VDD18 + VDDA)	I_{DD18}	Si5360[1, 2]	—	404	654	mA
	I_{DDA}	Si5360[1,2]	—	193	233	mA
	I_{DD18_PD}	RSTb = 0	—	120	300	mA
	I_{DDA_PD}	RSTb = 0	—	15	16	mA
Peripheral supply current (VDDIN + VDDIO + VDDXO)	I_{DDIN} + I_{DDIO}	Si5360[1,2]	—	32	49	mA
	I_{DDXO}	Si5360[1,2]	—	12	15	mA
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDXO_PD}	RSTb = 0	—	2	3	mA
Output buffer supply current (VDDOX)	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 156.25 MHz[3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 156.25 MHz[3]	—	13	15	mA
		S-LVDS (1.8 V) @ 156.25 MHz[3]	—	12	14	mA
		CML (1.8 V, 2.5 V, 3.3 V) @ 156.25 MHz[3]	—	14	17	mA
		3.3 V LVCMOS @ 156.25 MHz[4]	—	19	22	mA
		2.5 V LVCMOS @ 156.25 MHz[4]	—	15	17	mA
		1.8 V LVCMOS @ 156.25 MHz[4]	—	11	22	mA
		HCSL internal termination (1.8 V, 2.5 V, 3.3 V)@ 156.25 MHz[5]	—	20	23	mA
	I_{DDOX_PD}	RSTb = 0	—	0.23	0.3	mA
Total power dissipation	P_D	Si5360[1]	—	2	2.8	W
		Si5360 low-power mode[2]	—	1.4	2	W
Supply voltage ramp rate	T_{VDD}	Fastest VDD ramp rate allowed on startup	—	—	100	V/ms

1. Typical test configuration: The following frequencies on 12 LVDS outputs:
   Four 156.25 MHz (Q)
   Two 312.5 MHz (Q)
   One 125 MHz (Q)
   One 100 MHz (NB)
   One 50 MHz (NB)
   Two 644. 53125MHz (NA)
   One 322.265625 MHz (NA)
   Excludes power in termination resistors. VDDIN = 1.8 V, VDDO = 3.3 V.
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100 Ω load.
4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se

Table 9. Si5360 Input Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVCMOS (XO Applied to XO_IN)						
Input frequency range	fIN_CMOS		30.72	—	250	MHz
Slew rate[1, 2, 3]	SR		0.75	—	—	V/ns
Input voltage	VIL		—	—	VDDXO x 0.3	V
	VIH		VDDXO x 0.7	—	—	V
Input resistance	RIN		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	CIN_SE		—	1.25	—	pF
Differential (XO Applied to XO_IN)						
Input frequency range	fIN_DIFF		30.72	—	983.04	MHz
Voltage swing[2]	VIN_DIFF		200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
Slew rate[1, 2, 3]	SR		0.75	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	CIN_DIFF		—	2.5	—	pF
Crystal (Connected to XA/XB Pins)[4]						
Frequency range	fIN_XTAL		48	—	61.44	MHz
Load capacitance	CL		—	8	—	pF
Crystal drive level	dL		—	—	200	µW
Equivalent series resistance	RESR		Refer to the Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual to determine ESR and shunt capacitance values.			
Shunt capacitance	C0					
Differential (INx/INxb)						
Input frequency range	fIN_DIFF	Differential, AC coupled	30.72	—	750	MHz
	fIN_SE	Single-ended, AC coupled	30.72	—	250	MHz
Voltage swing	VIN_DIFF	Differential, AC coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	VIN_SE	Single-ended, AC coupled	400	1600	1800	mVpp_se
Slew rate[3, 5]	SR		0.4	—	—	V/ns
Duty cycle	DC		40	—	60	%
Capacitance	CIN_DIFF		—	2.5	—	pF
LVCMOS (INx/INxb)						
Input frequency range	fIN_LVCMOS		30.72	—	250	MHz
Slew rate[3, 5]	SR		0.2	0.4	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF

Table 9. Si5360 Input Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Other Control Input Pins - RSTb, FINC, FDEC, OE, PLLx_INSEL[#], IN_FAIL[#]						
Update rate	f_{UR}	RSTb[6]	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum pulse width	PW		150	—	—	ns
Programmable internal pullup, pulldown	R_{IN}		—	20	—	kΩ

1. The minimum slew rate on the XO applied to XO_IN is recommended to meet the specified jitter performance”
2. To achieve this slew rate and voltage swing use one of the XOs from the "Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual” placed as close as possible to the XO_IN pins.
3. Slew rate can be estimated using the following simplified equation: SR = ((0.8 - 0.2) x VIN_VPP_se)/tr.
4. To meet specified jitter performance use one of the XTALs from the "Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual".
5. The minimum slew rate on the input clock applied to INx/INxb is recommended to meet the specified input-to-output delay performance.
6. Glitches and toggles on RSTb more frequent than fUR may cause the device to lock up in reset. Power cycle the device to restore operation.

Table 10. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output frequency[5]	f_{OUT}	Q divider (Grade A/C)[1]		0.008	—	1300	MHz
		Q divider (Grade B/D)[1]		0.008	—	350	MHz
		NA, NB divider (Grade A)[2]		0.008	—	650	MHz
		NA, NB divider (Grade B)[2]		0.008	—	350	MHz
Duty cycle	DC	f < 400 MHz		49.5	50.0	50.5	%
		400 MHz < f < 1.3 GHz		48.0	50.0	52.0	%
Output-to-output skew	T_{SK}	Q divider outputs, same differential format		–50	—	50	ps
		Multisynth (NA or NB) outputs, same differential format, same Multisynth					
OUT-OUTb skew[3]	T_{SK_OUT}	VDDO = 3.3 V	LVPECL, LVDS, CML and custom diff f < 500 MHz	—	—	10	ps
		VDDO = 2.5 V	LVPECL, LVDS, CML and custom diff f < 500 MHz	—	—	25	ps
		VDDO = 3.3 V/2.5 V	LVPECL, LVDS, CML, and custom diff f > 500 MHz	—	—	25	ps
		VDDO = 1.8 V	CML, S-LVDS, and custom diff all frequencies	—	—	35	ps
Output voltage swing[4]	V_{OUT}	VDDO = 3.3 V/2.5 V	LVDS	330xSF	360xSF	380xSF	mVpp_se
		VDDO = 1.8 V	S-LVDS	350xSF	370xSF	410xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	AC-coupled LVPECL	780xSF	840xSF	910xSF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8 V	CML	390xSF	420xSF	460xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	Custom Diff 600 mVpp_se	560xSF	610xSF	650xSF	mVpp_se

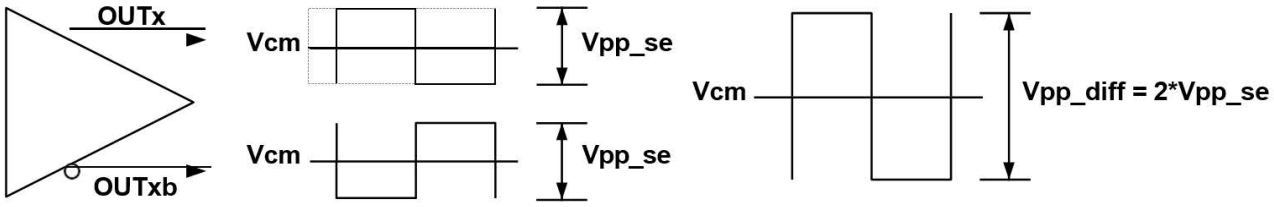
Table 10. Differential Clock Output Specifications(Continued)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output voltage swing scaling factor (SF) OUT0-15[6]	SF	f < 500 MHz		1.00	1.00	1.00	
		500 MHz < f < 1 GHz		0.90	0.95	1.00	
		1 GHz < f < 1.3 GHz		0.80	0.90	1.00	
Output voltage swing scaling factor (SF) OUT16-17[6]	SF	f < 500 MHz		1.00	1.00	1.00	
		500 MHz < f < 1 GHz		0.85	0.95	1.00	
		1 GHz < f < 1.3 GHz		0.80	0.90	0.95	
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V	LVDS, custom differential, CML, AC-coupled LVPECL	1.15	1.20	1.25	V
		VDDO = 1.8 V	S-LVDS, CML	0.85	0.90	0.95	V
Rise and fall times (20% to 80%) OUT0–15	t_r/t_f	VDDO = 3.3 V/2.5 V	LVDS, AC-coupled LVPECL, custom diff	—	125	260	ps
		VDDO = 1.8 V	S-LVDS	—	150	270	ps
		VDDO = 3.3 V/2.5 V/1.8 V	CML	—	150	280	ps
Rise and fall times (20% to 80%) OUT16–17	t_r/t_f	VDDO = 3.3 V/2.5 V	LVDS, AC-coupled LVPECL, custom diff	—	140	300	ps
		VDDO = 1.8 V	S-LVDS	—	165	310	ps
		VDDO = 3.3 V/2.5 V/1.8 V	CML	—	165	320	ps
Differential output impedance	Z_O	All differential formats		—	100	—	Ω
Power supply noise rejection[7]	PSR	25 kHz sinusoidal noise		—	-94	—	dBc
		100 kHz sinusoidal noise		—	-95	—	dBc
		500 kHz sinusoidal noise		—	-91	—	dBc
		1 MHz sinusoidal noise		—	-91	—	dBc
Output-to-output crosstalk[8]	$XTALK_{OUT}$	Differential outputs, same format		—	-95	—	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB Multisynths support any output frequency within the specified range.
3. Skew between positive and negative output pins.
4. Output voltage swing is dependent on frequency range. Scale all values by the Output Voltage Swing Scaling Factor (SF). Voltage swing is specified in mVpp_SE as shown below.



5. HCSL output format is not supported for f_{OUT} > 400 MHz.
6. OUT16/17 have programmable slew rate limit capability when configured as SRL LVCMOS. This causes additional attenuation for higher frequency outputs. The output voltage swing scaling factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for f_{OUT} > 500 MHz.
7. Measured for a 156.25 MHz LVDS output frequency. 100 mVpp sine wave noise added to VDDO = 3.3 V and noise spur amplitude measured.
8. Crosstalk spur measured with the victim running at 156.25 MHz and the aggressor at 155.52 MHz. Victim and aggressor are separated by two unused channels.

Table 11. Si5360 HCSL Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider (Grade A/C)[1]		0.008	—	500	MHz
		Q divider (Grade B/D)[1]		0.008	—	350	MHz
		NA, NB divider[2] (Grade A)		0.008	—	500	MHz
		NA, NB divider (Grade B)[2]		0.008	—	350	MHz
Duty cycle	DC	f < 400 MHz		49.5	50.0	50.5	%
		400 MHz < f < 500 MHz		48.0	50.0	52.0	%
Output-to-output skew	T_{SK}	Q divider outputs, same differential format[3]		–50	—	50	ps
		Multisynth (NA or NB) outputs, same differential format, same Multisynth					
OUT-OUTb skew[3]	T_{SK_OUT}	VDDO = 3.3 V	HCSL Standard, 800 mVpp_se, int term	—	—	15	ps
			HCSL Standard, 800 mVpp_se, ext term	—	—	25	ps
			HCSL Fast, 800 mV or_1200 mV, ext term	—	—	10	ps
		VDDO = 2.5 V	HCSL Standard, 800 mVpp_se, int term	—	—	15	ps
			HCSL Standard, 800 mVpp_se, ext term	—	—	30	ps
			HCSL Fast, 800 mV or_1200 mV, ext term	—	—	20	ps
		VDDO = 1.8 V	HCSL Standard, 800 mVpp_se, int term	—	—	22	ps
			HCSL Standard, 800 mVpp_se, ext term	—	—	70	ps
			HCSL Fast, 800 mV, ext term	—	—	36	ps
Output voltage swing[4]	V_{OUT}	VDDO = 3.3 V/2.5 V/1.8V	HCSL Standard, 800 mVpp_se, int term	740xSF	810xSF	895xSF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8V	HCSL Standard, 800 mVpp_se, ext term	730xSF	810xSF	930xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	HCSL Fast, 800 mVpp_se, ext term	730xSF	810xSF	930xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	HCSL Fast, 1200 mVpp_se, ext term	1100xSF	1175xSF	1260xSF	mVpp_se
Output voltage swing scaling factor (SF) Standard, 800 mVpp_se, int term OUT0-17	SF	f < 10 MHz		1.00	1.00	1.00	
		10 MHz < f < 100 MHz		0.91	0.94	0.95	
		100 MHz < f < 200 MHz		0.89	0.91	0.93	
		200 MHz < f < 400 MHz		0.83	0.85	0.92	
		f > 400 MHz		0.74	0.78	0.89	
Output voltage swing scaling factor (SF) Standard, 800 mVpp_se, ext term OUT0-17	SF	f < 10 MHz		1.00	1.00	1.00	
		10 MHz < f < 100 MHz		0.97	0.96	0.97	
		100 MHz < f < 200 MHz		0.94	0.93	0.95	
		200 MHz < f < 400 MHz		0.91	0.90	0.88	
		f > 400 MHz		0.68	0.71	0.75	
Output Voltage swing scaling factor (SF) Fast, 800 or 1200 mVpp_se, ext term OUT0-17	SF	f < 10 MHz		1.00	1.00	1.00	
		10 MHz < f < 100 MHz		0.98	0.99	0.99	
		100 MHz < f < 200 MHz		0.94	0.94	0.96	
		200 MHz < f < 400 MHz		0.94	0.95	0.97	
		f > 400 MHz		0.89	0.92	0.95	

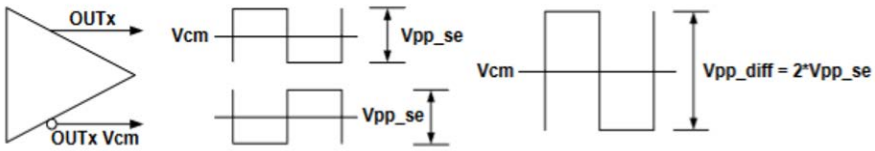
Table 11. Si5360 HCSL Clock Output Specifications(Continued)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Common mode voltage	V_{CM}	V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL 800 mVpp_se	0.35	0.425	0.52	V
		V_{DDO} = 3.3 V/2.5 V	HCSL 1200 mVpp_se	0.55	0.60	0.68	V
Rise and fall times (20% to 80%) OUT0–15	tr/tf	V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL Fast, 800 or 1200 mVpp_se, ext term	—	270	360	ps
		V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800 mVpp_se, ext term	—	450	700	ps
		V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800 mVpp_se, int term	—	270	420	ps
Rise and fall times (20% to 80%) OUT16–17[5]	tr/tf	V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL Fast, 800 or 1200 mVpp_se, ext term	—	285	400	ps
		V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800 mVpp_se, ext term	—	465	740	ps
		V_{DDO} = 3.3 V/2.5 V/1.8 V	HCSL Standard, 800 mVpp_se, int term	—	285	460	ps
Differential output impedance	Z_O	HCSL Standard Slew Rate, int term		—	100	—	Ω
		HCSL Standard Slew Rate, ext term		—	Hi-Z	—	Ω
		HCSL Fast Slew Rate, ext term		—	200	—	Ω
Output-to-output cross-talk[6]	$XTALK_{OUT}$	HCSL outputs, same format		—	-95	—	dBc

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB Multisynths support any output frequency within the specified range.
3. Skew between positive and negative output pins.
4. Output voltage swing is dependent on frequency range, HCSL slew rate and HCSL termination settings. Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_se as shown below.



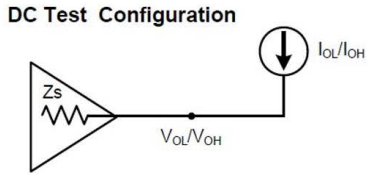
5. OUT16/17 have programmable slew rate limit capability when configured as LVCMOS. This causes additional attenuation for higher frequency outputs. The Output Voltage Swing Scaling Factor (SF) for OUT16/OUT17 is shown below. It is recommended to use OUT0-15 for f_{OUT} > 491.52 MHz.
6. Crosstalk spur measured with the victim running at 156.25 MHz and the aggressor at 155.22 MHz. Victim and aggressor are separated by two unused channels.

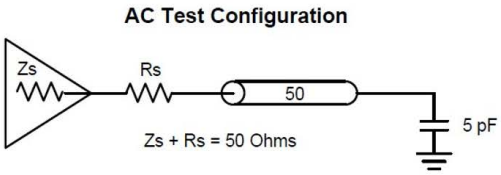
Table 12. Si5360 LVCMOS Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider[1]	0.008	—	250	MHz
		NA or NB divider[2]	0.008	—	250	MHz
Duty cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	45	—	55	%
Output voltage high[3]	V_{OH}	VDDO = 3.3 V/2.5 V/1.8 V IOH= –8/–6/–4 mA IOL = 8/6/4 mA	V_{DDO} x 0.85	—	—	V
Output voltage low[3]	V_{OL}		—	—	V_{DDO}x0.15	V
Rise and fall times (20% to 80%)[4, 5]	t_r/t_f	LVCMOS	0.35	0.8	1.35	ns
		SRL LVCMOS 4 ns rise/fall[5]	3	4	6	ns
		SRL LVCMOS 6.5 ns rise/fall[5]	4	6.5	10	ns
		SRL LVCMOS 13 ns rise/fall[5]	7	13	24	ns
		SRL LVCMOS 25 ns rise/fall[5]	13	25	42	ns

1. Q dividers support output frequencies within the specified range equal to fVCO/Q where Q is an integer.
2. NA, NB Multisynths support any output frequency within the specified range.
3. V_{OL}/V_{OH} is measured at I_{OL}/I_{OH} as shown in the DC Test Configuration.
4. A 15 to 25 Ω series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed as shown in the AC Test Configuration.





5. Slew rate limited (SRL) LVCMOS format only available on OUT16/OUT17.

Table 13. Si5360 Output Status Pin Specifications

V_{DDIO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low-Power Mode: V_{DDIO} = 1.8 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Status Output Pins (GPIO, SDA)						
Output voltage high[1]	VOH	IOH = –2 mA	VDDIO x 0.85	—	—	V
Output voltage low	VOL	IOL = 2 mA	—	—	VDDIO x 0.15	V

1. The VOH specification does not apply to the open-drain SDA output when the serial interface is in I^2C mode. VOL remains valid in all cases.

Table 14. Si5360 I^2C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	—	100	—	400	kHz
SMBus timeout	—	25	35	25	35	ms
Hold time (Repeated) START condition	$t_{HD:STA}$	4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$	100	—	100	—	ns
Data setup time	$t_{SU:DAT}$	250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f	—	300	—	300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$	—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$	—	3.45	—	0.9	µs

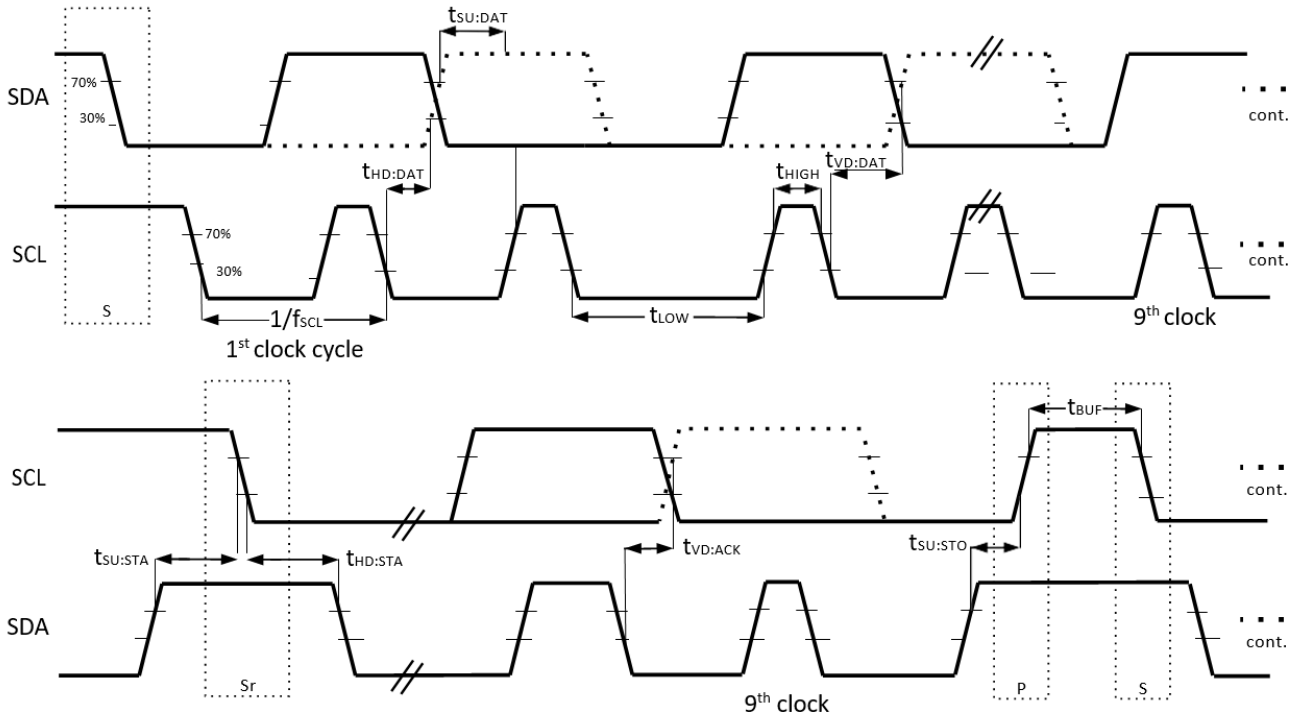


Figure 7. I²C Serial Port Timing Standard and Fast Modes

Table 15. Si5360 SPI Timing Specifications (4-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	TS_{U2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

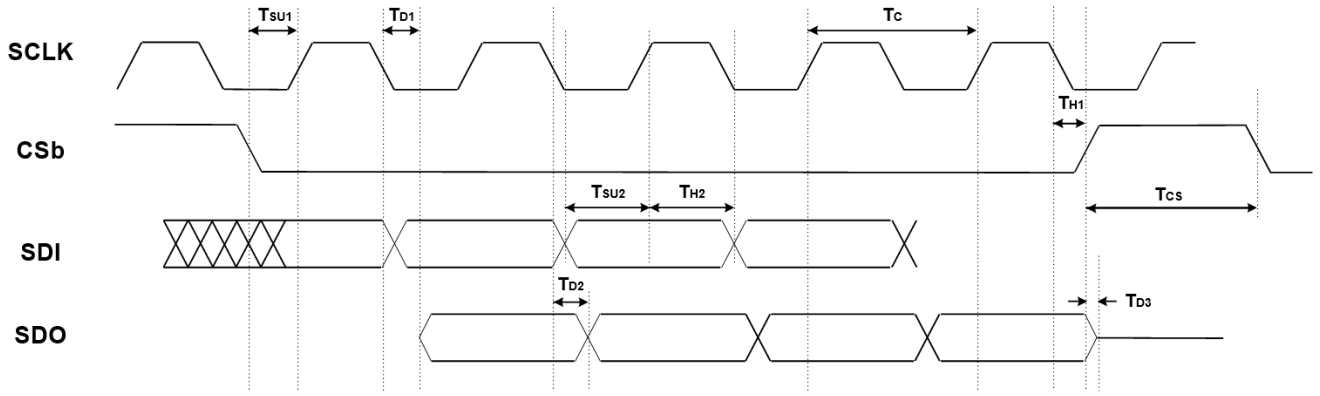


Figure 8. 4-Wire SPI Serial Interface Timing

Table 16. SPI Timing Specifications (3-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.33	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

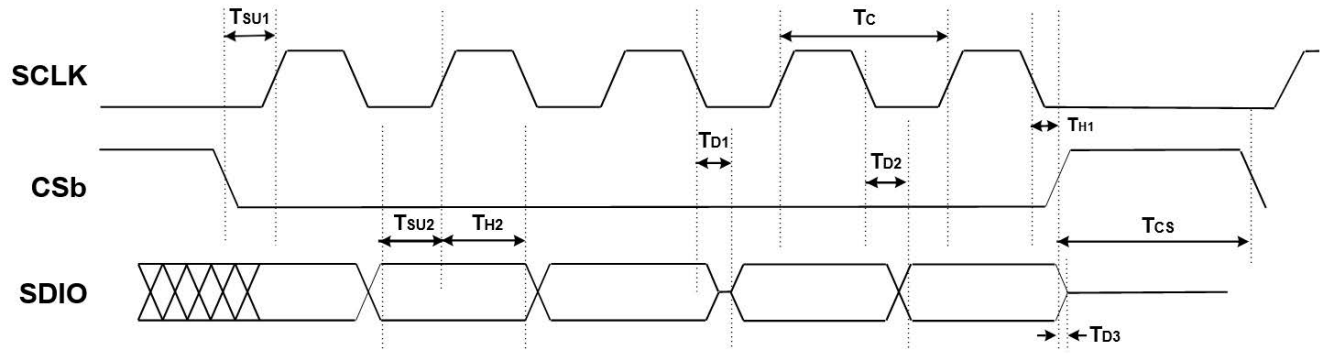


Figure 9. 3-Wire SPI Serial Interface Timing

4. Typical Operating Characteristics

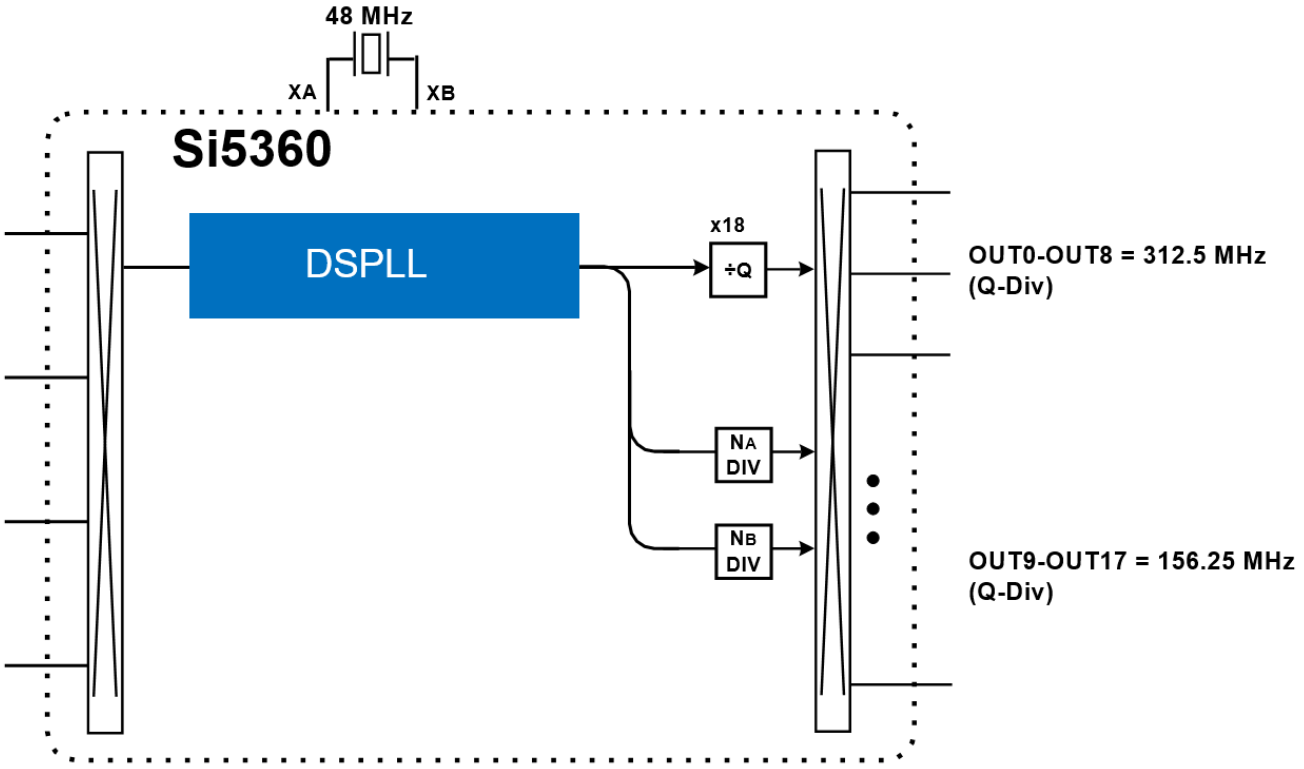


Figure 10. Si5360 Typical Operating Circuit

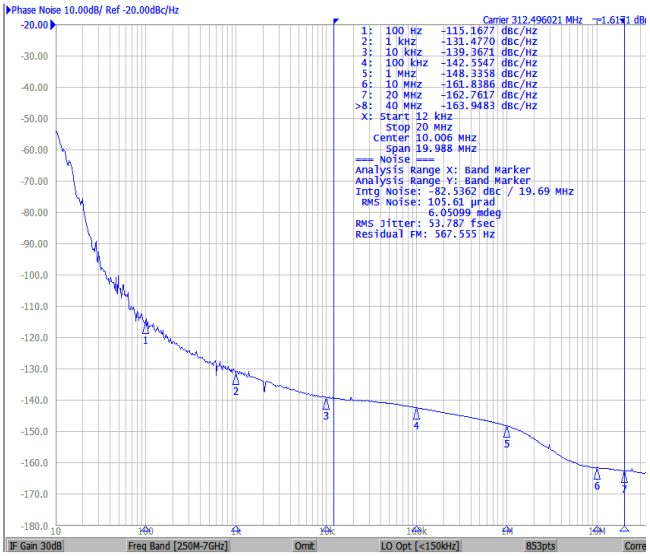


Figure 11. 53.7 fs RMS Jitter for SyncE 312.5 MHz

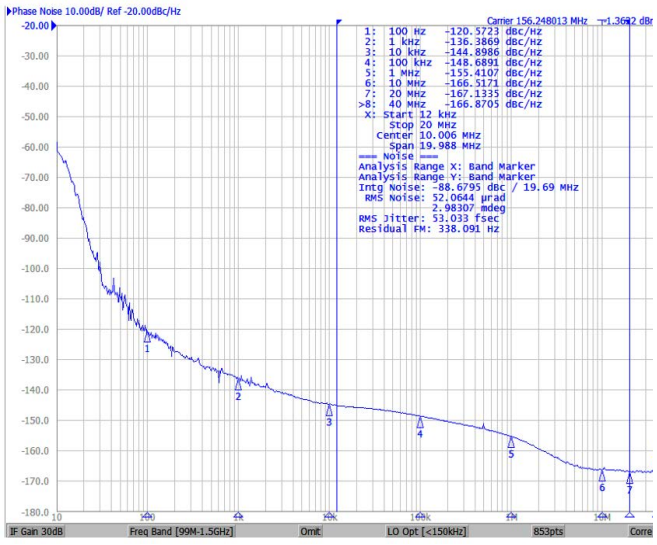


Figure 12. 53 fs RMS Jitter for SyncE 156.25 MHz

5. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si5360 can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

5.1. Package Outline

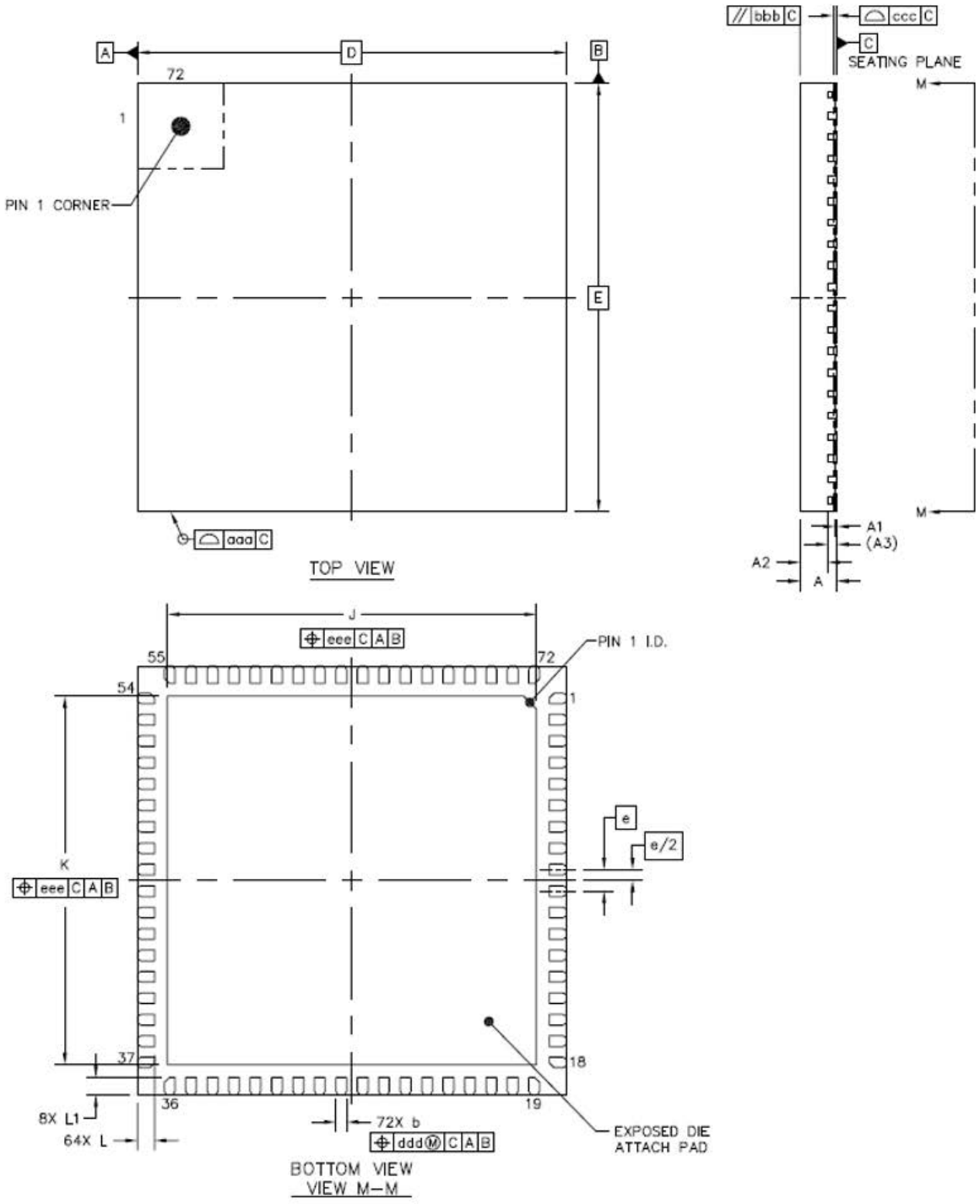


Figure 13. 72-Pin QFN Package

Table 17. Package Dimensions[1, 2, 3]

		Symbol	Min	Typ	Max
Total thickness		A	0.8	0.85	0.9
Stand off		A1	0	0.035	0.05
Mold thickness		A2	–	0.65	–
L/F thickness		A3		0.203 REF	
Lead width		b	0.2	0.25	0.3
Body size	X	D		10 BSC	
	Y	E		10 BSC	
Lead pitch		e		0.5 BSC	
EP size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead offset		ddd		0.1	
Exposed pad offset		eee		0.1	
Weight		N/A	—	0.35 g	—

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220

5.2. PCB Land Pattern

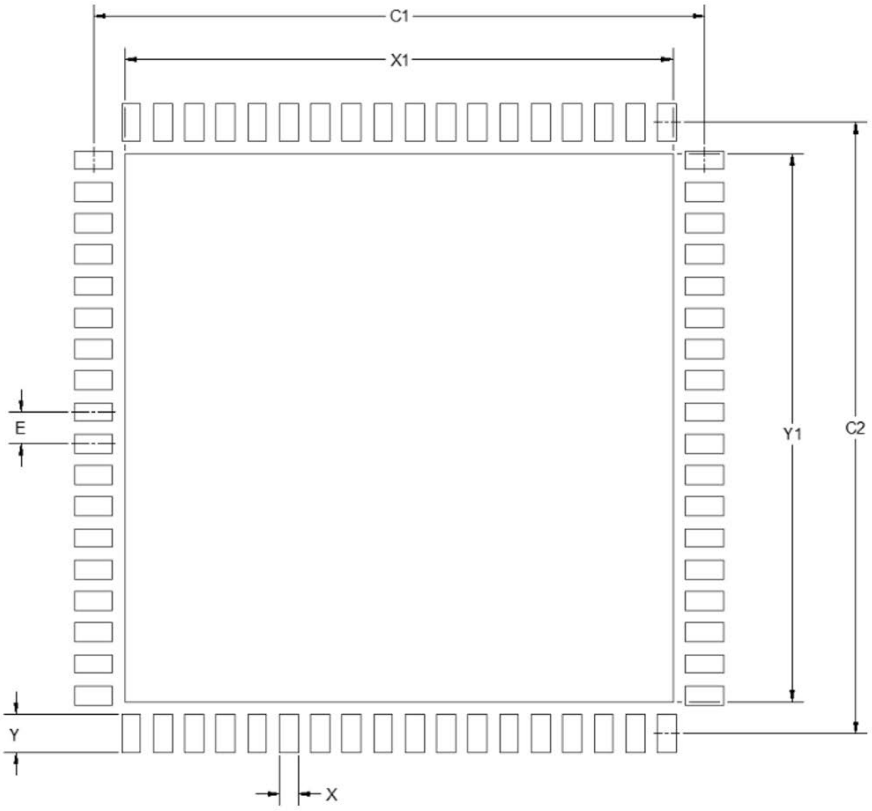


Figure 14. Si5360 PCB Land Pattern

Table 18. Land Pattern Dimensions

Dimension	mm	Notes
C1	9.70	**General** 1. All dimensions shown are in millimeters (mm). 2. This land pattern design is based on the IPC-7351 guidelines. 3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all pads. 4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components. *Above notes and stencil design are recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.
C2	9.70	
E	0.50	
X	0.30	
Y	0.60	
X1	8.70	
Y1	8.70	

5.3. Package Marking: 72-Pin QFN Package

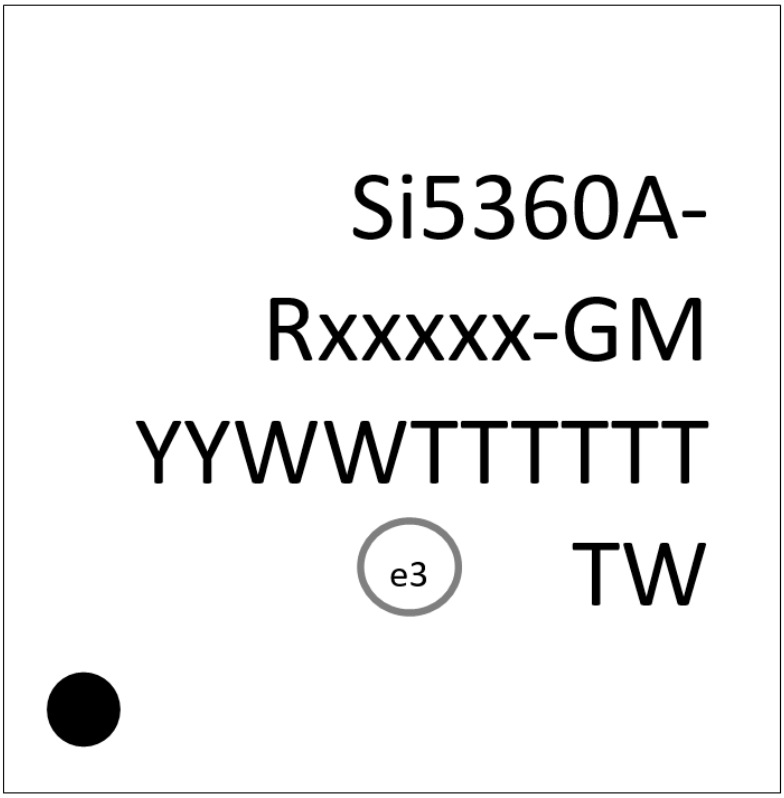


Figure 15. Si5360 Typical Package Marking

Line	Characters	Description
1	Si5360A-	Base part number and device grade A = Device grade.
2	Rxxxxx-GM	R = Product revision. xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. -GM = Package (QFN) and temperature range (–40 to +95 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 0.6 mm (72-QFN) diameter	Pin 1 indicator, left-justified
	e3 TW	Pb-free symbol, center-justified TW = Taiwan, country of origin (ISO abbreviation)

6. Ordering Information

Ordering Part Number (OPN)	Frequency Synthesis Mode	Number of Outputs	Max Differential Output Frequency	Package	Temperature Range
Si5360A-Axxxxx-GM	Integer and fractional	18	1300 MHz	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board
Si5360B-Axxxxx-GM	Integer and fractional	18	350 MHz	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board
Si5360C-Axxxxx-GM	Integer only	18	1300 MHz	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board
Si5360D-Axxxxx-GM	Integer only	18	350 MHz	72-Lead QFN 10 x 10 mm	–40 to 95 °C ambient –40 to 105 °C board
Si5360-A-EVB	—	18	1300 MHz	Evaluation board	—

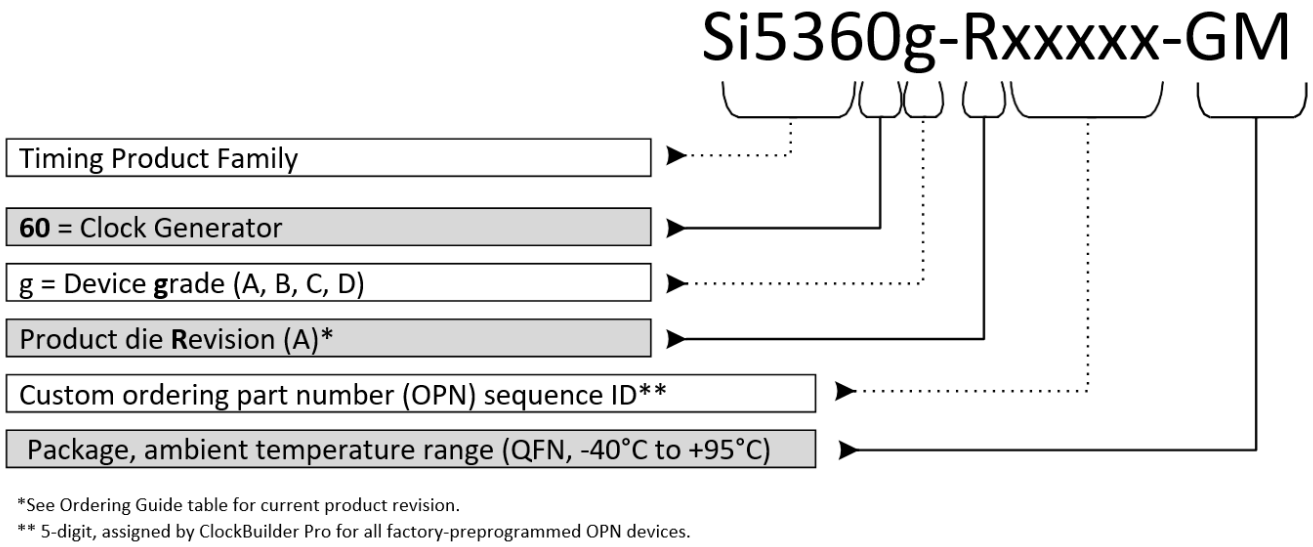


Figure 16. Ordering Guide

7. Revision History

Revision	Date	Description	Notes
A	August 16, 2023	Initial release.	