DATA SHEET

# Si86Px: Dual and Quad Digital Isolators with Integrated Power

## Applications

- Industrial automation systems
- Isolated switch mode supplies
- Inverters
- Data acquisition
- Motor control
- PLCs, distributed control systems

## Features

- High-speed isolators with integrated isolated power
- Fully integrated hysteretic control converter with frequency dithering for reduced EMI
- DC-DC converter peak efficiency up to 43%
- Isolated power output up to 0.5 W
- Standard voltage conversion:
  - 3.3 V/5 V input to isolated 3.3 V/5 V output
- Precise timing performance on digital isolators:
  - Data rates from 0 to 150 Mbps
  - 15 ns max propagation delay
- High electromagnetic immunity and low emissions
- RoHS-compliant package options:
  - WB SOIC-16 and WB SOIC-20
- Up to 3.75 $kV_{RMS}$ isolation rating
- High transient immunity of 100 kV/µs (minimum)
- WB SOIC-16 package MSL rating 3
- WB SOIC-20 package MSL rating 3
- Wide operating temperature range: –40 to +125 °C
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

## Safety Regulatory Approvals (Pending)

- UL recognized
  - 1577 (3750 $V_{RMS}$ for one minute)
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (basic insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

## Description

The Si86Px family integrates proven Skyworks digital isolation technology with an integrated isolated dc-dc converter and matched miniature transformer, delivering a complete solution for both signal and power isolation.

Utilizing a stable hysteretic control methodology, the converter achieves excellent output regulation across voltages from 3.3 to 5.0 V, with peak output power up to 0.5 W.

These devices support up to four digital isolation channels, offering significant advantages in data rate, propagation delay, size, and reliability compared to legacy isolation technologies. They support data rates up to 150 Mbps and feature a maximum propagation delay of 15 ns.

Ordering options include configurations with two or four signal isolation channels, with various channel arrangements available. All products are certified by UL, CSA, VDE, and CQC.

## 1. Functional Block Diagrams

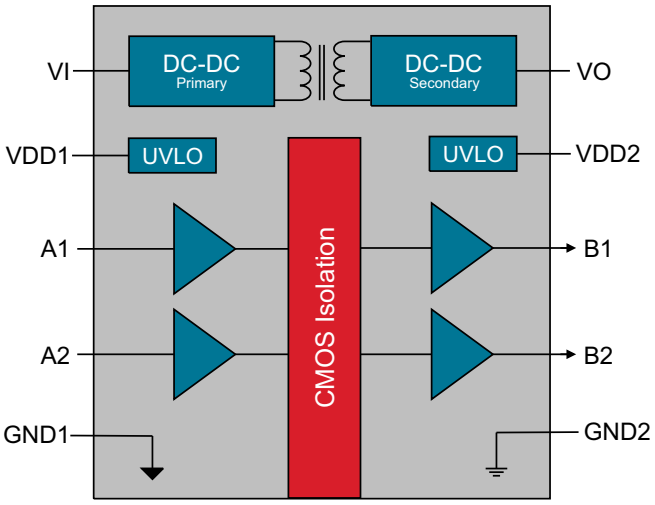



**Figure 1. Si86Px20x**

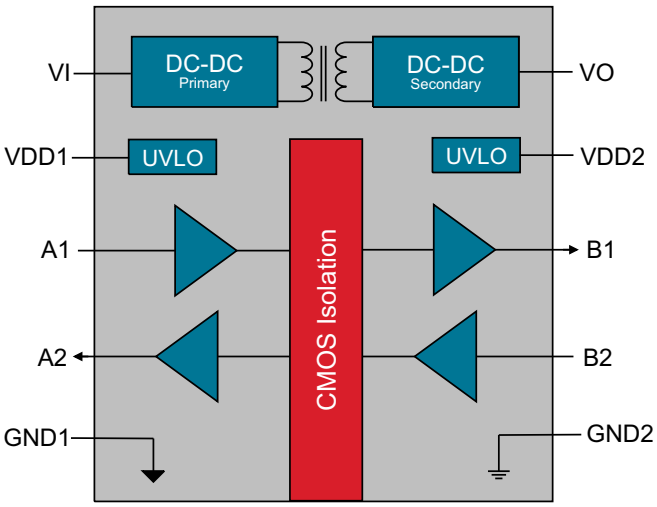



**Figure 2. Si86Px21x**

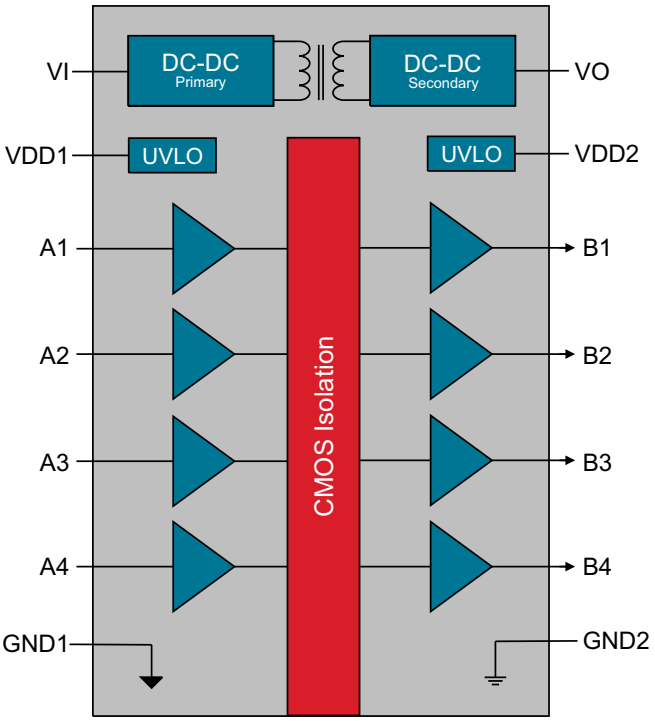



**Figure 3. Si86Px40x**

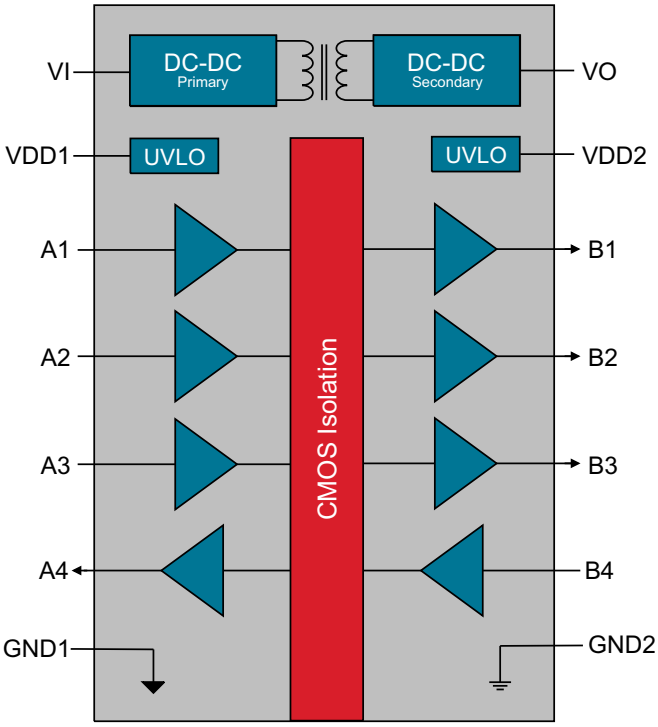



**Figure 4. Si86Px41x**

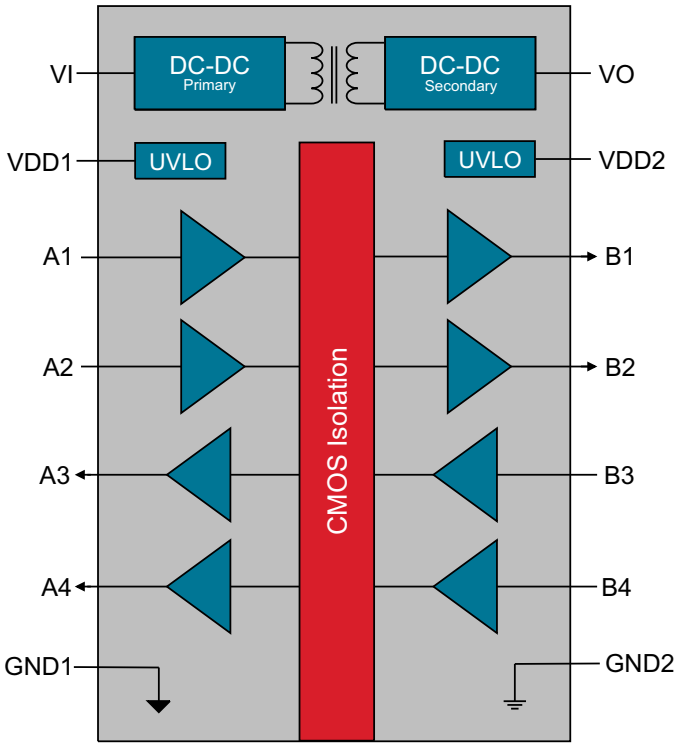



**Figure 5. Si86Px42x**

# 2. Pin Descriptions

## 2.1. WB SOIC-16

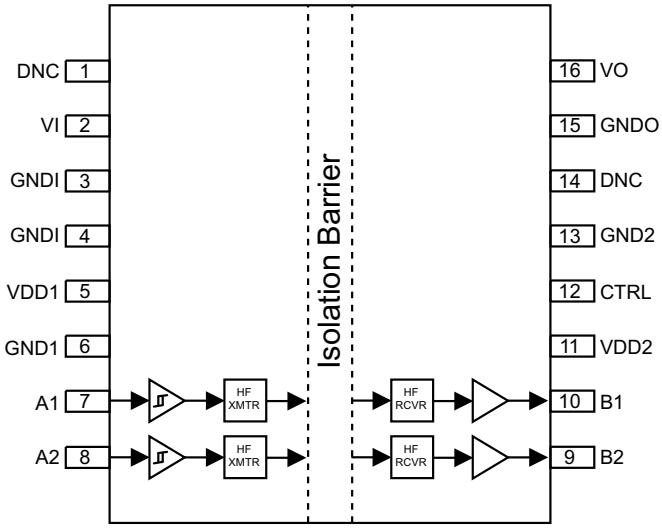



**Figure 6. Si86P320x/420x/520x**

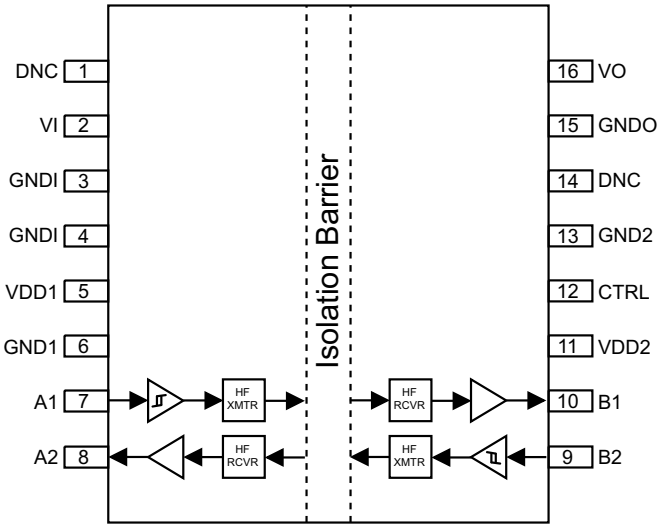



**Figure 7. Si86P321x/421x/521x**

**Table 1. WB SOIC-16 Pin Descriptions**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | DNC | Do not connect |
| 2 | VI | Power supply for integrated power |
| 3 | GNDI | Integrated power primary side ground |
| 4 | GNDI | Integrated power primary side ground |
| 5 | VDD1 | Primary side signal power supply |
| 6 | GND1 | Primary side signal ground |
| 7 | A1 | Signal channel 1 on the VDD1 side |
| 8 | A2 | Signal channel 2 on the VDD1 side |
| 9 | B2 | Signal channel 2 on the VDD2 side |
| 10 | B1 | Signal channel 1 on the VDD2 side |
| 11 | VDD2 | Secondary side signal power supply |
| 12 | CTRL | Output voltage control input |
| 13 | GND2 | Secondary side signal ground |
| 14 | DNC | Do not connect |
| 15 | GNDO | Integrated power secondary side ground |
| 16 | VO | Integrated power output |

## 2.2. WB SOIC-20

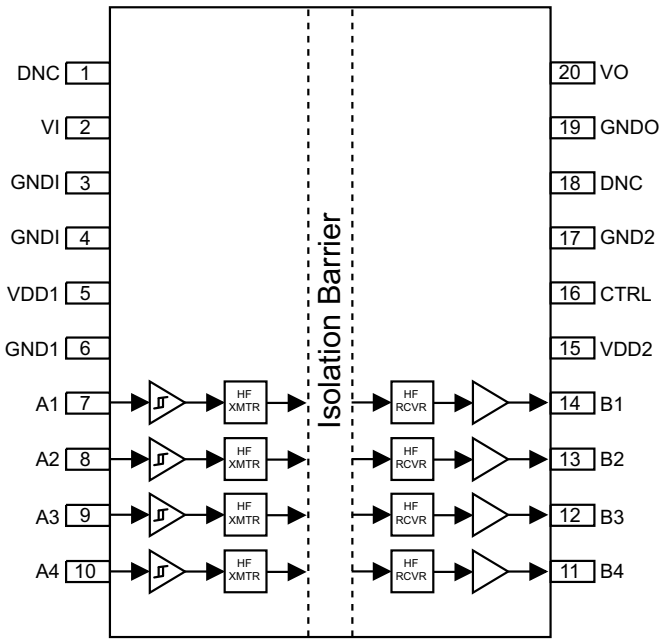



**Figure 8. Si86P340x/440x/540x**

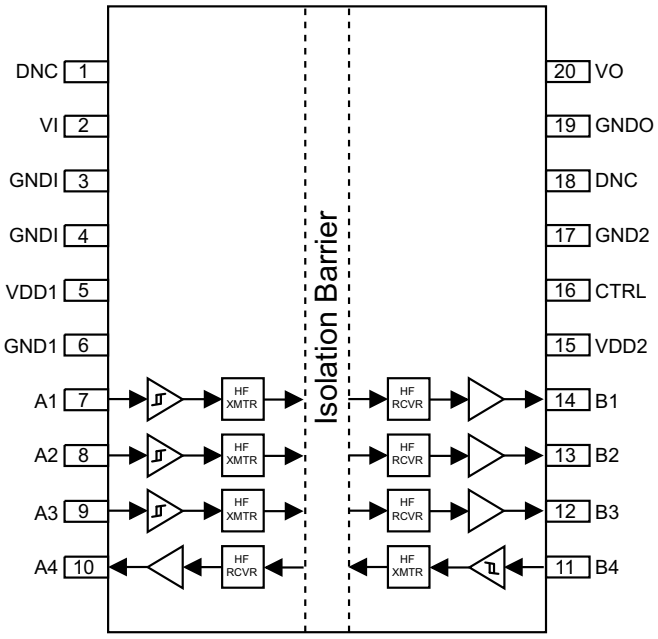



**Figure 9. Si86P341x/441x/541x**

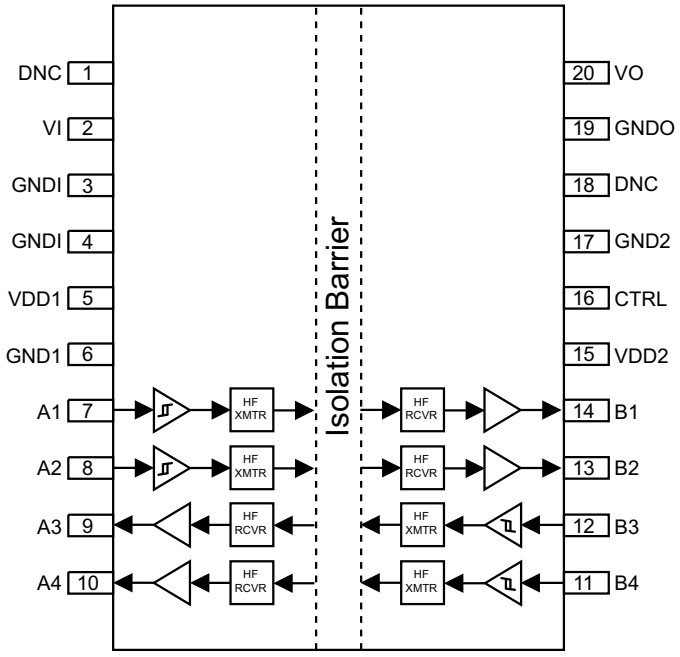



**Figure 10. Si86P342x/442x/542x**

**Table 2. WB SOIC-20 Pin Descriptions**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | DNC | Do not connect |
| 2 | VI | Power supply for integrated power |
| 3 | GNDI | Integrated power primary side ground |
| 4 | GNDI | Integrated power primary side ground |
| 5 | VDD1 | Primary side signal power supply |
| 6 | GND1 | Primary side signal ground |
| 7 | A1 | Signal channel 1 on the VDD1 side |
| 8 | A2 | Signal channel 2 on the VDD1 side |
| 9 | A3 | Signal channel 3 on the VDD1 side |
| 10 | A4 | Signal channel 4 on the VDD1 side |
| 11 | B4 | Signal channel 4 on the VDD1 side |
| 12 | B3 | Signal channel 3 on the VDD1 side |
| 13 | B2 | Signal channel 2 on the VDD1 side |
| 14 | B1 | Signal channel 1 on the VDD2 side |
| 15 | VDD2 | Secondary-side signal power supply |
| 16 | CTRL | Output voltage control input |
| 17 | GND2 | Secondary-side signal ground |
| 18 | DNC | Do not connect |
| 19 | GNDO | Integrated power secondary side ground |
| 20 | VO | Integrated power output |

# 3. Functional Description

## 3.1. Digital Isolation

The Si86Px series can transfer digital data signals between power domains with up to 3.75 $kV_{RMS}$ of isolation. Additionally, Si86Px products feature a fully integrated power transfer solution, including a dc-dc converter and a miniature transformer that regulates output voltage by sensing it on the isolated side.

A simplified block diagram for a single Si86Px channel is shown in Figure 11 below. The operation of an Si86Px digital channel is analogous to that of a digital buffer, except an RF carrier transmits data across the isolation barrier. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up.

A channel consists of an RF transmitter and RF receiver separated by a silicon dioxide capacitive isolation barrier.

In the transmitter, the input signal modulates the carrier provided by an RF oscillator using on/off keying.

The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to the output via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 12 on page 8 for modulation scheme details.

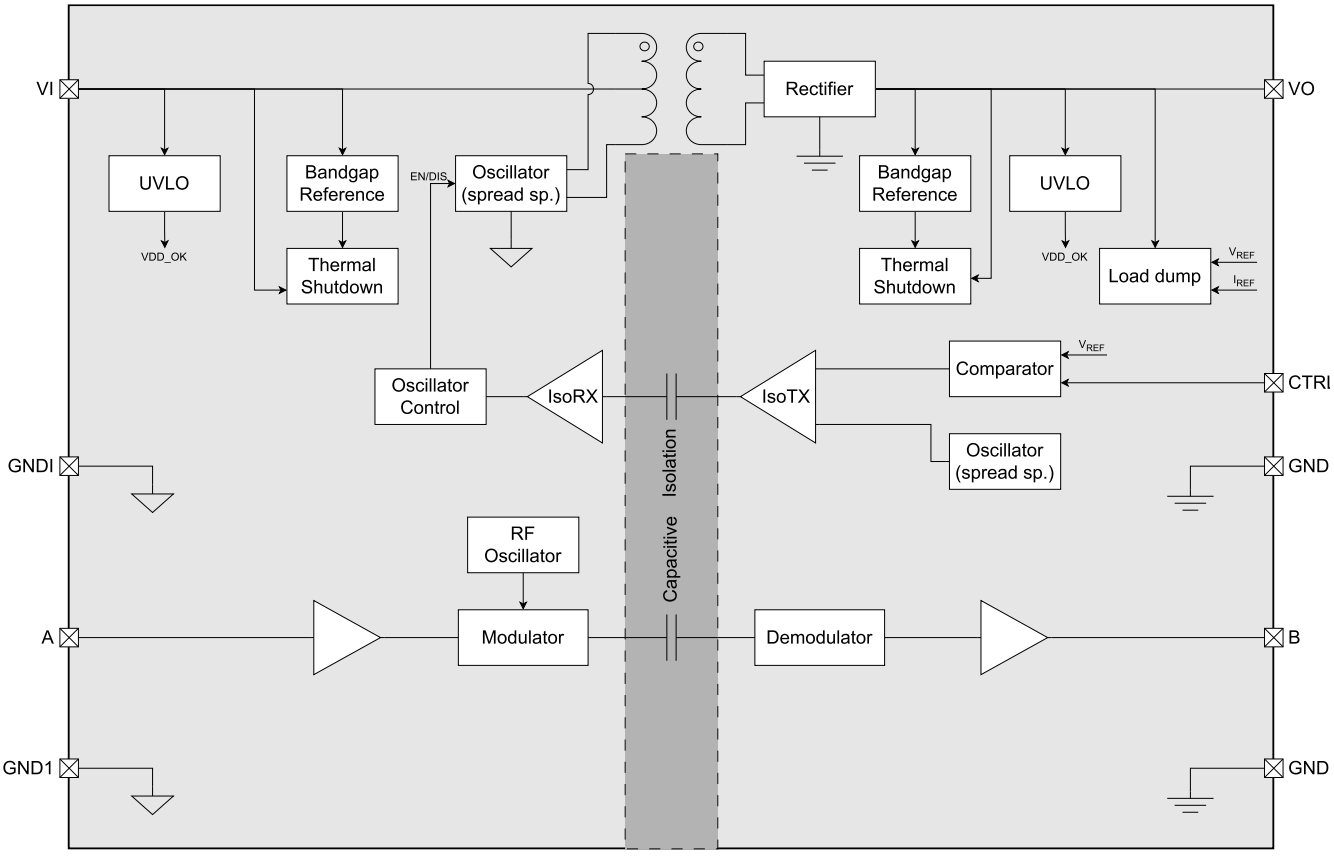



**Figure 11. Si86Px Power and Signal Isolation Block Diagram**

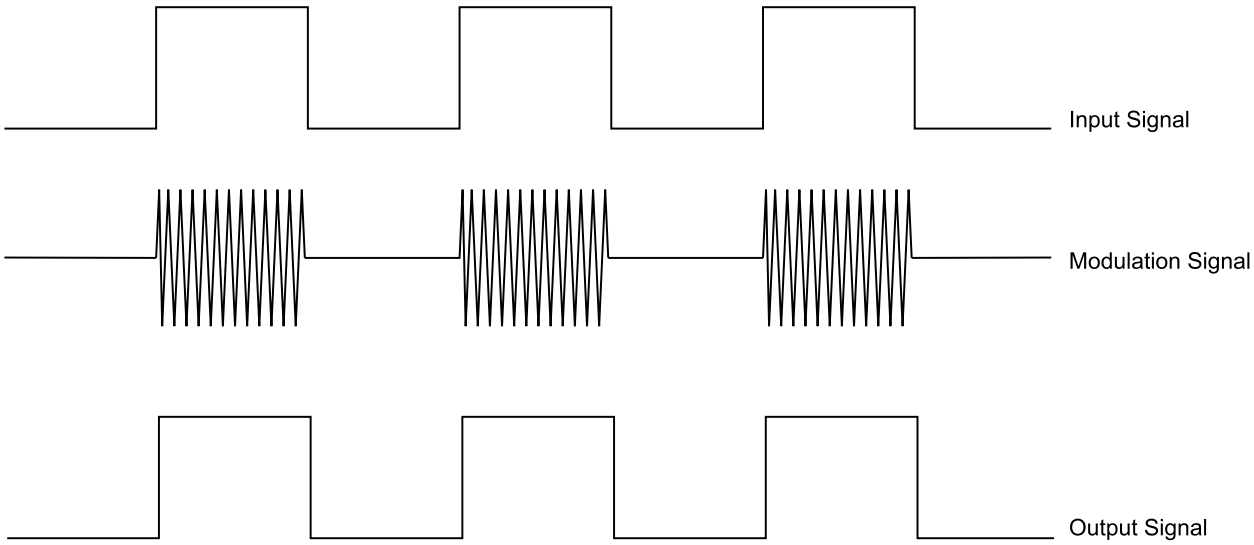



**Figure 12. Modulation Scheme**

## 3.2. Power Isolation

Figure 13. “Isolated Power Transfer” below illustrates the concept behind the isolated power transfer system, which consists of three main parts described below.

### 3.2.1. DC-to-AC Conversion

The dc-to-ac conversion is performed by the NMOS cross-coupled pair and an LC tank. This pair on the primary side (input voltage domain) enables the LC tank to oscillate in near Class-D mode, pumping energy into the LC tank at a frequency determined by the system passive components. The primary-side transformer winding can experience voltages up to 3 x VI due to the near Class-D mode operation of the oscillator.

The oscillation can be turned on or off by means of switches that cut off the current path to the transformer.

The Class-D operation of the oscillator provides zero cross switching, enhancing efficiency by limiting the time the NMOS devices can dissipate a high amount of power.

The oscillator on/off control requires a means of preventing instant discharges of the transformer windings and the resulting high voltages at the transformer terminals. Snubber clamps are included to protect the device by providing a discharge path for node voltages exceeding device limitations.

### 3.2.2. AC-to-AC Conversion

The ac-to-ac conversion utilizes an air-core transformer with a 1:N turns ratio (where N is approximately 1) to convert ac electrical energy into magnetic flux, which is then coupled to the secondary side (output voltage domain) and converted back to electrical energy. The transformer provides 3.75 $kV_{RMS}$ isolation while transferring energy between the primary-to-secondary voltage domains.

### 3.2.3. AC-to-DC Conversion

The ac-to-dc conversion is achieved by means of an on-chip, full-wave rectifier using Schottky diodes in conjunction with cross-coupled NMOS devices. This improves power transfer efficiency as the voltage drop across the NMOS devices can be much lower than the forward voltage of the Schottky diodes.

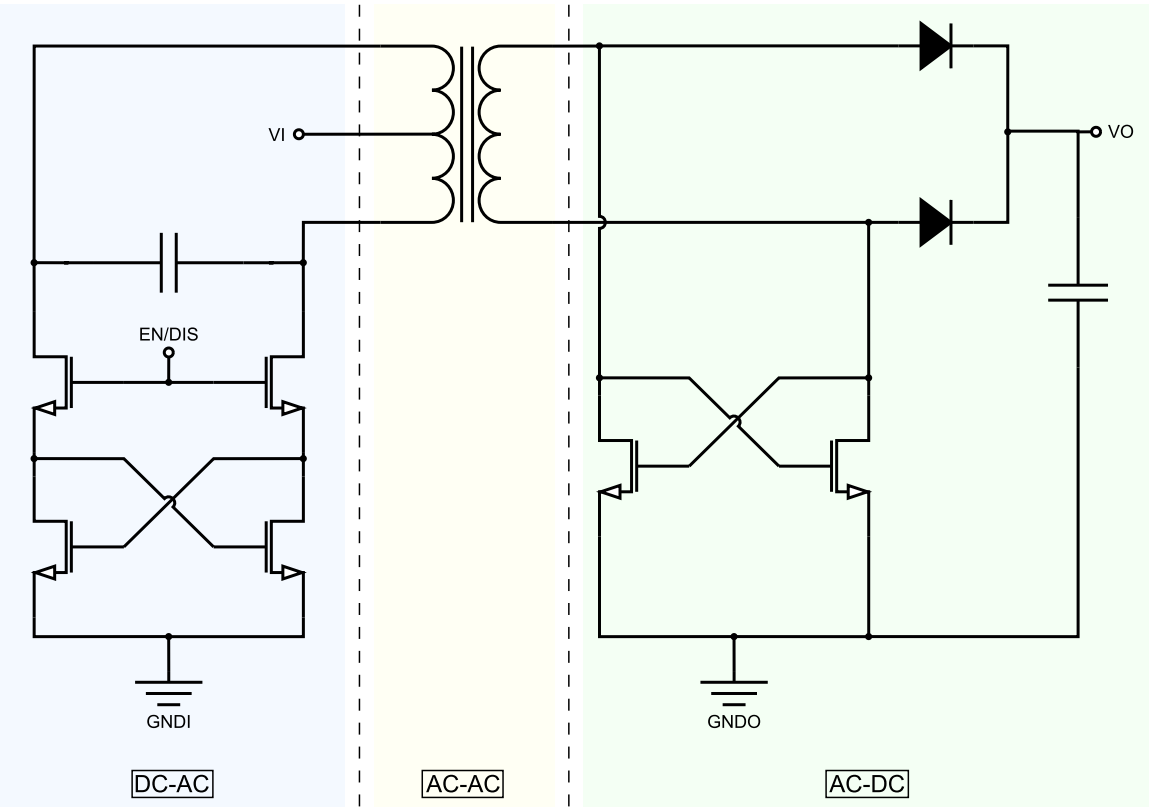



**Figure 13. Isolated Power Transfer**

# 4. Digital Isolator Device Operation

This section describes the capabilities of the device and how it should be used to achieve different goals within a design. Refer to 6.1. “Recommended Application Circuits” and 8. “Ordering Information” for information on each device and how they are best utilized for different applications.

## 4.1. Logic Operation

Table 3 below describes the signal isolation behavior of the Si86Px under various input conditions and power supply states.

**Table 3. Si86Px Truth Table**

| Input | Power Supply State[1,2,3] | | Output | Comments |
|---|---|---|---|---|
| $VA_n$ | VDD1 | VDD2 | $VB_n$ | |
| H | P | P | H | Normal operation. |
| L | P | P | L | |
| X | UP | UP | Undetermined | VDD1 being unpowered results in VDD2 being unpowered. |
| X | P | UP | Undetermined | This is only a transitory condition as VDD2 powers up after the startup time has elapsed, at which point, $VB_n$ returns to the same state as $VA_n$. |

1. VDD1 and VDD2 are the input and output power supplies for the signal isolation channels. VDD2 is intended to be powered exclusively by VO and should not be driven by any external supply independent of the Si86Px device. VO serves as the integrated, isolated power output supply derived from the input supply VI. In the table above, VAn and VBn refer to the input and output signals at the respective isolator channels terminals.
2. “UP” is the “unpowered” state and “P” is the “powered” state. When VDD1 is powered, VDD2 is also powered unless there is a fault. If VDD1 is not powered, VDD2 is explicitly assumed to be in the “unpowered” state.
3. An I/O can power the die for a given side through an internal diode if its source has adequate current. This situation should be avoided. We recommend that I/Os not be driven high when primary side supply is turned off.

## 4.2. Device Startup

Outputs are held low during power up until VDDx is above the UVLO threshold for time period $t_{SU}$. Following this, the outputs follow the states of inputs. See 5.7. “Typical Performance Characteristics” for power converter and digital isolator startup sequence.

## 4.3. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDx is below its specified operating circuits range. Both sides of the isolation barrier have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when VDD1 falls below $VDD_{UV-}$ and exits UVLO when VDD1 rises above $VDD_{UV+}$. Side B operates the same as Side A with respect to its VDD2 supply.

## 4.4. Thermal Protection

The Si86Px integrates internal temperature sensors to safeguard against excessive junction temperatures caused by elevated ambient conditions or external component failures.

- **Protection Scope**
  Thermal shutdown is implemented exclusively on the power transfer circuitry. The digital isolator section does not include thermal shutdown functionality.
- **Shutdown Behavior**
  - If the input-side power circuitry exceeds its thermal threshold, its power oscillator is immediately disabled.
  - If the output-side circuitry overheats, a disable signal is transmitted across the isolation barrier to shut down the input-side oscillator.
- **System-Level Safety**
  This bidirectional shutdown mechanism ensures safe operation under thermal stress by halting power transfer across the isolation barrier when critical temperatures are detected.

## 4.5. Fault Tolerance and Protection

### 4.5.1. Overload/Short Circuit Protection

The cross-coupled NMOS and LC-tank-based oscillator on the primary side helps limit the peak current that could flow through the transformer. When the secondary side is shorted to ground, for example, the peak current limitation inherent in the architecture helps prevent excessive current draw from the supply. The system short circuit protection is mathematically described below:

$$Ipeak_{primary} = \frac{2 \times VDD}{2\Omega\, f_0 L(1-k^2) + R_s} \approx 316 \text{ mA peak for L } = 100 \text{ nH, k } = 0.6, (f_0 = 65\ MHz)$$

$$Ipeak_{secondary} = \frac{2 \times VDD}{2\Omega\, f_0 L(1-k^2) + R_s} \approx 200 \text{ mA peak for L } = 100 \text{ nH, k } = 0.6, (f_0 = 65\ MHz)$$

### 4.5.2. Time-Out Block

In certain fault scenarios on the secondary side (such as a load pulled to ground through low resistance), the feedback channel may become inactive. This can cause the primary-side oscillator to continually deliver power to the secondary side, leading to on-chip thermal buildup and reduced device reliability.

One example involves excessive junction heating on the secondary side, triggering thermal shutdown. However, if a CMTI event or fault prevents the shutdown signal from reaching the primary side, power transfer continues unchecked.

To mitigate this, a timeout circuit monitors the feedback channel for activity. If no transitions are detected within 10 ms, it disables the oscillator for 10 ms. This cycle repeats until the fault clears and feedback resumes, helping protect the primary-side components from prolonged stress.

### 4.5.3. Overvoltage Protection

The integrated power output pin (VO) supplies power to both internal circuitry and externally connected devices, making robust over-voltage protection essential for reliable operation. In the event of a fault that disrupts the feedback channel, the primary-side oscillator may remain active, causing VO to exceed its rated maximum and potentially damaging connected components.

To prevent such over-voltage stress, a load dump block is implemented on the secondary side. Operating as an active clamp, it sinks excess current to maintain the output voltage below VO + 10%. The clamp uses the same reference and sense voltage as the comparator (see Figure 61, “Hysteresis Implementation,” on page 40) ensuring precise operation and minimizing the chance of false activation.

# 5. Electrical Specifications

**Table 4. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Storage temperature | $T_{STG}$ | | –65 | 150 | °C |
| Operating temperature | $T_A$ | | –40 | 125 | °C |
| Junction temperature | $T_J$ | | — | 150 | °C |
| Power converter supply voltage | VI | | 3.135 | 6.000 | V |
| Power converter isolated supply voltage | VO | | 3.135 | 5.500 | V |
| Digital isolator supply voltage | VDD1, VDD2 | | –0.600 | 6.000 | V |
| Voltage on any pin with respect to ground[2] | $V_{IO}$ | | –0.500 | VDD + 0.500 | V |
| Output drive current per channel | $I_O$ | | –10 | 10 | mA |
| Lead solder temperature | | Duration = 10 s | — | 260 | °C |
| **ESD** | | | | | |
| Human body model | HBM | | –4 | 4 | kV |
| Charged device model | CDM | | –2 | 2 | kV |

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This parameter is not subject to production test. It is assured by characterization.

***ESD Handling**: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

## 5.1. Si86P5x: 5 V Supply Input and 3.3 to 5 V Continuous Supply Output

**Table 5. Power Converter (DC to DC) Characteristics—Si86P5x Devices**

Operating range for the following specifications with ± 5% supply variation:
VI = 5.0 V; VO = 5.0 V; $T_A$ = –40 to +125 °C with $T_A$ (typical) = 25 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input supply voltage | VI | | 4.750 | 5.000 | 5.250 | V |
| Output supply voltage | VO | | 3.135 | — | 5.250 | V |
| Output clamp voltage | VCLMP | | — | VO + 10% | - | V |
| Output supply current | IDDO | VI = 5.0 V; VO = 5.0 V | — | — | 100 | mA |
| | | VI = 5.0 V; VO = 3.3 V | — | — | 125 | mA |
| Average input short circuit current | $I_{I\_SC\_AVG}$ | VI = 5.0 V; VO shorted to GNDO | — | 117 | — | mA |
| Average output short circuit current | $I_{O\_SC\_AVG}$ | VI = 5.0 V; VO shorted to GNDO | — | 90 | — | mA |
| Peak efficiency | η | VI = 5.0 V; VO = 5.0 V | — | 43 | — | % |
| | | VI = 5.0 V; VO = 3.3 V | — | 34 | — | % |
| Switching frequency | $f_{SW}$ | | — | 70 | — | MHz |
| Line regulation | Line regulation | VI = 4.75 to 5.25 V; IDDO = 100 mA<br>(ΔVO (Line)/ΔVI) | — | 5 | — | mV/V |
| Load regulation | % Load regulation | IDDO = 0 to 100 mA<br>(ΔVO (Load)/VO x 100%) | — | 0.1 | — | % |
| Output voltage ripple | | VI = 5.0 V; VO = 5.0 V; IDDO = 100 mA<br>$C_{OUT}$ = 0.1 µF, 1 µF, and 4.7 µF; BW = 20 MHz | — | 60 | — | $mV_{P-P}$ |
| | | VI = 5.0 V; VO = 3.3 V; IDDO = 125 mA<br>$C_{OUT}$ = 0.1 µF, 1 cF, and 4.7 µF; BW = 20 MHz | — | 40 | — | $mV_{P-P}$ |
| **Thermal Shutdown** | | | | | | |
| Shutdown temperature | $T_{Jsh}$ | | — | 160 | — | °C |
| Thermal hysteresis | $T_{shHYS}$ | | — | 15 | — | °C |

## 5.2. Si86P4x: 3.3 V to 5 V Continuous Supply Input and 3.3 V Supply Output

**Table 6. Power Converter (DC to DC) Characteristics—Si86P4x Devices**

Operating range for the following specifications with ±5% supply variation: VI = 3.3 V to 5.0 V; VO = 3.3 V; $T_A$ = –40 to +125 °C with $T_A$ (typical) = 25 °C.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input supply voltage | VI | | 3.135 | — | 5.250 | V |
| Output supply voltage | VO | | 3.135 | — | 3.465 | V |
| Output clamp voltage | VCLMP | | — | VO + 10% | — | V |
| Output supply current | IDDO | VI = 5.0 V; VO = 3.3 V | — | — | 125 | mA |
| | | VI = 4.0 V; VO = 3.3 V | — | — | 85 | mA |
| | | VI = 3.3 V; VO = 3.3 V | — | — | 60 | mA |
| Average input short-circuit current | $I_{I\_SC\_AVG}$ | VI = 5.0 V; VO shorted to GNDO | — | 110 | — | mA |
| | | VI = 3.3 V; VO shorted to GNDO | — | 72 | — | mA |
| Average output short-circuit current | $I_{O\_SC\_AVG}$ | VI = 5.0 V; VO shorted to GNDO | — | 90 | — | mA |
| | | VI = 3.3 V; VO shorted to GNDO | — | 55 | — | mA |
| Peak efficiency | η | VI = 5.0 V; VO = 3.3 V | — | 34 | — | % |
| | | VI = 4.0 V; VO = 3.3 V | — | 40 | — | % |
| | | VI = 3.3 V; VO = 3.3 V | — | 43 | — | % |
| Switching frequency | $f_{SW}$ | | — | 70 | — | MHz |
| Line regulation | Line regulation | VI = 3.3 to 5.0 V; IDDO = 60 mA (ΔVO (Line)/ΔVI) | — | 5 | — | mV/V |
| Load regulation | % load regulation | VI = 5.0 V; IDDO = 0 to 125 mA (ΔVO (Load)/VO x 100%) | — | 0.1 | — | % |
| | | VI = 3.3 V; IDDO = 0 to 60 mA (ΔVO (Load)/VO x 100%) | — | 0.1 | — | % |
| Output voltage ripple | $VO_{RIPPLE}$ | VI = 5.0 V; VO = 3.3 V; IDDO = 125 mA $C_{OUT}$ = 0.1 µF, 1 µF, and 4.7 µF; BW = 20 MHz | — | 40 | — | $mV_{P-P}$ |
| | | VI = 3.3 V; VO = 3.3 V; IDDO = 60 mA $C_{OUT}$ = 0.1 µF, 1 µF, and 4.7 µF; BW = 20 MHz | — | 40 | — | $mV_{P-P}$ |
| **Thermal Shutdown** | | | | | | |
| Shutdown temperature | $T_{Jsh}$ | | — | 160 | — | °C |
| Thermal hysteresis | $T_{shHYS}$ | | — | 15 | — | °C |

## 5.3. Si86P3x: 3.3 V Supply Input and 3.3 V Supply Output

**Table 7. Power Converter (DC to DC) Characteristics—Si86P3x Devices**

Operating range for the following specifications with ±5% supply variation:
VI = 3.3 V; VO = 3.3 V; $T_A$ = –40 to +125 °C with $T_A$ (typical) = 25 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input supply voltage | VI | | 3.135 | 3.300 | 3.465 | V |
| Output supply voltage | VO | | 3.135 | — | 3.465 | V |
| Output clamp voltage | VCLMP | | — | VO + 10% | — | V |
| Output supply current | IDDO | VI = 3.3 V; VO = 3.3 V | — | — | 60 | mA |
| Average input short-circuit current | II_SC_AVG | VI = 3.3 V; VO shorted to GNDO | — | 76 | — | mA |
| Average output short-circuit current | IO_SC_AVG | VI = 3.3 V; VO shorted to GNDO | — | 55 | — | mA |
| Peak efficiency | η | VO = 3.3 V | — | 43 | — | % |
| Switching frequency | $f_{SW}$ | | — | 70 | — | MHz |
| Line regulation | Line regulation | VI = 3.15 to 3.45 V; IDDO = 60 mA (ΔVO (Line)/ΔVI) | — | 10 | — | mV/V |
| Load regulation | % load regulation | VI = 3.3 V; IDDO = 0 to 60 mA (ΔVO (Load)/VO x 100%) | — | 0.1 | — | % |
| Output voltage ripple | $VO_{RIPPLE}$ | VI = 3.3 V; VO = 3.3 V; IDDO = 60 mA COUT = 0.1 µF, 1 µF, and 4.7 µF; BW = 20 MHz | — | 40 | — | $mV_{P-P}$ |
| **Thermal Shutdown** | | | | | | |
| Shutdown temperature | $T_{Jsh}$ | | — | 160 | — | °C |
| Thermal hysteresis | $T_{shHYS}$ | | — | 15 | — | °C |

## 5.4. Supply Input Current Characteristics

**Table 8. Supply Input Current Characteristics**

Operating range for the following specifications with ±5% supply variation:
VI = 5.0 V or 3.3 V; $T_A$ = –40 to +125 °C with $T_A$ (typical) = 25 °C.

| Parameter | Symbol | Test Condition | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input current consumption (Si86P5x devices) | IDD | VI = 5.0 V | VO = 5.0 V | IDDO = 0 mA | — | 15 | — | mA |
| | | | | IDDO = 50 mA | — | 126 | — | mA |
| | | | | IDDO = 100 mA | — | 234 | — | mA |
| | | VI = 5.0 V | VO = 3.3 V | IDDO = 0 mA | — | 14 | — | mA |
| | | | | IDDO = 62.5 mA | — | 130 | — | mA |
| | | | | IDDO = 125 mA | — | 243 | — | mA |
| Input current consumption (Si86P4x devices) | | VI = 5.0 V | VO = 3.3 V | IDDO = 0 mA | — | 15 | — | mA |
| | | | | IDDO = 62.5 mA | — | 134 | — | mA |
| | | | | IDDO = 125 mA | — | 241 | — | mA |
| | | VI = 3.3 V | VO = 3.3 V | IDDO = 0 mA | — | 14 | — | mA |
| | | | | IDDO = 30 mA | — | 78 | — | mA |
| | | | | IDDO = 60 mA | — | 140 | — | mA |
| Input current consumption (Si86P3x devices) | | VI = 3.3 V | VO = 3.3 V | IDDO = 0 mA | — | 14 | — | mA |
| | | | | IDDO = 30 mA | — | 78 | — | mA |
| | | | | IDDO = 60 mA | — | 140 | — | mA |

## 5.5. Electrical Characteristics—Digital Isolator

### 5.5.1. Logic Input and Output Characteristics

**Table 9. Logic Input and Output Characteristics**

Operating range for the following specifications with ±5% supply variation:
VDD1 = VDD2 = 3.3 V – 5.0 V; $T_A$ = –40 to +125 °C with $T_A$ (typical) = 25 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD1 undervoltage threshold | $VDD1_{UV+}$ | VDD1 rising | 2.70 | 2.82 | 3.10 | V |
| VDD1 undervoltage threshold | $VDD1_{UV–}$ | VDD1 falling | 2.32 | 2.54 | 2.75 | V |
| VDD2 undervoltage threshold | $VDD2_{UV+}$ | VDD2 rising | 2.40 | 2.67 | 2.90 | V |
| VDD2 undervoltage threshold | $VDD2_{UV–}$ | VDD2 falling | 2.27 | 2.47 | 2.64 | V |
| VDD1 undervoltage hysteresis | $VDD1_{HYS}$ | | 314 | 370 | 420 | mV |
| VDD2 undervoltage hysteresis | $VDD2_{HYS}$ | | 150 | 190 | 228 | mV |
| Logic high input voltage | $V_{IH}$ | | 0.7 x VDDx | — | — | V |
| Logic low input voltage | $V_{IL}$ | | — | — | 0.3 x VDDx | V |
| Logic input hysteresis | $V_{HYS}$ | | 0.15 x VDDx | — | — | V |
| Logic high output voltage | $V_{OH}$ | $I_{OH}$ = –4 mA | VDD1 – 0.4,<br>VDD2 – 0.4 | — | — | V |
| Logic low output voltage | $V_{OL}$ | $I_{OL}$ = 4 mA | — | — | 0.4 | V |
| Input leakage current | $I_L$ | | –10 | — | +10 | µA |
| Input capacitance[1] | $C_I$ | $V_{TEST}$ = 0.1 $V_{RMS}$, $f_{TEST}$ = 1 MHz | — | 3.6 | — | pF |
| Input to output capacitance[2] | $C_{IO}$ | $V_{TEST}$ = 0.1 $V_{RMS}$, $f_{TEST}$ = 1 MHz | — | 4.3 | — | pF |
| Output impedance | $Z_O$ | | — | 50 | — | Ω |

1. Measured from digital input to ground.
2. Pins on the primary side are shorted together to form the first terminal and pins on the secondary side are shorted together to form the second terminal. The parameters are then measured between these two terminals.

## 5.5.2. Supply Current Characteristics

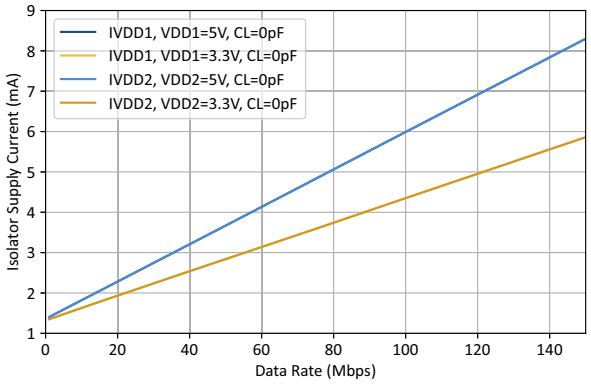



**Figure 14. Isolator Supply Current vs. Data Rate in 1 Forward/1 Reverse Configuration, $C_L$ = 0 pF**

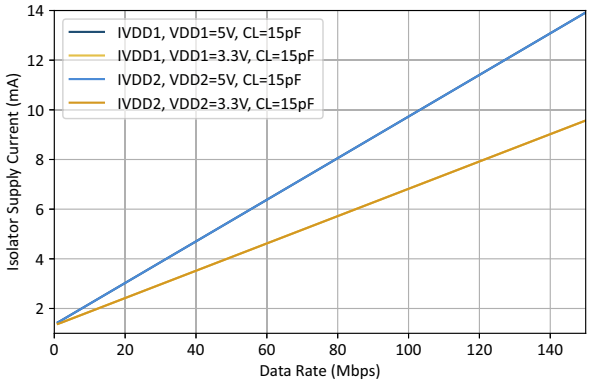



**Figure 15. Isolator Supply Current vs. Data Rate in 1 Forward/1 Reverse Configuration, $C_L$ = 15 pF**

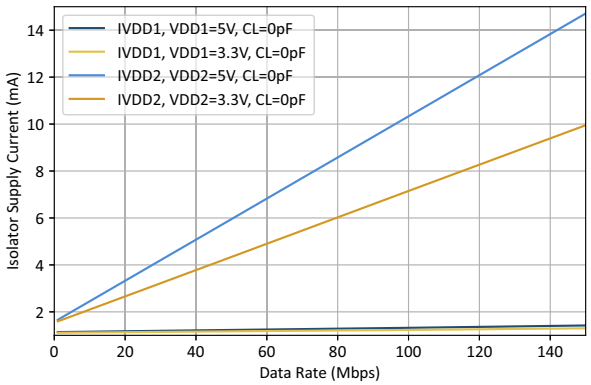



**Figure 16. Isolator Supply Current vs. Data Rate in 2 Forward/0 Reverse Configuration, $C_L$ = 0 pF**

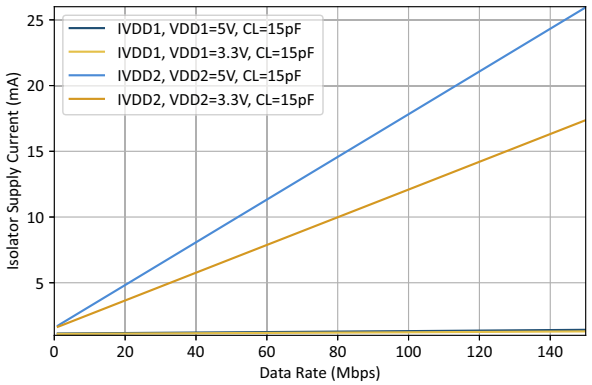



**Figure 17. Isolator Supply Current vs. Data Rate in 2 Forward/0 Reverse Configuration, $C_L$ = 15 pF**

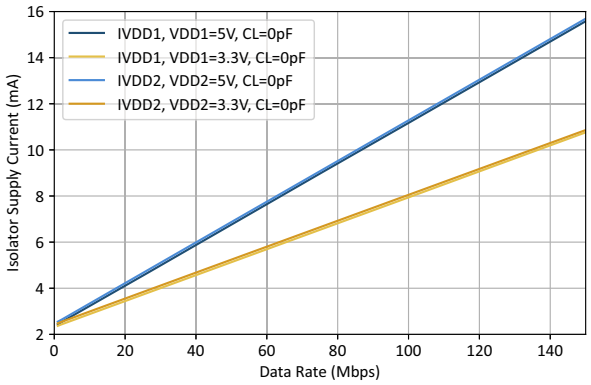



**Figure 18. Isolator Supply Current vs. Data Rate in 2 Forward/2 Reverse Configuration, $C_L$ = 0 pF**

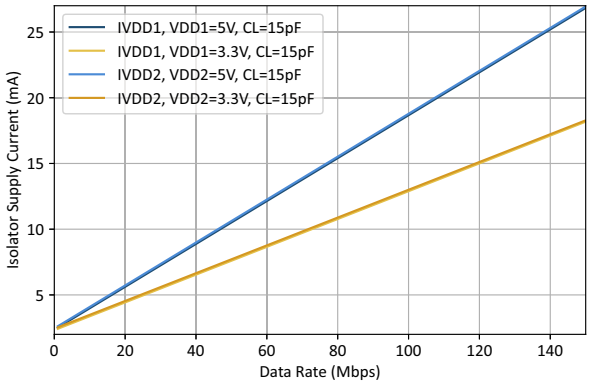



**Figure 19. Isolator Supply Current vs. Data Rate in 2 Forward/2 Reverse Configuration, $C_L$ = 15 pF**

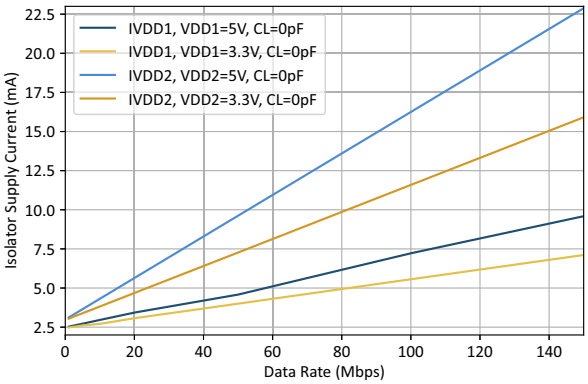



**Figure 20. Isolator Supply Current vs. Data Rate in 3 Forward/1 Reverse Configuration, $C_L$ = 0 pF**

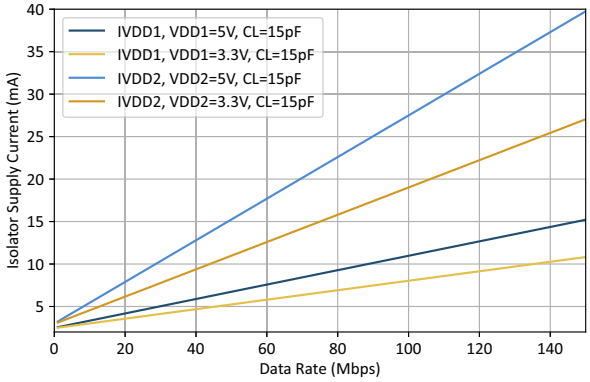



**Figure 21. Isolator Supply Current vs. Data Rate in 3 Forward/1 Reverse Configuration, $C_L$ = 15 pF**

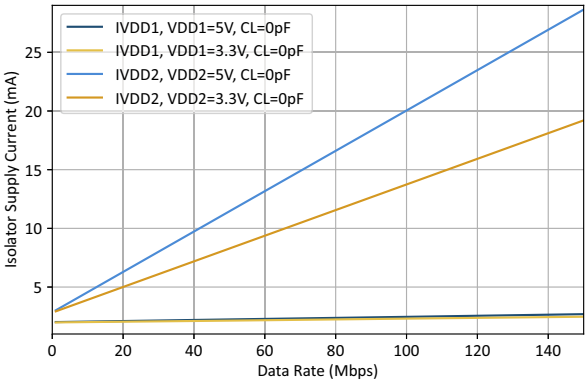



**Figure 22. Isolator Supply Current vs. Data Rate in 4 Forward/0 Reverse Configuration, $C_L$ = 0 pF**

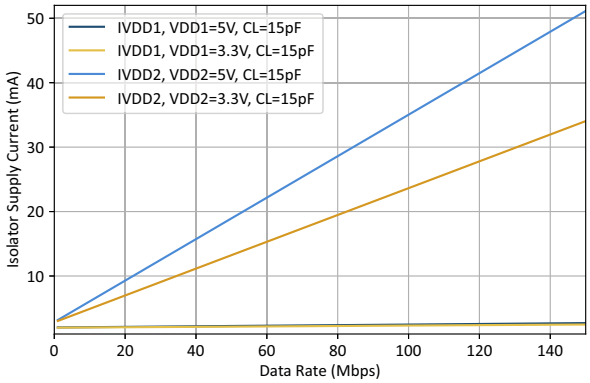



**Figure 23. Isolator Supply Current vs. Data Rate in 4 Forward/0 Reverse Configuration, $C_L$ = 15 pF**

## 5.6. Timing Characteristics

**Table 10. Isolator Timing Characteristics**

Operating range for the following specifications with ±5% supply variation: VDD1 = VDD2 = 3.3 V for Si86P3x devices, VDD1 = 3.3 V to 5.0 V and VDD2 = 3.3 V for Si86P4x devices, VDD1 = 5.0 V and VDD2 = 3.3 V to 5.0 V for Si86P5x; $T_A$ = –40 to +125 °C with $T_A$ (typical) = 25 °C.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Data rate | | | — | — | 150 | Mbps |
| Pulse width | | Minimum pulse width guaranteed to be transmitted to output. | 6.7 | — | — | ns |
| Propagation delay | $t_{PHL}$, $t_{PLH}$ | See Figure 24. “Propagation Delay Timing for Digital Channels” | 5.0 | 8.0 | 15.0 | ns |
| Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$ | PWD | See Figure 24. “Propagation Delay Timing for Digital Channels” | — | 0.2 | 3.0 | ns |
| Propagation delay skew | $t_{PSK(P-P)}$[1] | | — | 2.0 | 4.5 | ns |
| Channel-channel skew | $t_{PSK}$ | | — | 0.4 | 2.5 | ns |
| Output rise time | $t_R$ | $C_{LOAD}$ = 15 pF<br>See Figure 24. “Propagation Delay Timing for Digital Channels” | — | 2.5 | 4.0 | ns |
| Output fall time | $t_F$ | $C_{LOAD}$ = 15 pF<br>See Figure 24. “Propagation Delay Timing for Digital Channels” | — | 2.5 | 4.0 | ns |
| Peak eye diagram jitter | $t_{JIT(PK)}$ | | — | 350 | — | ps |
| Startup time[2] | $t_{ST}$ | No load<br>Full load<br>See 5.7. “Typical Performance Characteristics” | —<br>— | 290<br>300 | —<br>— | µs |
| Common-mode transient immunity | CMTI | $V_{An}$ = VDDx or 0 V<br>VCM = 1500 V | 100 | — | — | kV/µs |

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
2. Startup time is the time period from the application of power to the appearance of valid data at the output.

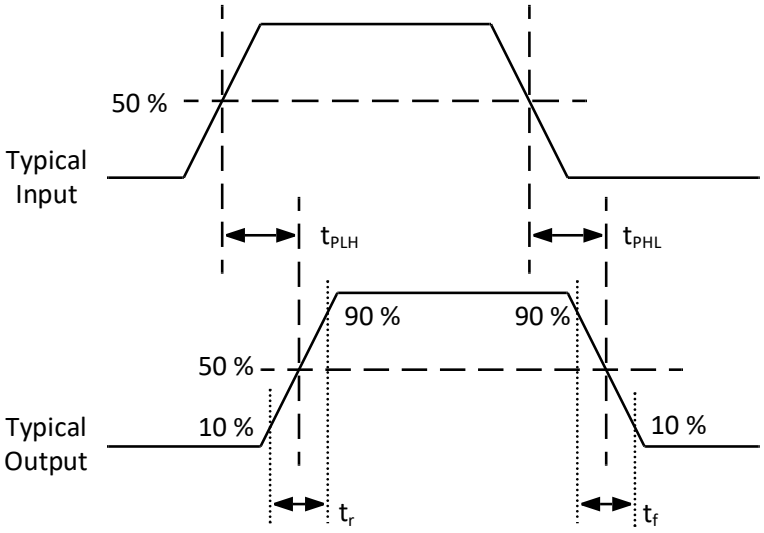



**Figure 24. Propagation Delay Timing for Digital Channels**

## 5.7. Typical Performance Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in 5. "Electrical Specifications" for actual specification limits.

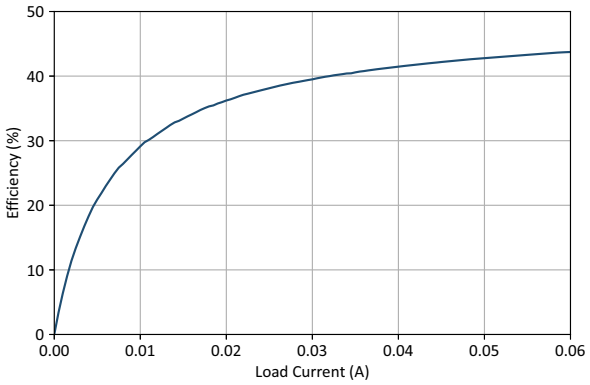



**Figure 25. Si86P3x Efficiency vs. Load Current**

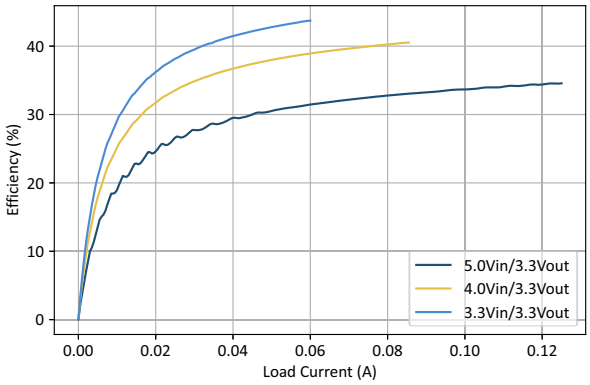



**Figure 26. Si86P4x Efficiency vs. Load Current**

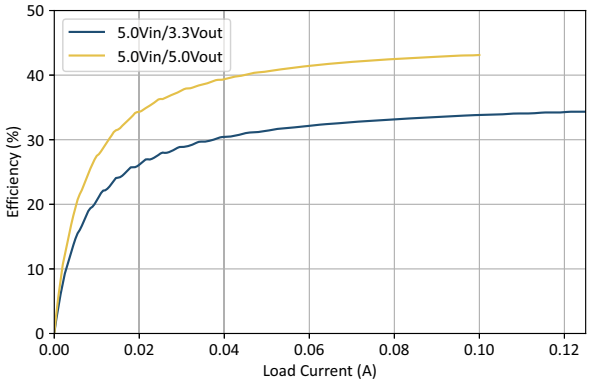



**Figure 27. Si86P5x Efficiency vs. Load Current**

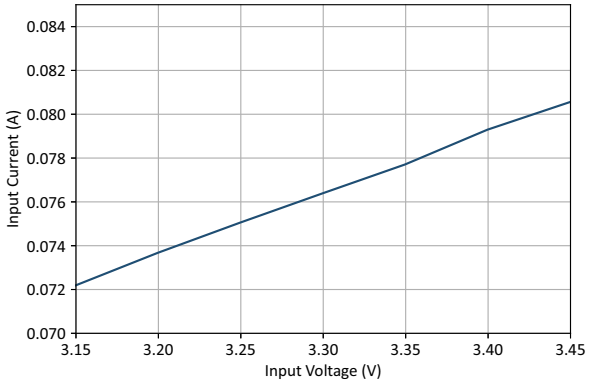



**Figure 28. Si86P3x Short Circuit Supply Current vs. Supply Voltage**

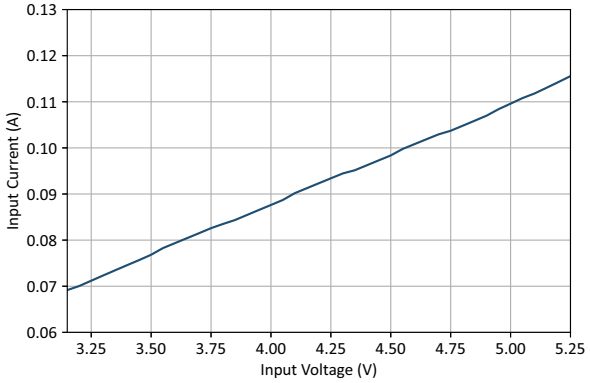



**Figure 29. Si86P4x Short Circuit Supply Current vs. Supply Voltage**

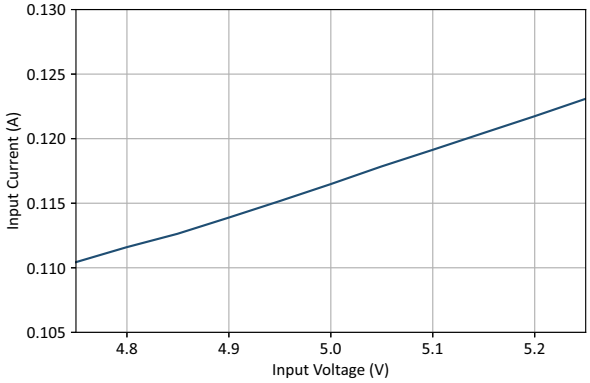



**Figure 30. Si86P5x Short Circuit Supply Current vs. Supply Voltage**

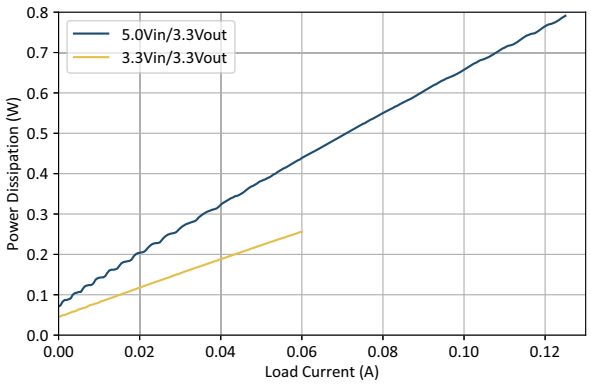



**Figure 31. Si86P4x Power Dissipation vs. Load Current**

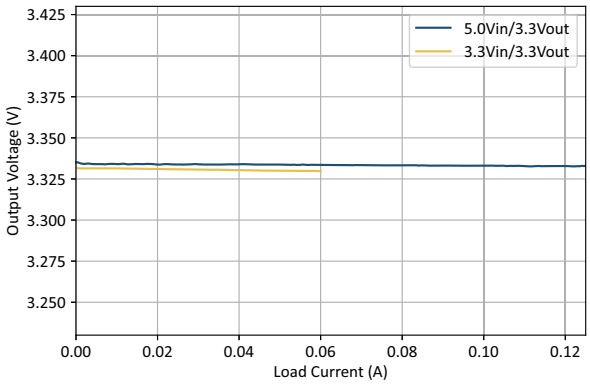



**Figure 32. Si86P4x Output Voltage vs. Load Current**

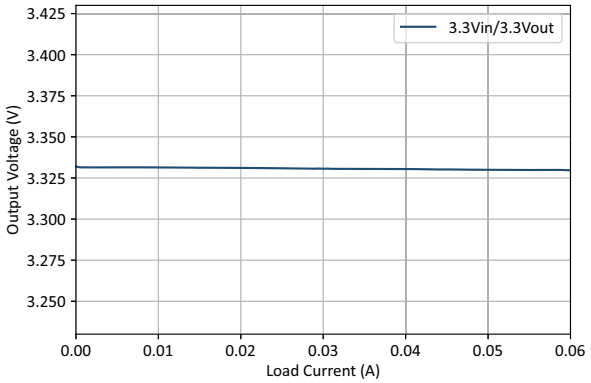



**Figure 33. Si86P3x Output Voltage vs. Load Current**

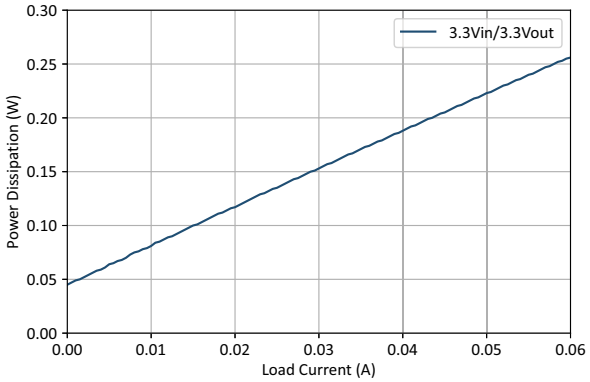



**Figure 34. Si86P3x Power Dissipation vs. Load Current**

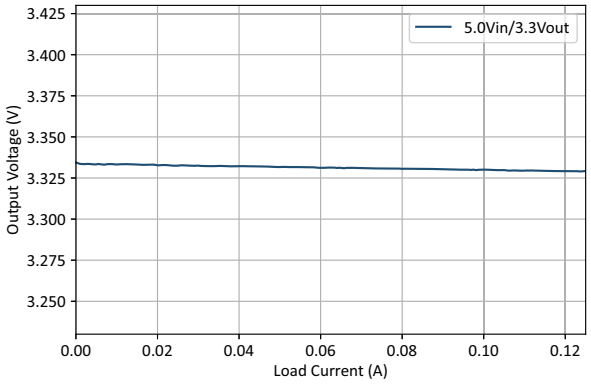



**Figure 35. Si86P5x Output Voltage vs. Load Current**

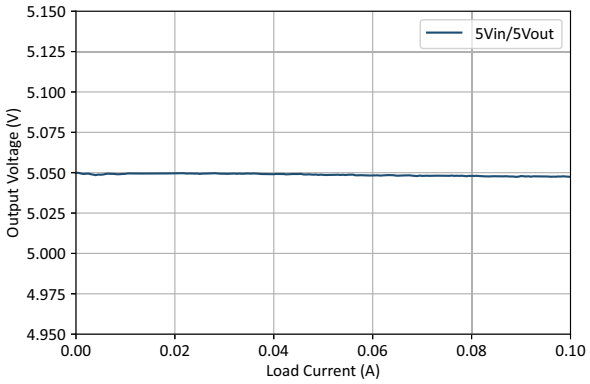



**Figure 36. Si86P5x Output Voltage vs. Load Current**

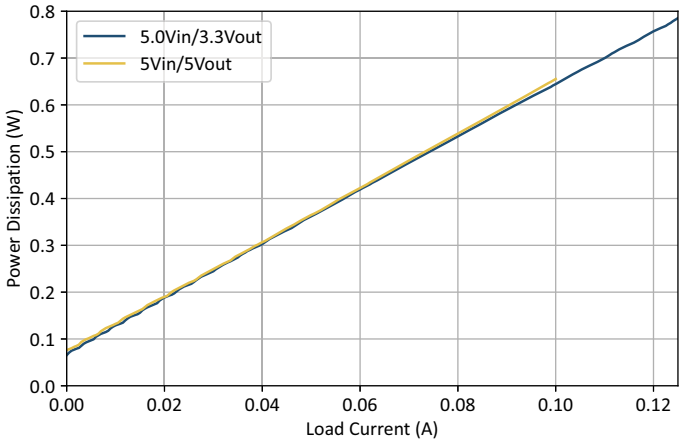



**Figure 37. Si86P5x Power Dissipation vs. Load Current**

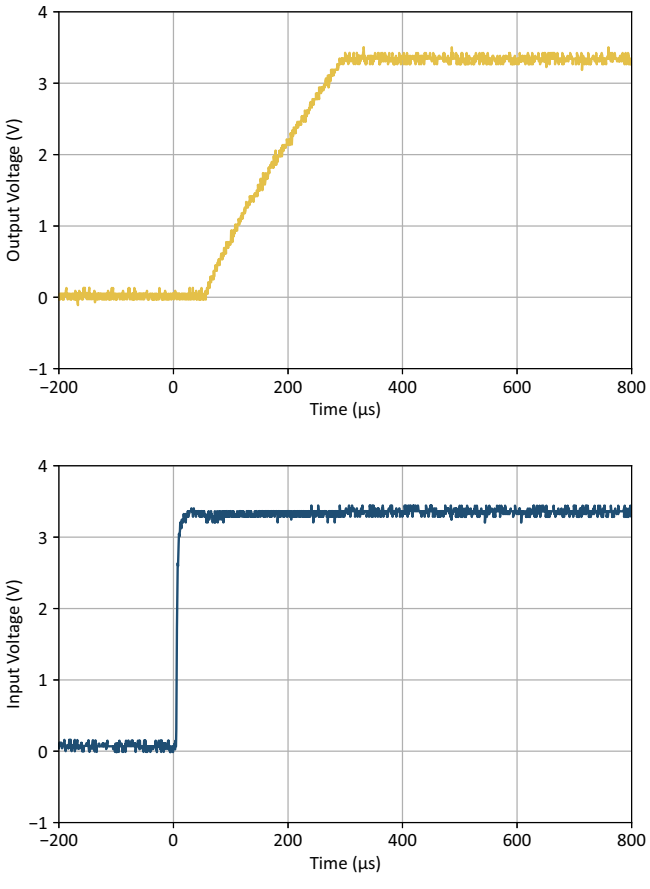



**Figure 38. Si86P3x Power Supply Startup at No Load ($C_{LOAD}$ = 5.8 µF)**

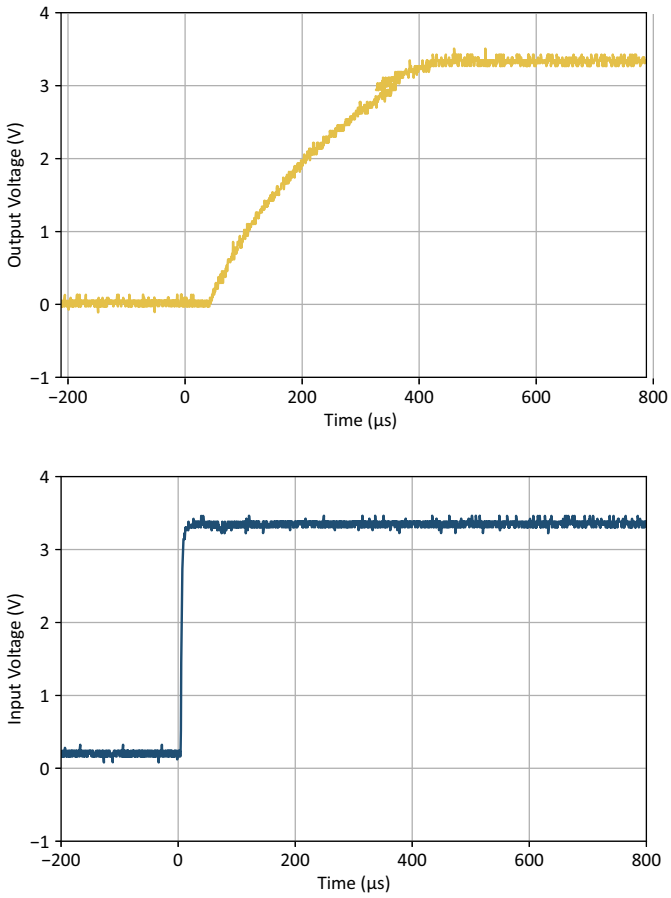



**Figure 39. Si86P3x Power Supply Startup at Full Load ($C_{LOAD}$ = 5.8 µF)**

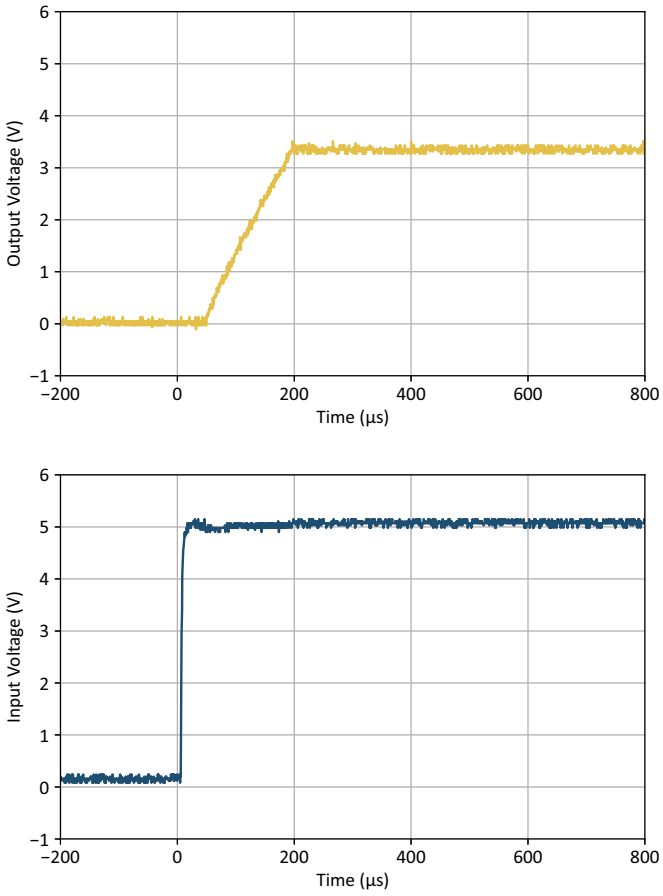



**Figure 40. Si86P4x Power Supply Startup at No Load 5 V to 3.3 V ($C_{LOAD}$ = 5.8 µF)**

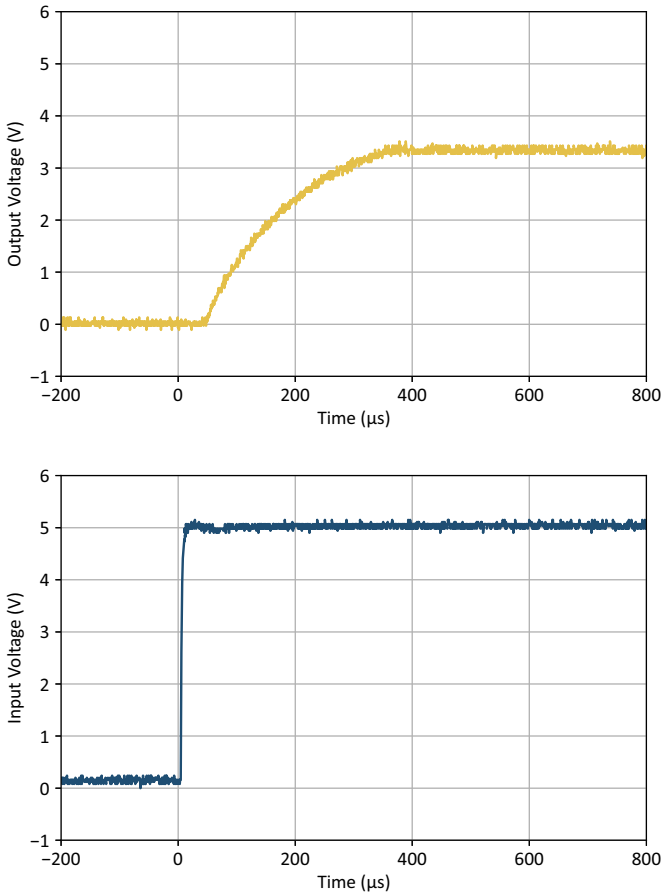
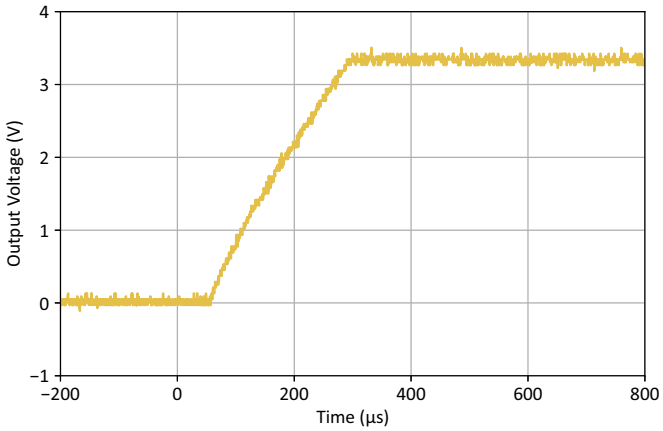



**Figure 41. Si86P4x Power Supply Startup at Full Load 5 V to 3.3 V ($C_{LOAD}$ = 5.8 µF)**



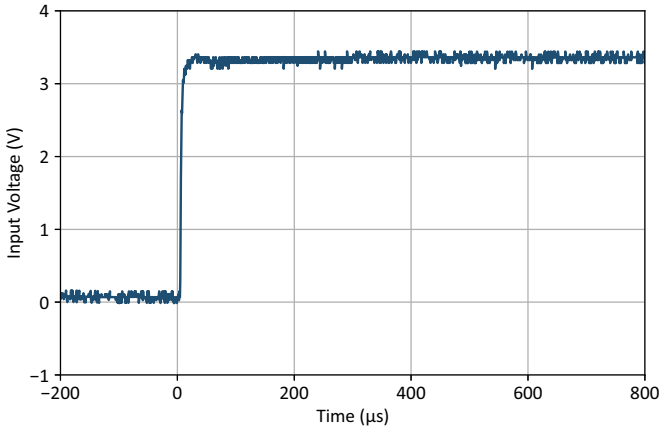
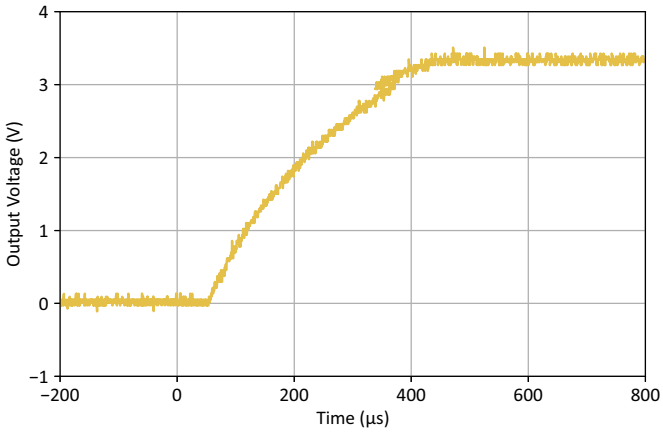




**Figure 42. Si86P4x Power Supply Startup at No Load 3.3 V to 3.3 V ($C_{LOAD}$ = 5.8 µF)**



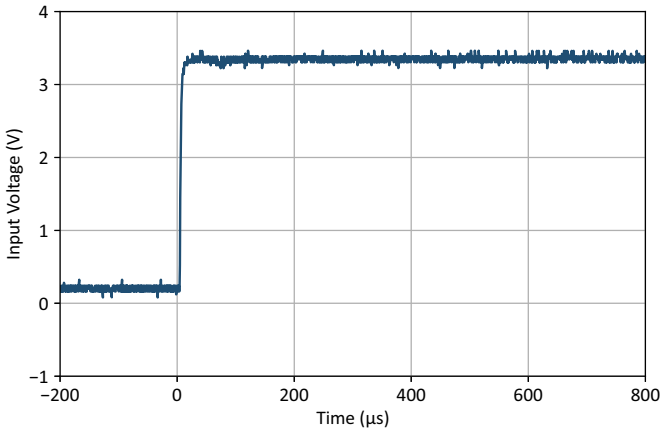




**Figure 43. Si86P4x Power Supply Startup at Full Load 3.3 V to 3.3 V ($C_{LOAD}$ = 5.8 µF)**

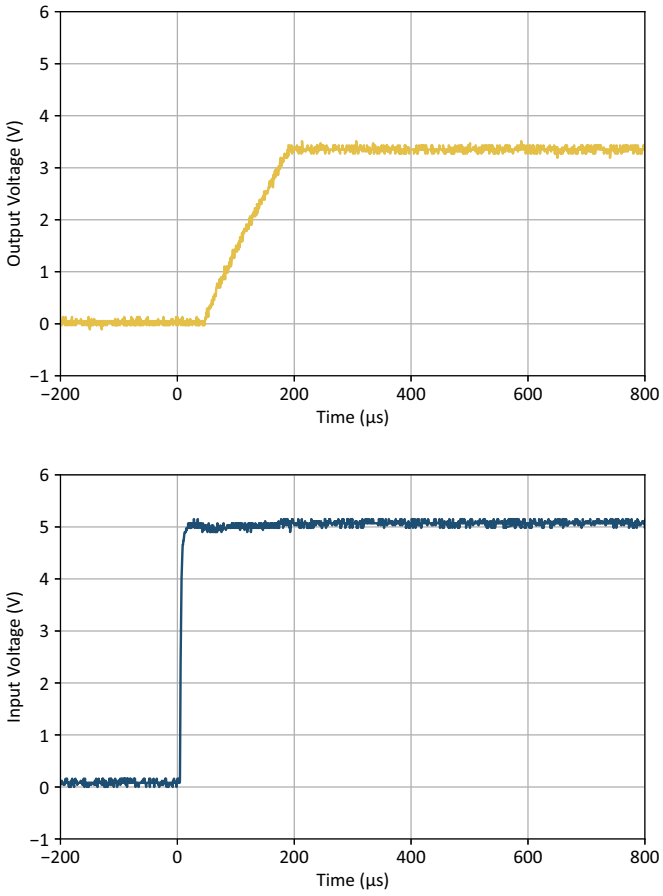



**Figure 44. Si86P5x Power Supply Startup at No Load 5 V to 3.3 V ($C_{LOAD}$ = 5.8 µF)**

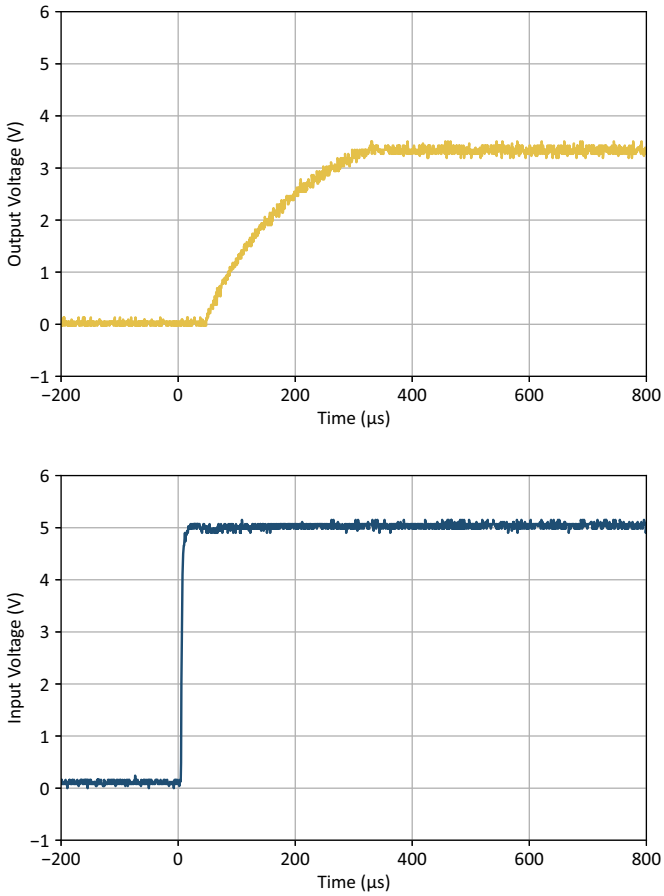



**Figure 45. Si86P5x Power Supply Startup at Full Load 5 V to 3.3 V ($C_{LOAD}$ = 5.8 µF)**

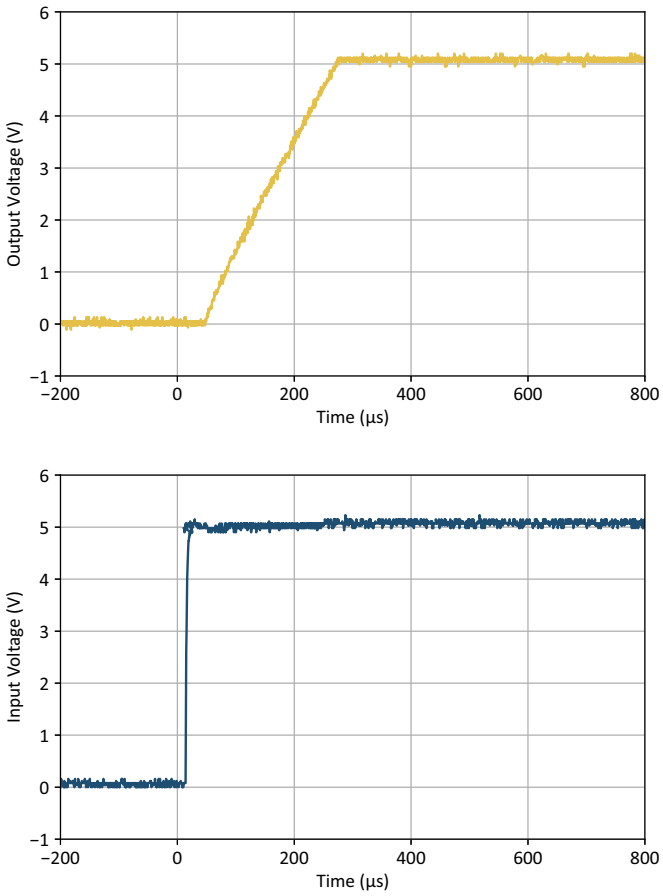



**Figure 46. Si86P5x Power Supply Startup at No Load 5 V to 5 V ($C_{LOAD}$ = 5.8 µF)**

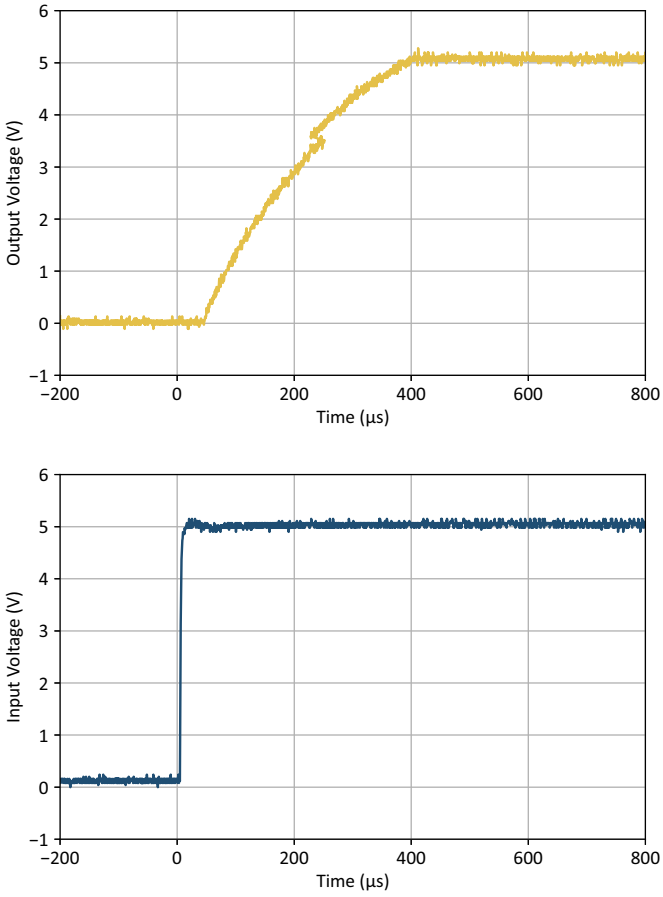



**Figure 47. Si86P5x Power Supply Startup at Full Load 5 V to 5 V ($C_{LOAD}$ = 5.8 µF)**

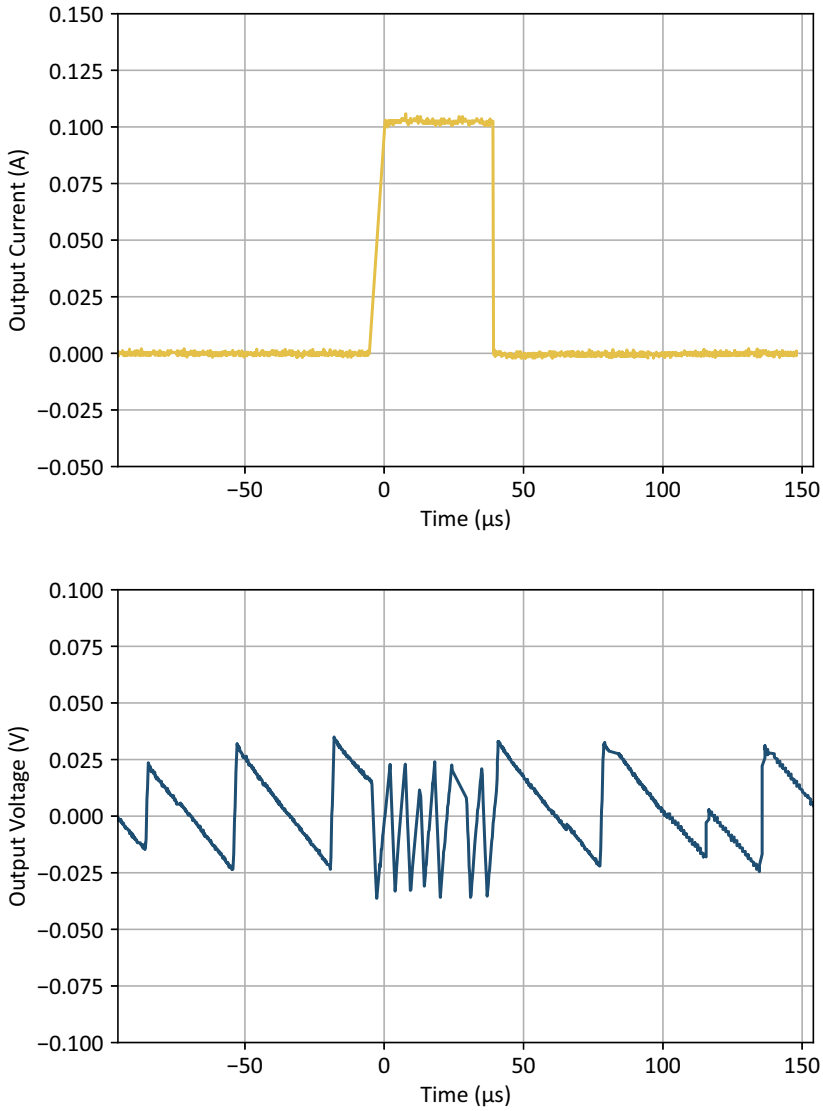



**Figure 48. Si86P5x Transient Response (No Load to Full Load)**

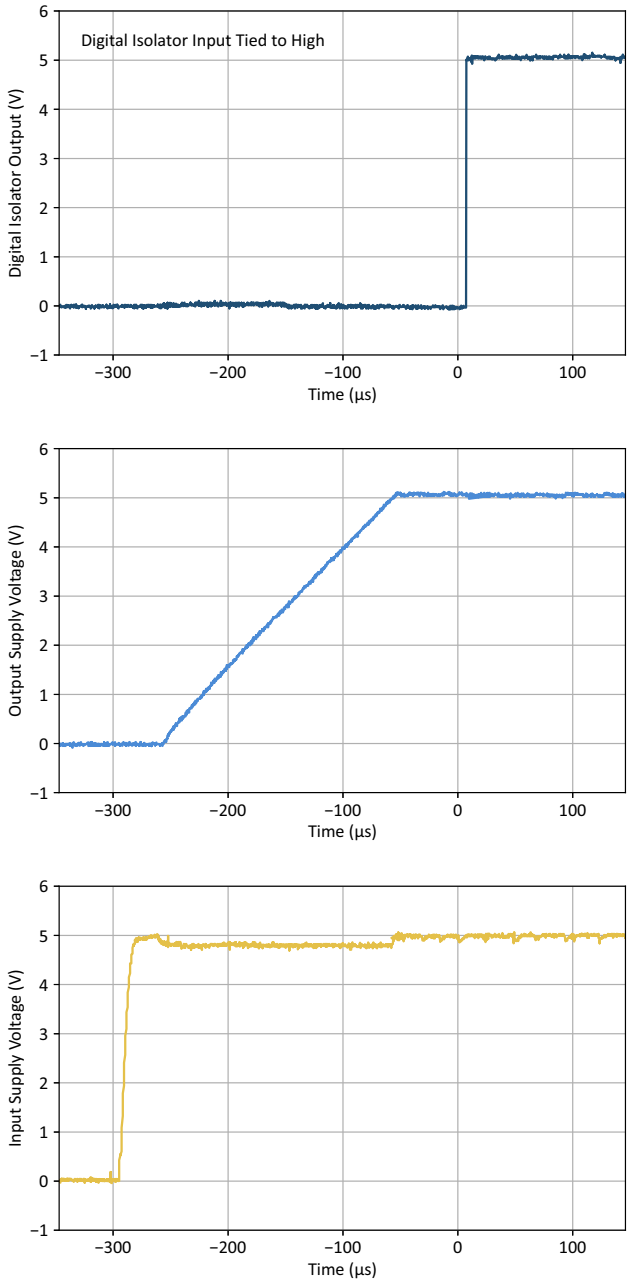



**Figure 49. Si86P5x Digital Isolator Startup Sequence at No Load**

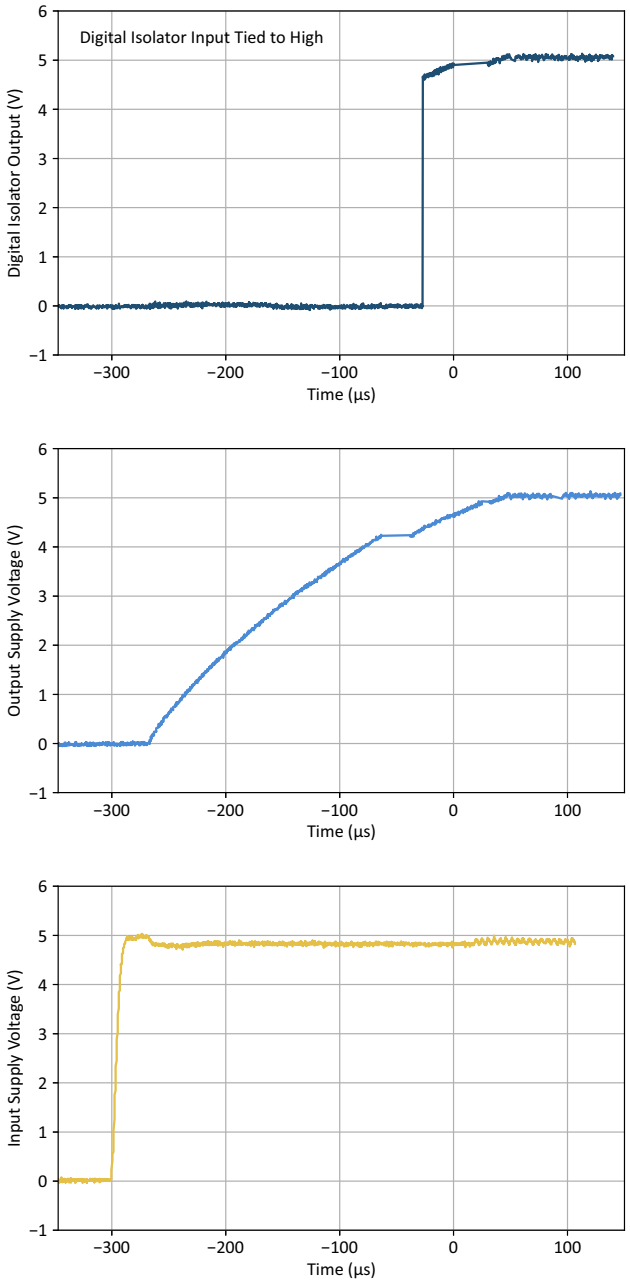



**Figure 50. Si86P5x Digital Isolator Startup Sequence at Full Load**

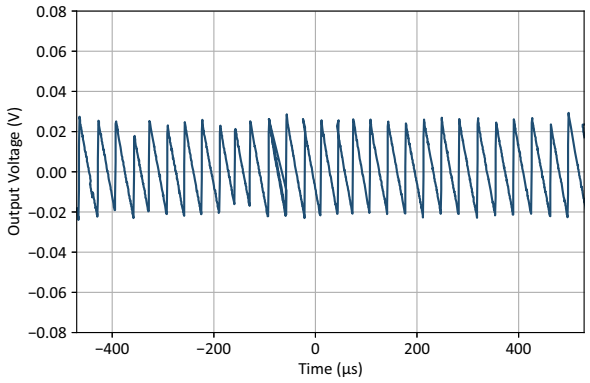



**Figure 51. Si86P5x Output Ripple (No Load, $C_{OUT}$ = 5.8 µF)**

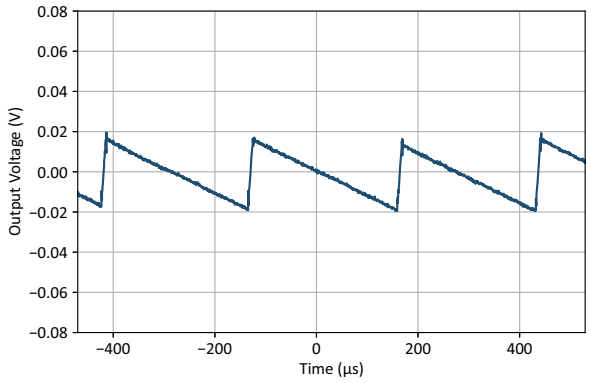



**Figure 52. Si86P5x Output Ripple (No Load, $C_{OUT}$ = 47 µF)**

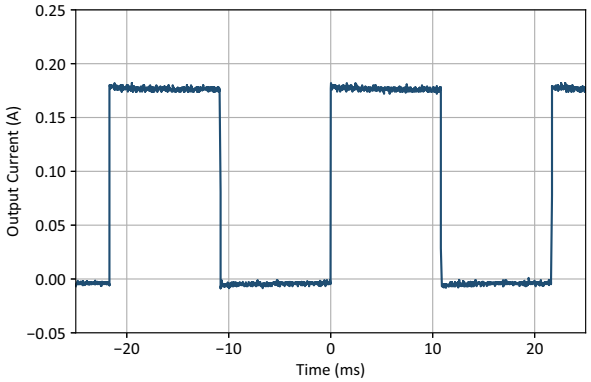



**Figure 53. Si86P4/5x Short Circuit Output Supply Current $V_I$ = 5.0 V**

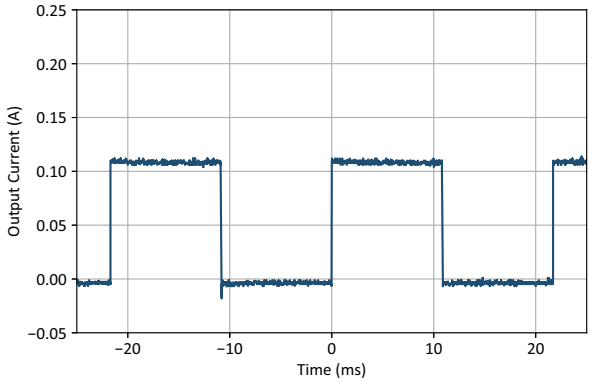



**Figure 54. Si86P3/4x Short Circuit Output Supply Current $V_I$ = 3.3 V**

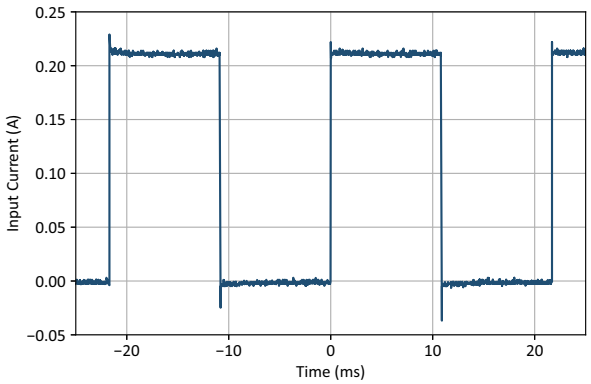



**Figure 55. Si86P4/5x Short Circuit Input Supply Current $V_I$ = 5.0 V**

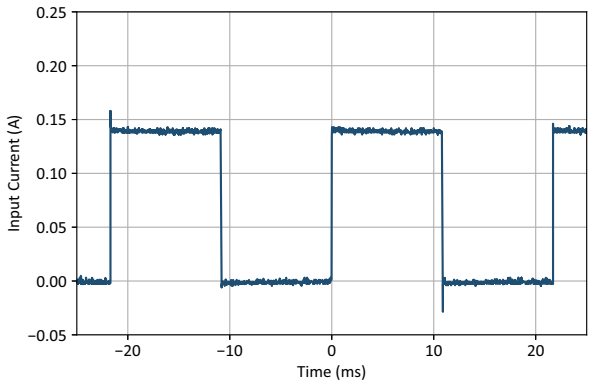



**Figure 56. Si86P3/4x Short Circuit Input Supply Current $V_I$ = 3.3 V**

## 5.8. Thermal Characteristics

**Table 11. Thermal Characteristics**

| Parameter | Symbol | Test Condition | WB SOIC-16 | WB SOIC-20 | Unit |
|---|---|---|---|---|---|
| **Thermal resistance** | | | | | |
| Junction-to-ambient | $\theta_{JA}$ | 4-layer, 2s2p JEDEC test board | 70 | 65 | °C/W |
| **Characterization parameter** | | | | | |
| Junction-to-top | $\psi_{JT}$ | 4-layer, 2s2p JEDEC test board | 8 | 7 | °C/W |
| Junction-to-board | $\psi_{JB}$ | 4-layer, 2s2p JEDEC test board | 45 | 36 | °C/W |

## 5.9. Safety Certifications and Specifications (Pending)

**Table 12. Regulatory Information[1]**

| |
|---|
| **CSA** |
| The Si86Px is certified under CSA. For more details, see master contract number 232873. |
| 62368-1: rated up to 600 $V_{RMS}$ reinforced insulation working voltage; rated up to 1000 $V_{RMS}$ basic insulation working voltage. |
| 60601-1: rated up to 250 $V_{RMS}$ working voltage and two Means of Patient Protection (MOPP). |
| **VDE** |
| The Si86Px is certified under VDE. For more details, see file 5028467. |
| 60747-17: rated up to 891 $V_{PEAK}$ for basic insulation working voltage. |
| **UL** |
| The Si86Px is certified under UL1577 component recognition program. For more details, see file E257455. |
| Rated up to 3.75 $kV_{RMS}$ VISO isolation voltage for basic protection. |
| **CQC** |
| The Si86Px is certified under GB4943.1. |
| Rated up to 250 $V_{RMS}$ reinforced insulation working voltage at 5000 meters tropical climate. |

1. For more information, see 8. "Ordering Information".

**Table 13. Insulation and Safety-Related Specifications**

| Parameter | Symbol | Test Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC- 16 | WB SOIC-20 | |
| Nominal external air gap (clearance)[1,2,3] | CLR | | 7.6 | 7.6 | mm |
| Nominal external tracking (creepage)[1,2,3] | CRP | | 7.6 | 7.6 | mm |
| Minimum internal gap (internal clearance) | DTI | | 0.016/0.100 | 0.016/0.100 | mm |
| Tracking resistance | CTI or PTI | IEC60112 | Up to 600 | Up to 600 | $V_{RMS}$ |

1. CSA certifies the clearance and creepage limits listed in this table.
2. UL does not impose a clearance and creepage minimum for component-level certifications.
3. VD certifies the clearance and creepage limits as: B SOIC $\geq$7.6 mm.

**Table 14. IEC60664-1 Ratings**

| Parameter | Test Conditions | Specification | |
|---|---|---|---|
| | | WB SOIC-16 | WB SOIC-20 |
| Material group | | I/II | I/II |
| Overvoltage category | Rated mains voltage ≤ 150 $V_{RMS}$ | I-IV | I-IV |
| | Rated mains voltage ≤ 300 $V_{RMS}$ | I-IV | I-IV |
| | Rated mains voltage ≤ 600 $V_{RMS}$ | I-III | I-III |
| | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-II | I-II |

**Table 15. IEC60747-17 Insulation Characteristics[1]**

| Parameter | Symbol | Test Condition | Characteristic | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC-16 | WB SOIC- 20 | |
| Maximum working isolation voltage | $V_{IOWM}$ | According to Time-Dependent Dielectric Breakdown (TDDB) Test | C = 630 | C = 630 | $V_{RMS}$ |
| Maximum repetitive isolation voltage | $V_{IORM}$ | According to Time-Dependent Dielectric Breakdown (TDDB) Test | C = 891 | C = 891 | $V_{PEAK}$ |
| Apparent charge | $Q_{PD}$ | Method b: At routine test (100% production) and preconditioning (type test);<br>$V_{INI}$ = 1.2 x $V_{IOTM}$, $t_{INI}$ = 1 s<br>$V_{PD(M)}$ = 1.5 x $V_{IORM}$, $t_M$ = 1 s (method b1) or<br>$V_{PD(M)}$ = $V_{INI}$, $t_M$ = $t_{INI}$ (method b2) | ≤5 | ≤5 | pC |
| Maximum transient isolation voltage | $V_{IOTM}$ | $V_{TEST}$ = $V_{IOTM}$, t = 60 s (qualification);<br>$V_{TEST}$ = 1.2 x $V_{IOTM}$, t = 1 s (100% production) | C = 5302 | C = 5302 | $V_{PEAK}$ |
| Maximum surge isolation voltage | $V_{IOSM}$ | Tested in oil with ≥1.3 x $V_{IMP}$ and 1.2 µs/50 µs profile (qualification) | 8000 | 8000 | $V_{PEAK}$ |
| Maximum impulse voltage | $V_{IMP}$ | Tested in air with 1.2 µs/50 µs profile (qualification) | 6154 | 6154 | $V_{PEAK}$ |
| Capacitance (input-to-output)[2] | $C_{IO}$ | f = 1 MHz | 3.8 | 4.2 | pF |
| Isolation resistance[2] | $R_{IO}$ | $T_A$ = 25 °C, $V_{IO}$ = 500 V | $>10^{12}$ | $>10^{12}$ | Ω |
| | | $T_A$ = 125 °C, $V_{IO}$ = 500 V | $>10^{11}$ | $>10^{11}$ | Ω |
| | $R_{IO\_S}$ | $T_A$ = $T_S$, $V_{IO}$ = 500 V | $>10^9$ | $>10^9$ | Ω |
| Pollution degree | | | 2 | 2 | |
| Climatic category | | | 40/125/21 | 40/125/21 | |

1. This coupler is suitable for “basic insulation” only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.
2. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.

**Table 16. IEC60747-17 Safety Limiting Values[1]**

| Parameter | Symbol | Test Condition | Max | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC-16 | WB SOIC-20 | |
| Safety temperature | $T_S$ | | 150 | 150 | °C |
| Safety input, output, or supply current | $I_S$ | Refer to $\theta_{JA}$ in Table 11. "Thermal Characteristics"; VDDx = 5 V, $T_J$ = 150 °C, $T_A$ = 25 °C | 357 | 385 | mA |
| Safety input, output, or total power | $P_S$ | Refer to $\theta_{JA}$ in Table 11. "Thermal Characteristics"; $T_J$ = 150 °C, $T_A$ = 25 °C | 1.79 | 1.92 | W |

1. Maximum value allowed in the event of a failure; also see the temperature derating curves below.

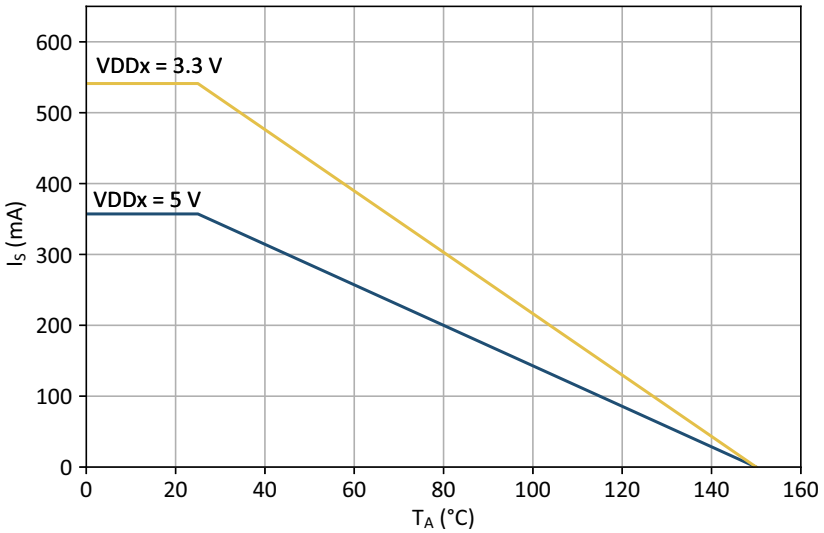



**Figure 57. WB SOIC-16 Safety Current vs. Ambient Temperature Derating Curve**

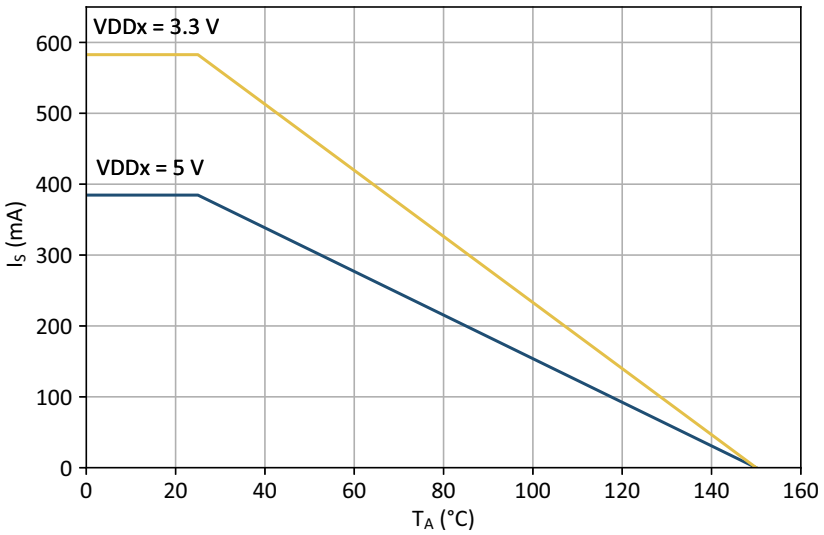



**Figure 58. WB SOIC-20 Safety Current vs. Ambient Temperature Derating Curve**

**Table 17. UL1577 Insulation Characteristics**

| Parameter | Symbol | Test Condition | Characteristic | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC-16 | WB SOIC-20 | |
| Maximum withstanding isolation voltage | $V_{ISO}$ | $V_{TEST} = V_{ISO}$, t = 60 s (qualification);<br>$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production) | C = 3750 | C = 3750 | $V_{RMS}$ |
| Primary-side current rating | | VDDx = 5 V, $T_A$ = 25 °C, (qualification per channel) | 10 | 10 | mA |
| Primary-side power rating | | | 50 | 50 | mW |
| Secondary-side current rating | | | 10 | 10 | mA |
| Secondary-side power rating | | | 50 | 50 | mW |

# 6. Application Information

The Si86Px is designed to be flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate configuration must be selected and its circuit carefully designed.

## 6.1. Recommended Application Circuits

An example application of the Si86Px41x for isolated SPI communication is shown in Figure 59 below. Traditional digital isolators require power supplied at both the primary and secondary side for the controller and AD converter. In this example, the built-in isolated power source of the Skyworks isolator is used to supply the AD converter, making a secondary-side power supply unnecessary. This high level of integration offered by Si86Px devices makes them an ideal choice for compact, isolated, multi-channel data acquisition applications.

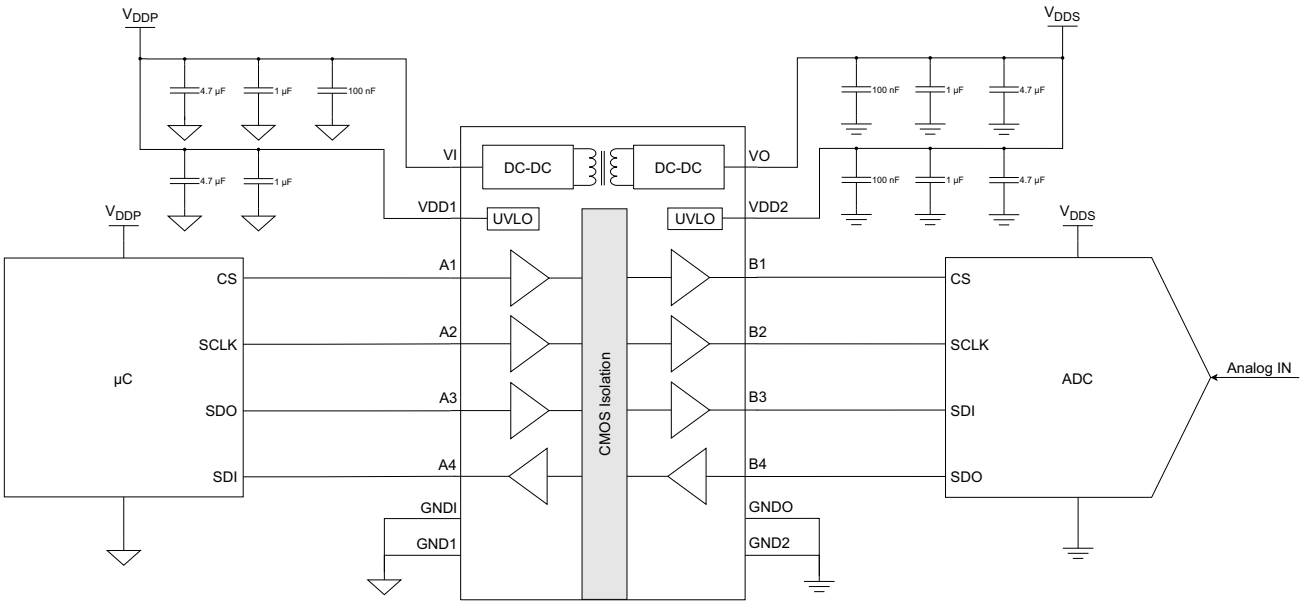



**Figure 59. Si86Px41 Isolated SPI Communication Example**

## 6.2. Power Supply and Layout Considerations

- Bypass capacitors (usually 0.1 µF, 1 µF, and 4.7 µF) for the power converter supply pins (VI and GNDI at the input side, VO and GNDO at the output side) should be placed as close to the these pins as possible with thick and short traces.
- Bypass capacitors (usually 0.1 µF and 1 µF) for the digital isolator supply pins (VDD1 and GND1 at the input side, VDD2 and GND2 at the output side) should be placed as close to these pins as possible.
- Low EMI design requires a four layer PCB stack up. Top and bottom layers can be used for signal routing and the internal layers for creating an embedded capacitor over the isolation barrier which must withstand the required test voltages.
- Low EMI design requires additional high-frequency filtering on the input and output sides. Long wires at the input or output side can act as transmitting antennas that pick up high-frequency switching noise from the integrated isolated dc-to-dc converter. Using a common-mode choke at the input side and ferrite beads at the output side helps reduce radiated emissions by attenuating common-mode currents in the wiring.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the input and output sides.
- If the application requires extremely high common-mode transient immunity (CMTI) performance, add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no-connect (NC) pins. This helps improve the CMTI performance but also decreases the maximum usable data rate.
- To enhance the robustness of the design in excessively noisy environment, resistors in the range of 50 to 300 Ω should be placed in series with the digital isolator inputs and outputs.

## 6.3. Hysteretic Control and Programmable Output Voltage

To regulate the isolated output supply at the VO pin, a hysteretic on/off controller is used for its inherent stability and fast response. Internally, the regulated output voltage level ($V_{out}$), generated by a full-wave rectifier, is sensed via an external resistive divider network. The divided voltage ($V_{comp}$) feeds the comparator on the secondary side through the control pin, where it is measured against an integrated reference voltage.

When $V_{out}$ exceeds the upper threshold ($V_{out\_max}$), the comparator toggles its output, sending a control signal through an isolation channel to the primary side. This signal disables the oscillator, and the load on the secondary side begins to discharge the output capacitor, causing VO to drop at a rate defined by:

$$\frac{dV_{out}}{dt} = \frac{-I_{load}}{C_{load}}$$

Once $V_{out}$ falls below the lower threshold ($V_{out\_min}$), the comparator output switches again,

reenabling the primary oscillator and ramping $V_{out}$ backup. This creates a controlled ripple in $V_{out}$, with transitions of the control signal synchronized to threshold crossings as shown in Figure 60 below.

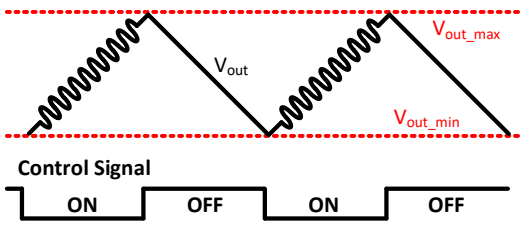



**Figure 60. Isolated Output Voltage with OOK Ripple**

As described above, the sensed voltage ($V_{comp}$) is compared to an internal reference to establish the upper and lower threshold level, $V_{out\_max}$ and $V_{out\_min}$, used for hysteretic regulation of the internal output signal $V_{out}$. By adjusting the ratio of external resistors R1 and R2 in the divider network, $V_{out}$, and by extension the voltage at the integrated power output pin (VO), can be continuously programmed to a desired level.

$$V_{out} = V_{ref} \times \frac{R1 + R2}{R2}$$

Figure 61 below shows how a bias current (I1) and a series-connected PMOS/NMOS pair create asymmetry between rising and falling edges of $V_{out}$, allowing independent analog control of both output voltage and hysteresis.

$$V_{hys} = 2 \times I1 \times R1$$

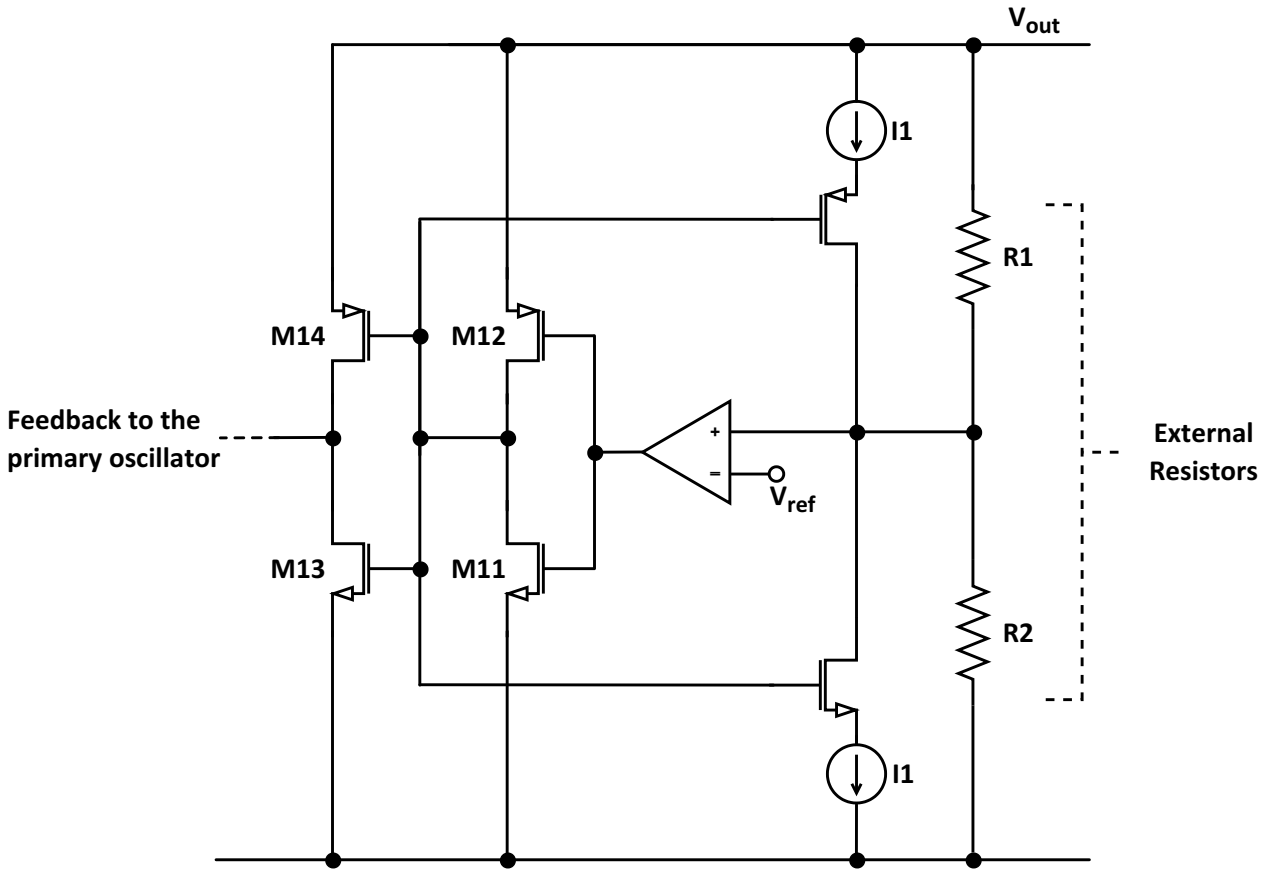



**Figure 61. Hysteresis Implementation**

The LC oscillator on the primary side delivers a fixed dc current to the load capacitor $C_{load}$ on the secondary side. In steady-state operation, where $V_{out}$ cycles between $V_{out\_max}$ and $V_{out\_min}$, $C_{load}$ charges at a constant rate of approximately:

$$\frac{dV_{out}}{dt} = \frac{I_{out} - I_{load}}{C_{load}}$$

and discharges at a rate of approximately:

$$\frac{dV_{out}}{dt} = \frac{-I_{load}}{C_{load}}$$

In steady state, $dV_{out} = V_{hys}$ implies that the on and off times of the primary-side oscillator are:

$$t_{on} = C_{load} \times \frac{V_{hys}}{I_{out} - I_{load}}$$

$$t_{off} = C_{load} \times \frac{V_{hys}}{I_{load}}$$

The control frequency is given by:

$$\frac{1}{t_{on} + t_{off}}$$

This frequency depends heavily on $C_{load}$, $V_{hys}$, $I_{load}$, and can be tuned for specific load conditions by adjusting $C_{load}$ and $V_{hys}$. The following content outlines how to achieve a target output voltage within the usable range of 3.15 V to 5.25 V.

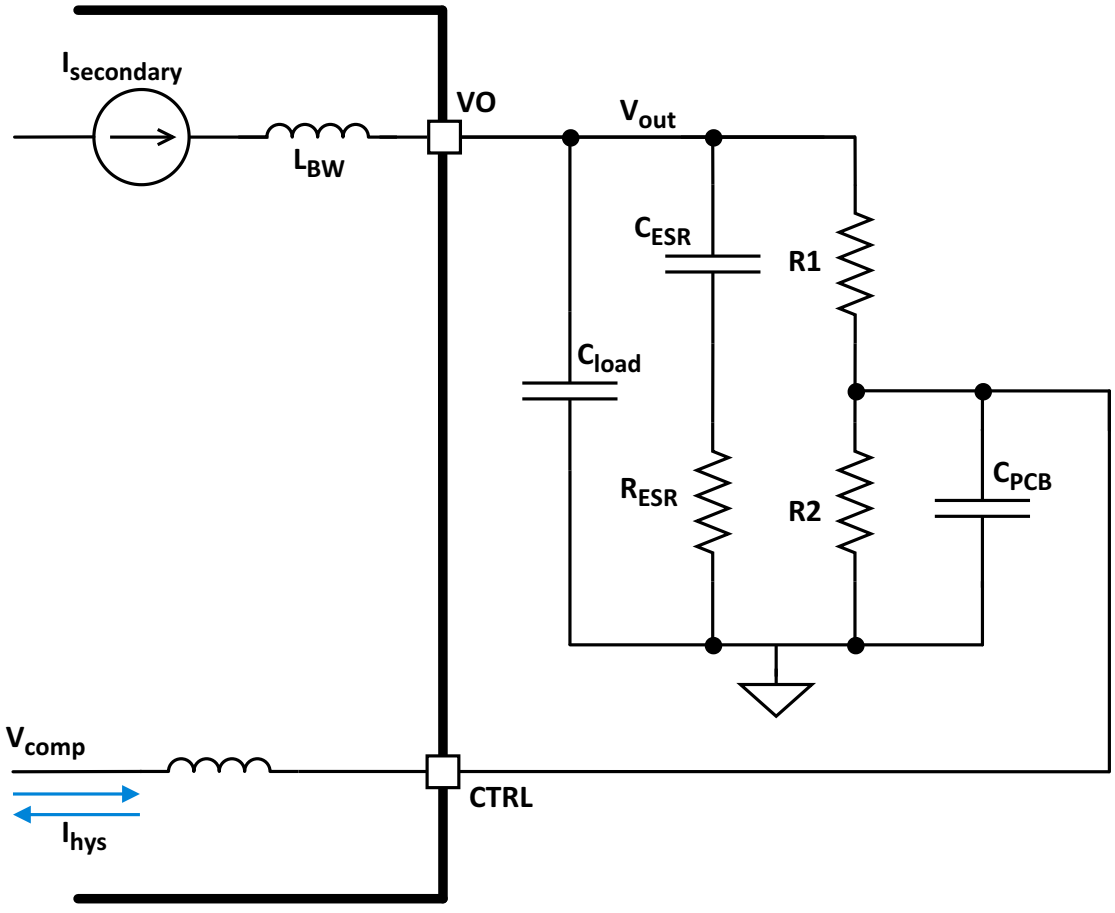



**Figure 62. Load Network**

$$V_{out} = V_{BG} \times \frac{R1 + R2}{R2}$$

$$\Delta V_{out} = 2 \times I_{hys} \times R1$$

**Table 18. Output Voltage and Hysteresis Programming Based on R1, R2 Values**

| R1 (Ω) | R2 (Ω) | $V_{out}$ (V) | V_hys (ΔVout) (V) |
|---|---|---|---|
| 17.2 k | 10 k | 3.3 | 27.2 m |
| 31.3 k | 10 k | 5 | 41.3 m |
| 63.25 k | 36.75 k | 3.3 | 100 m |
| 75.8 k | 24.2 k | 5 | 100 m |

**Table 19. Parameter Range**

| Parameter | Range |
|---|---|
| $C_{load}$ | 1 to 10 µF |
| $C_{ESR}$ | 10 µF |
| $I_{secondary}$ | 150 to 250 mA |

$$t_{start} = \frac{(C_{load} + C_{ESR}) \times V_{out}}{I_{secondary}}$$

**Table 20. Typical Startup Time**

| $V_{out}$ (V) | $C_{load}$ (F) | $C_{ESR}$ (F) | $t_{start}$ (s) (No load startup time) |
|---|---|---|---|
| 3.3 | 1 µ | 10 µ | 0.15 to 0.25 m |
| 3.3 | 10 µ | 10 µ | 0.3 to 0.45 m |
| 5 | 1 µ | 10 µ | 0.25 to 0.4 m |
| 5 | 10 µ | 10 µ | 0.45 to 0.7 m |

$$t_{on} = C_{load} \times \frac{\Delta V_{out}}{I_{secondary}} \qquad t_{off} = C_{load} \times R_{load} \times \frac{\Delta V_{out}}{V_{out}} \qquad f_{control} = \frac{1}{t_{on} + t_{off}}$$

Hysteresis and $C_{load}$ scale the control period linearly. Below is a table for $C_{load}$ = 4.7 µF and $V_{hys}$ = 100 mV. To keep $C_{ESR}$ out of the control frequency equation, $C_{load}$ and $R_{ESR}$ must be chosen appropriately. Choosing a $R_{ESR}$ of 1.5 to 2 Ω limits the cycle-by-cycle error to $f_{control}$.

**Table 21. Cycle-by-Cycle Error Control Limits vs. Component Selection**

| $V_{out}$ (V) | $R_{load}$ (Ω) | $f_{control}$ (Hz) |
|---|---|---|
| 3.3 | 50 | 100 to 115 k |
| 5 | 50 | 130 to 150 k |

**Table 22. Electrical Symbols and Definitions**

| Symbol | Definition |
|---|---|
| VI | Input power supply to the primary side of the Si86Px |
| VO | Integrated isolated power output pin; externally accessible isolated supply derived from input supply VI |
| $V_{out}$ | Internally regulated output voltage level sense for control loop hysteresis |
| $V_{comp}$ | Comparator input voltage derived from the R1/R2 resistive divider network |
| $V_{out\_max}$ | Upper voltage threshold for comparator toggling |
| $V_{out\_min}$ | Lower voltage threshold for comparator toggling |
| $V_{hys}$ | Hysteresis voltage band between $V_{out\_max}$ and $V_{out\_min}$ |
| I1 ($I_{hys}$) | Bias current for analog hysteresis generation (typically 0.5 µA) |
| $I_{load}$ | Current drawn by external load from the VO pin |
| $C_{load}$ | Load capacitance seen at VO |
| $C_{ESR}$ | High ESR capacitor used to slow startup timing |
| $R_{ESR}$ | Equivalent series resistance of CESR |
| $C_{PCB}$ | PCB trace capacitance (typically 5 to 10 pF) |
| $I_{secondary}$ | Rectified current available on the secondary side |
| $L_{BW}$ | Bond wire inductance |
| $V_{BG}$ | Internal band-gap reference voltage |
| R1, R2 | External resistors forming voltage divider for $V_{comp}$ and programmable $V_{out}$ |
| $R_{load}$ | Equivalent resistive load connected to the VO pin, used to model $I_{load} = V_{out}/R_{load}$ |

## 7. Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

All products in this data sheet are rated to MSL3 at 260 °C.

They can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

## 7.1. WB SOIC-16 Top Marking

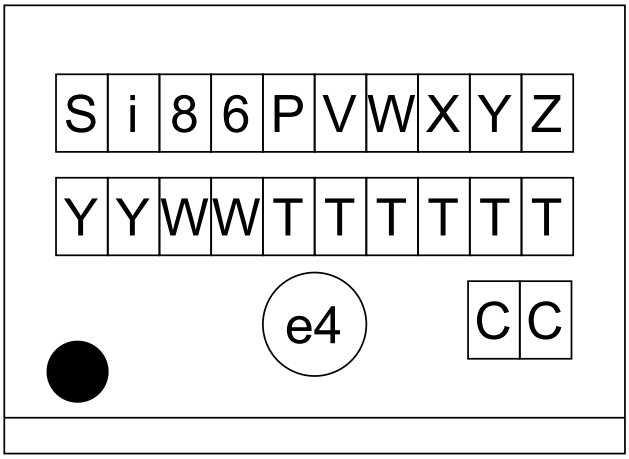



**Figure 63. WB SOIC-16 Top Marking**

**Table 23. WB SOIC-16 Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Base Part Number Ordering Options<br><br>(See 8. "Ordering Information" for more information) | Si86P = Isolator with integrated power transfer product series<br><br>V = Input supply voltage option<br><br>W = Total number of channels<br><br>X = Total number of reverse channels (right to left)<br><br>Y = Default isolated channel output state<br><br>Z = Isolation rating<br><br>C = 3.75 $kV_{RMS}$ |
| **Line 2 Marking:** | YY = Year<br><br>WW = Workweek | Assigned by the assembly house. Corresponds to the year and workweek of the mold date. |
| | TTTTTT = Mfg. Trace Code | Manufacturing Traceability Code<br><br>The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade. |
| **Line 3 Marking:** | e4 circle is 1.7 mm diameter | The "e4" symbol indicates Pb-free lead finish. |
| | CC = Country of Origin ISO Code Abbreviation | TW = Taiwan |

## 7.2. WB SOIC-20 Top Marking

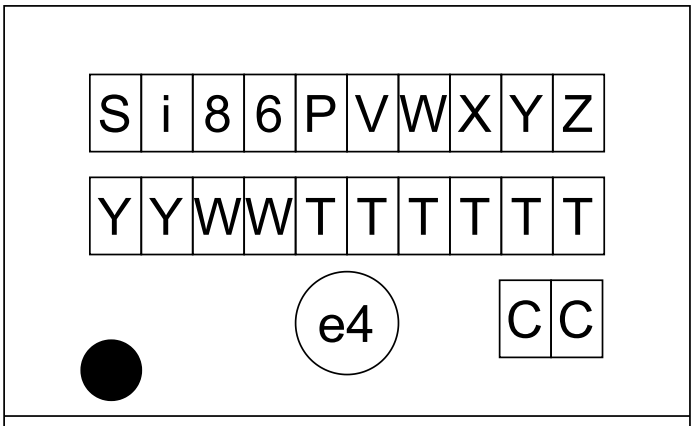



**Figure 64. WB SOIC-20 Top Marking**

**Table 24. WB SOIC-20 Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Base part number ordering options<br><br>(See 8. "Ordering Information" for more information) | Si86P = Isolator with integrated power transfer product series<br><br>V = Input supply voltage option<br><br>W = Total number of channels<br><br>X = Total number of reverse channels (right to left)<br><br>Y = Default isolated channel output state<br><br>Z = Isolation rating<br><br>C = 3.75 $kV_{RMS}$ |
| **Line 2 Marking:** | YY = Year<br><br>WW = Workweek | Assigned by the assembly house. Corresponds to the year and workweek of the mold date. |
| | TTTTTT = mfg. trace code | Manufacturing traceability code<br><br>The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate industrial-grade. |
| **Line 3 Marking:** | e4 circle is 1.7 mm diameter | The "e4" symbol indicates Pb-free lead finish. |
| | CC = country of origin ISO code abbreviation | TW = Taiwan |

## 7.3. WB SOIC-16 Package

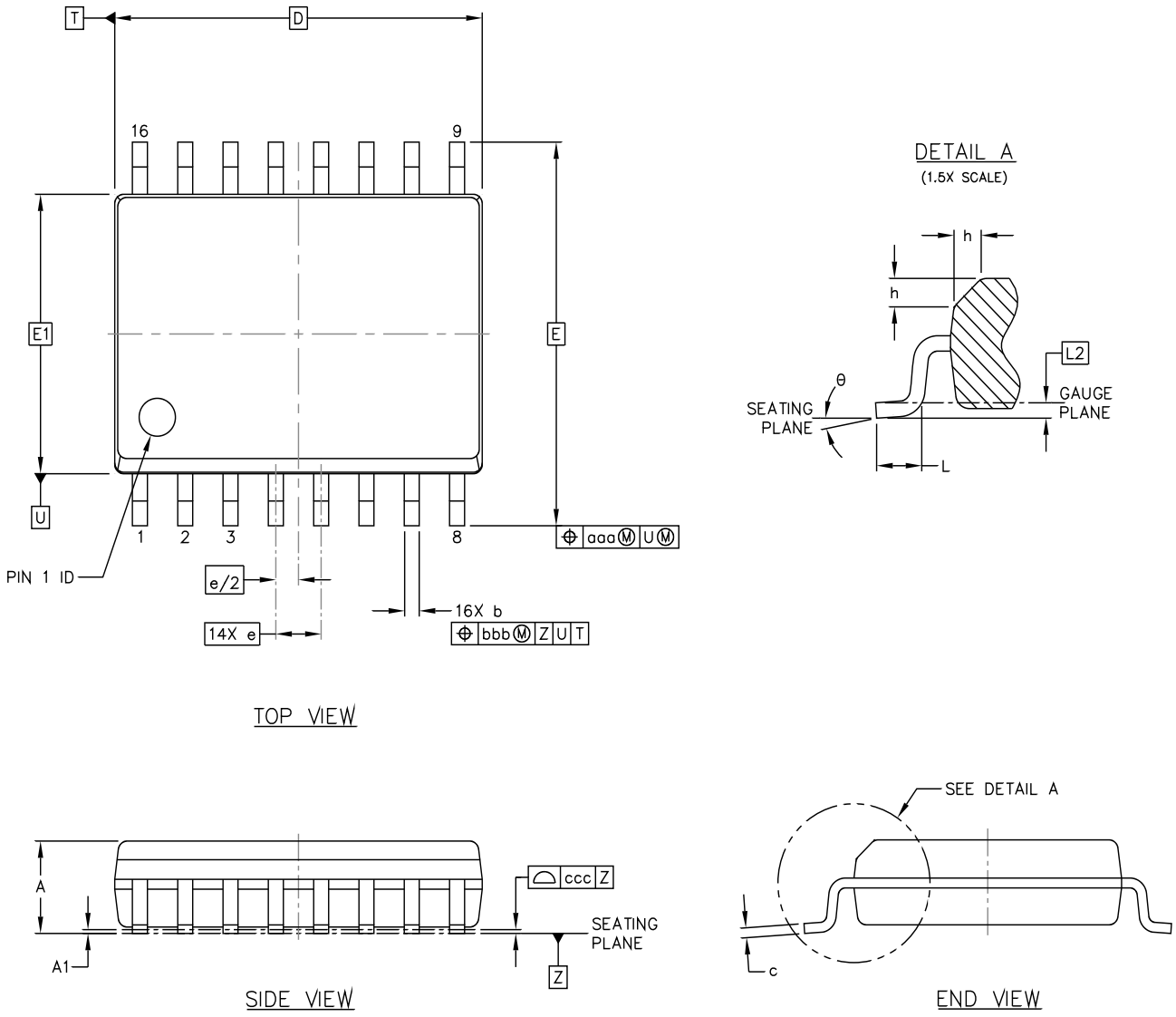



**Figure 65. WB SOIC-16 Package Dimensions**

**Table 25. WB SOIC-16 Package Dimensions[1,2,3,4,5]**

| Dimension | Min | Max |
|---|---|---|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 10.30 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | 0.33 | |
| bbb | 0.25 | |
| ccc | 0.10 | |

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ANSI Y14.5M:
   a. BSC: Basic dimension. Theoretically exact, shown without tolerance.
   b. REF: Reference dimension: Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions, or gate burrs, which shall not exceed 0.15 mm per end.
   Dimension E1 does not include interlead flash or protrusions, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-013, Variation AA.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small-body, lead-free components.

## 7.4. WB SOIC-20 Package

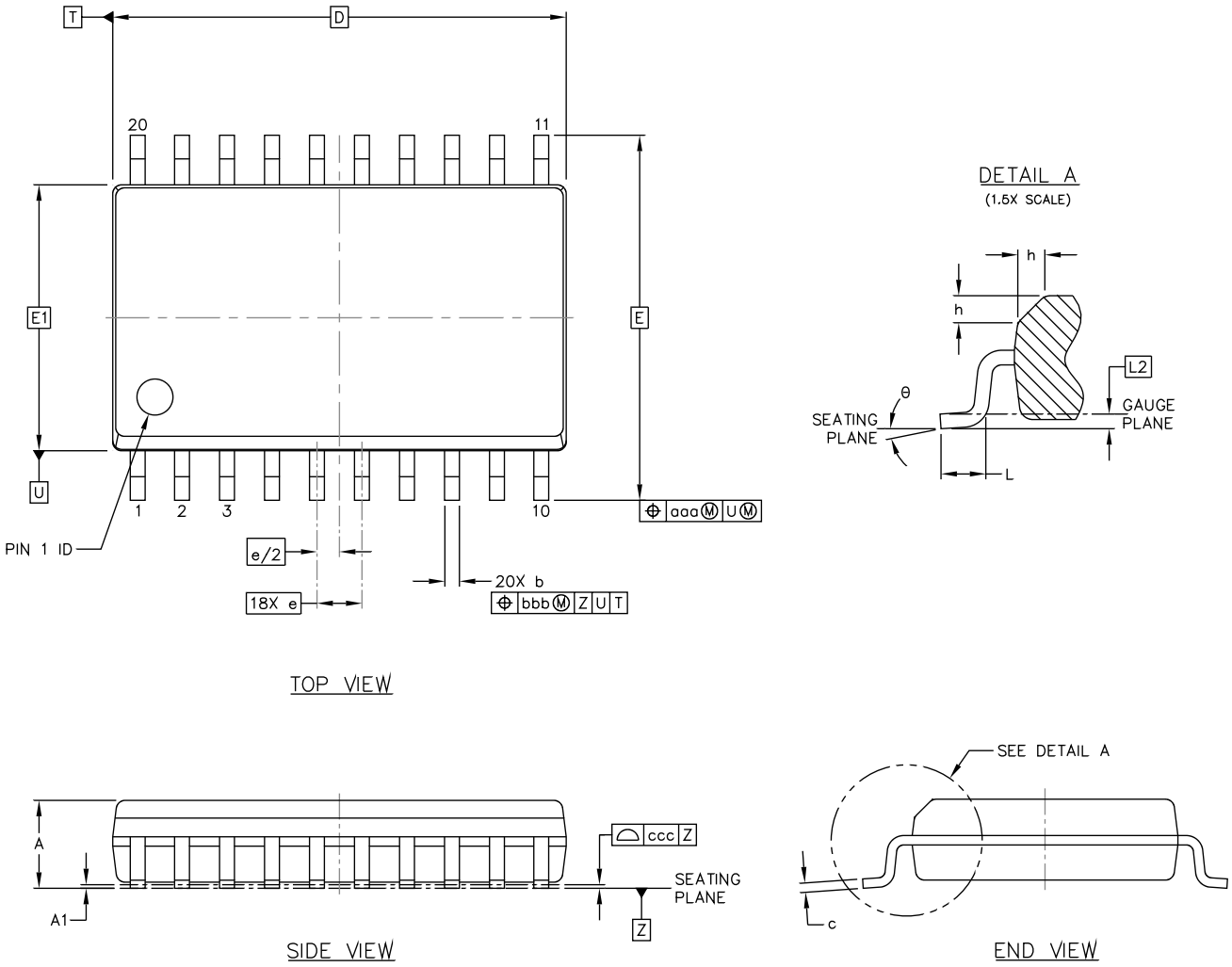



**Figure 66. WB SOIC-20 Package Dimensions**

**Table 26. WB SOIC-20 Package Dimensions[1,2,3,4,5]**

| Dimension | Min | Max |
|---|---|---|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 12.80 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | 0.33 | |
| bbb | 0.25 | |
| ccc | 0.10 | |

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ANSI Y14.5M:
   a. BSC: Basic dimension. Theoretically exact, shown without tolerance.
   b. REF: Reference dimension: Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions, or gate burrs, which shall not exceed 0.15 mm per end.
   Dimension E1 does not include interlead flash or protrusions, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-013, Variation AC.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small-body, lead-free components.

## 7.5. WB SOIC-16 Land Pattern

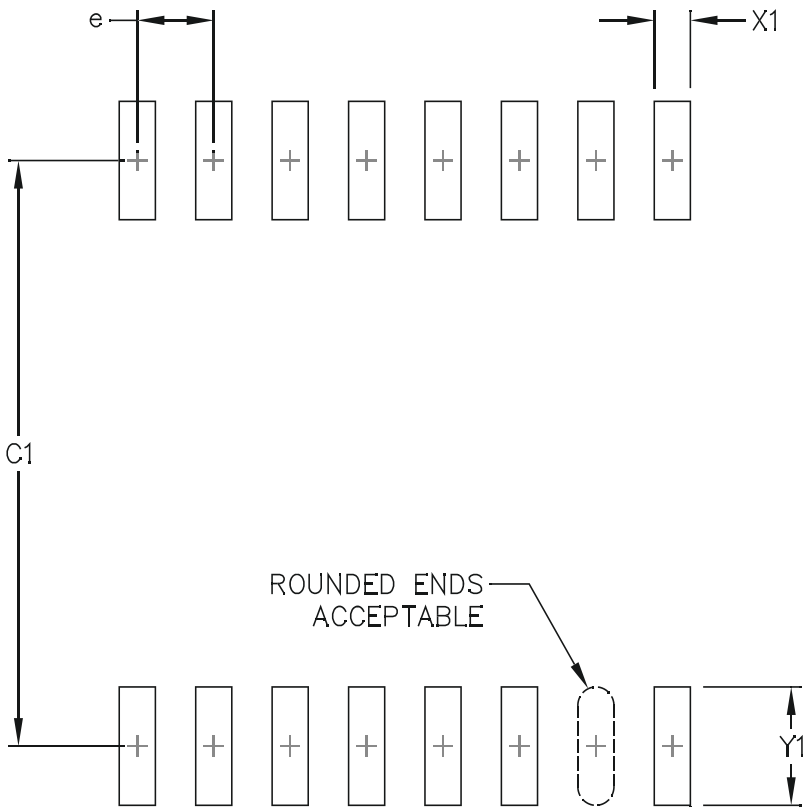


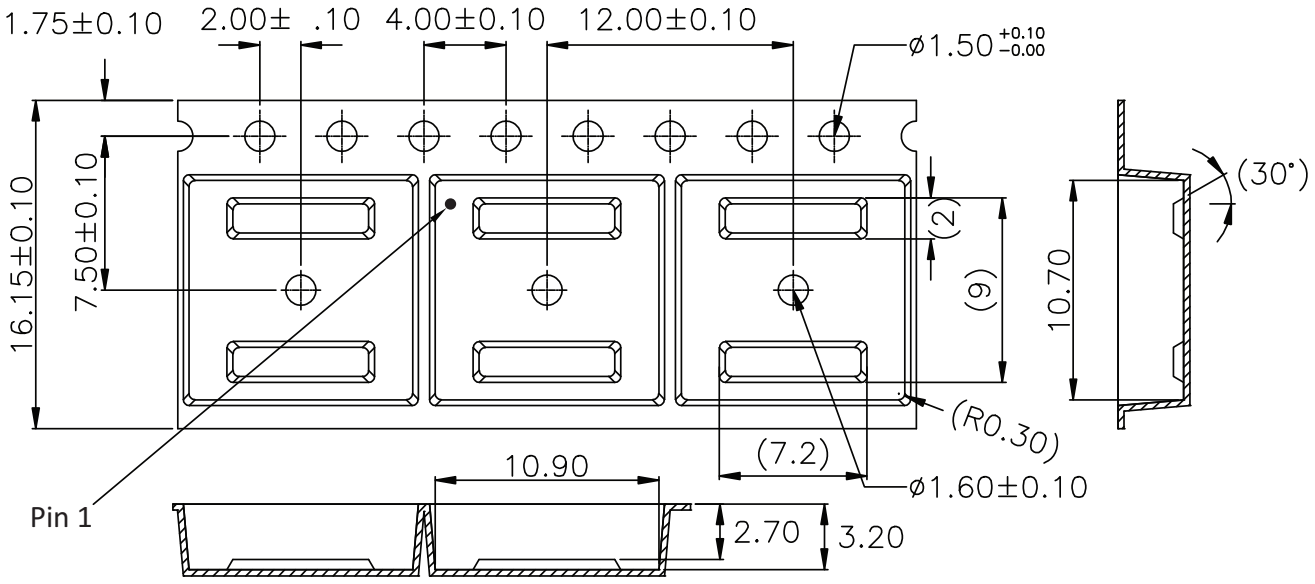

**Figure 67. WB SOIC-16 Land Pattern**

**Table 27. WB SOIC-16 Land Pattern Dimensions[1,2,3]**

| Dimension | Feature | mm |
|---|---|---|
| C1 | Pad column spacing | 9.40 |
| e | Pad row pitch | 1.27 |
| X1 | Pad width | 0.60 |
| Y1 | Pad length | 1.90 |

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 Pattern SOIC127P1032X265-16AN for Density Level B (median land protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

## 7.6. WB SOIC-16 Tape and Reel Information




NOTES
1. 10 sprocket hole pitch cumulative tolerance ±0.20 mm
2. All dimensions in mm

**Figure 68. WB SOIC-16 Carrier Tape Information**

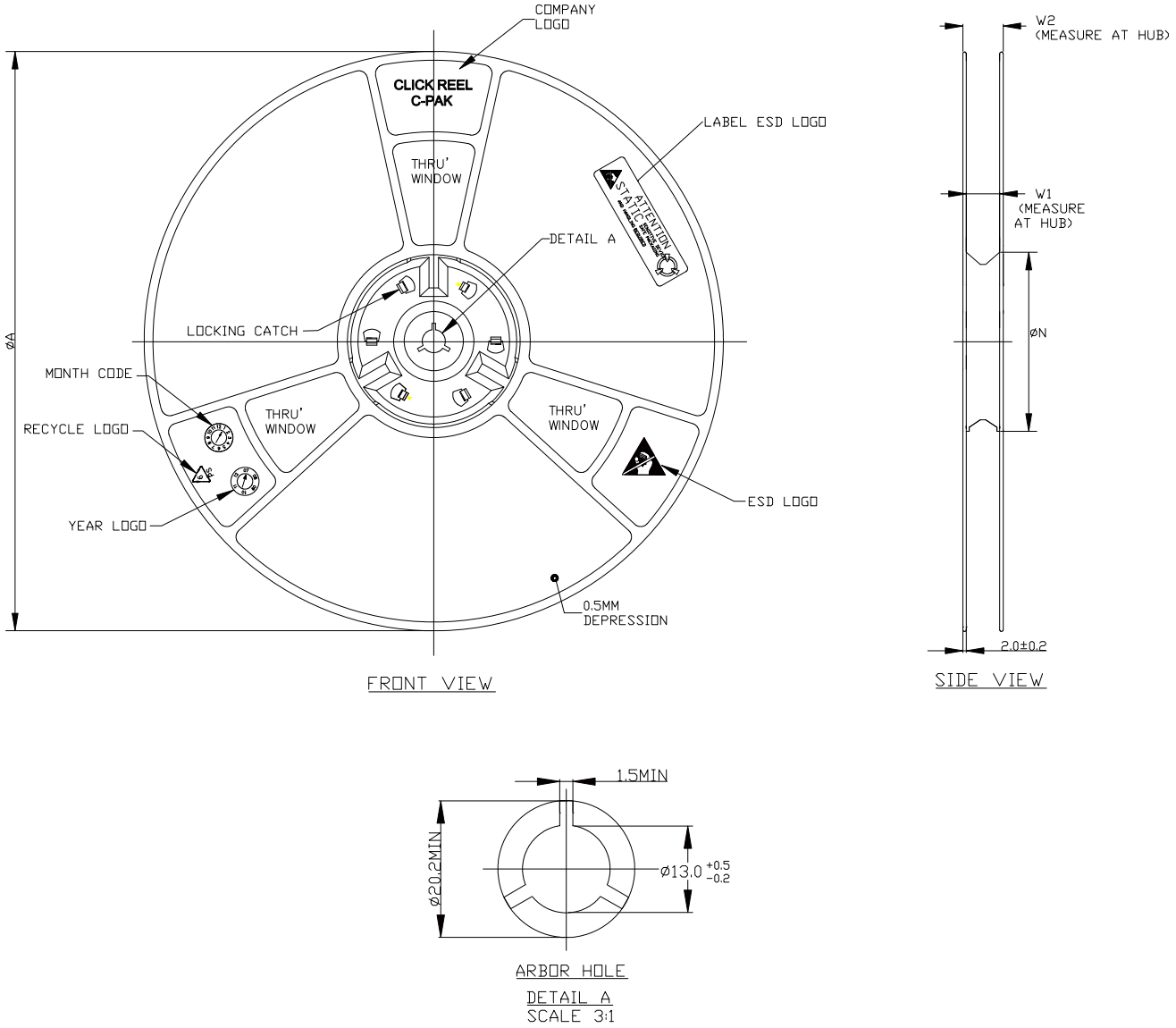



**Figure 69. WB SOIC-16 Reel Information**

## 7.7. WB SOIC-20 Land Pattern

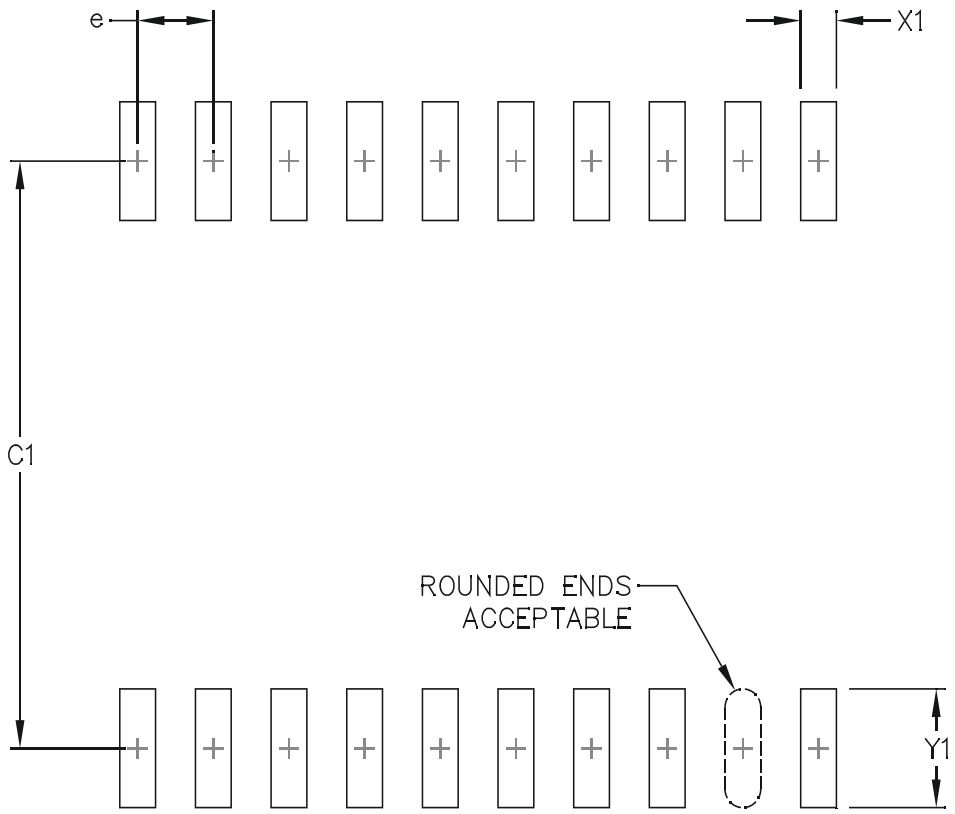


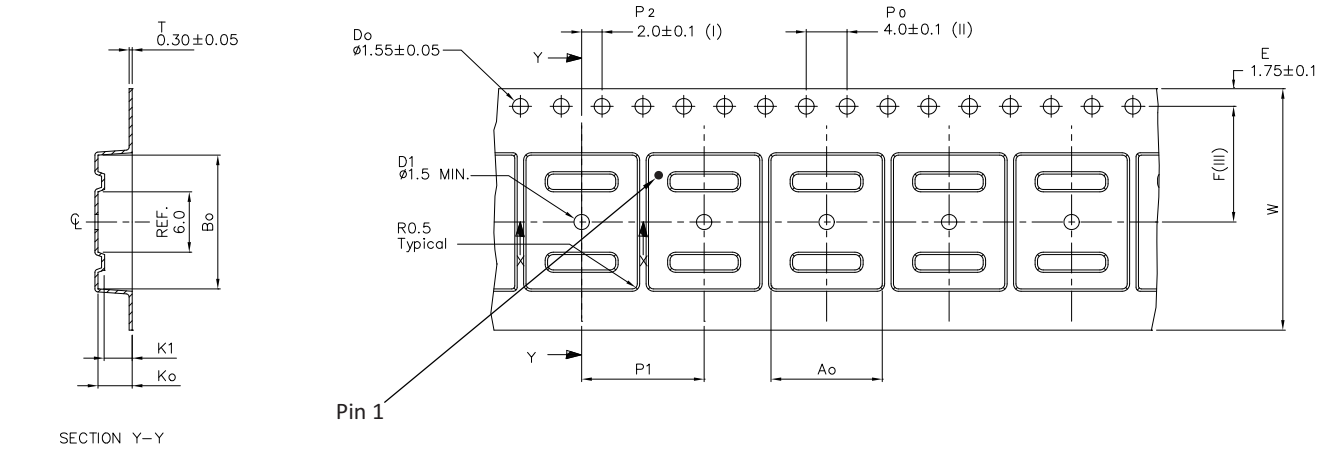

**Figure 70. WB SOIC-20 Land Pattern**

**Table 28. WB SOIC-20 Land Pattern Dimensions[1,2,3]**

| Dimension | Feature | mm |
|---|---|---|
| C1 | Pad column spacing | 9.40 |
| e | Pad row pitch | 1.27 |
| X1 | Pad width | 0.60 |
| Y1 | Pad length | 1.90 |

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 design guidelines for Density Level B (median land protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

## 7.8. WB SOIC-20 Tape and Reel Information




| | |
|---|---|
| Ao | 10.90 +/– 0.1 |
| Bo | 13.30 +/– 0.1 |
| Ko | 3.20 +/– 0.1 |
| K1 | 2.70 +/– 0.1 |
| F | 11.50 +/– 0.1 |
| P1 | 12.00 +/– 0.1 |
| W | 24.00 +0.3/– 0.0 |

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

**Figure 71. WB SOIC-20 Carrier Tape Information**

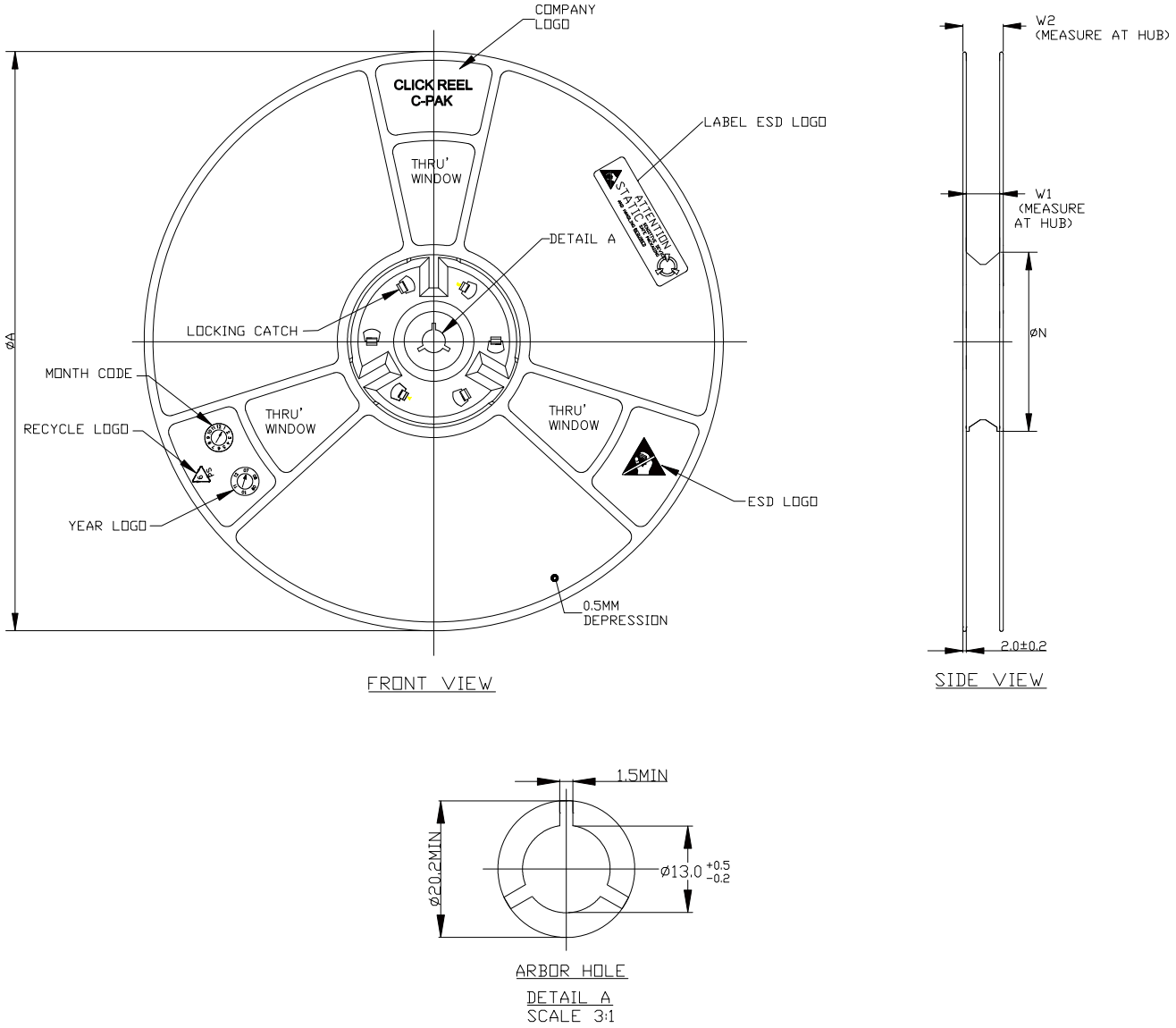



**Figure 72. WB SOIC-20 Reel Information**

# 8. Ordering Information

**Table 29. Si86Px Ordering Information[1,2,3,4,5]**

| Ordering Part Number (OPN) | Input Supply Voltage (V) | Output Supply Voltage (V) | Forward Channels (Primary Side) | Reverse Channels (Secondary Side) | Default Output State | Isolation Rating | Package Type |
|---|---|---|---|---|---|---|---|
| **WB SOIC-16 Package Options** | | | | | | | |
| Si86P320BC-IS | 3.3 | 3.3 | 2 | 0 | Low | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P320EC-IS | 3.3 | 3.3 | 2 | 0 | High | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P321BC-IS | 3.3 | 3.3 | 1 | 1 | Low | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P321EC-IS | 3.3 | 3.3 | 1 | 1 | High | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P420BC-IS | 3.3 to 5.0 (continuous) | 3.3 | 2 | 0 | Low | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P420EC-IS | 3.3 to 5.0 (continuous) | 3.3 | 2 | 0 | High | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P421BC-IS | 3.3 to 5.0 (continuous) | 3.3 | 1 | 1 | Low | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P421EC-IS | 3.3 to 5.0 (continuous) | 3.3 | 1 | 1 | High | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P520BC-IS | 5.0 | 3.3, 5.0 | 2 | 0 | Low | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P520EC-IS | 5.0 | 3.3, 5.0 | 2 | 0 | High | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P521BC-IS | 5.0 | 3.3, 5.0 | 1 | 1 | Low | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| Si86P521EC-IS | 5.0 | 3.3, 5.0 | 1 | 1 | High | 3.75 $kV_{RMS}$ | WB SOIC-16 |
| **WB SOIC-20 Package Options** | | | | | | | |
| Si86P340BC-IS | 3.3 | 3.3 | 4 | 0 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P340EC-IS | 3.3 | 3.3 | 4 | 0 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P341BC-IS | 3.3 | 3.3 | 3 | 1 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P341EC-IS | 3.3 | 3.3 | 3 | 1 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P342BC-IS | 3.3 | 3.3 | 2 | 2 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P342EC-IS | 3.3 | 3.3 | 2 | 2 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P440BC-IS | 3.3 to 5.0 (continuous) | 3.3 | 4 | 0 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P440EC-IS | 3.3 to 5.0 (continuous) | 3.3 | 4 | 0 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P441BC-IS | 3.3 to 5.0 (continuous) | 3.3 | 3 | 1 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P441EC-IS | 3.3 to 5.0 (continuous) | 3.3 | 3 | 1 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P442BC-IS | 3.3 to 5.0 (continuous) | 3.3 | 2 | 2 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P442EC-IS | 3.3 to 5.0 (continuous) | 3.3 | 2 | 2 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |

**Table 29. Si86Px Ordering Information[1,2,3,4,5] (Continued)**

| Ordering Part Number (OPN) | Input Supply Voltage (V) | Output Supply Voltage (V) | Forward Channels (Primary Side) | Reverse Channels (Secondary Side) | Default Output State | Isolation Rating | Package Type |
|---|---|---|---|---|---|---|---|
| Si86P540BC-IS | 5.0 | 3.3, 5.0 | 4 | 0 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P540EC-IS | 5.0 | 3.3, 5.0 | 4 | 0 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P541BC-IS | 5.0 | 3.3, 5.0 | 3 | 1 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P541EC-IS | 5.0 | 3.3, 5.0 | 3 | 1 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P542BC-IS | 5.0 | 3.3, 5.0 | 2 | 2 | Low | 3.75 $kV_{RMS}$ | WB SOIC-20 |
| Si86P542EC-IS | 5.0 | 3.3, 5.0 | 2 | 2 | High | 3.75 $kV_{RMS}$ | WB SOIC-20 |

1. “Si” and “SI” are used interchangeably.
2. An “R” at the end of the ordering part number indicates tape-and-reel packaging option.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to JEDEC industry-standard classifications and peak solder temperatures.
4. Automotive-grade devices (with an “-A” suffix) are identical in construction materials and electrical parameters to their Industrial-grade (with an “-I” suffix) version counterparts. Automotive-grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. Automotive-grade part numbers are included on shipping labels.
5. In top markings, the manufacturing code represented by either “TTTTT” or “TTTTTT” contains, as its first character, a letter in the range A through M to indicate industrial-grade or N through Z to indicate automotive-grade.

## 9. Revision History

| Revision | Date | Description |
|---|---|---|
| A | March, 2026 | Initial release. |

Copyright © 2026, Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc., and its subsidiaries (“Skyworks”) products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks’ Terms and Conditions of Sale.

THE INFORMATION IN THIS DOCUMENT AND THE MATERIALS AND PRODUCTS DESCRIBED THEREIN ARE PROVIDED “AS IS” WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not designed, intended, authorized, or warranted for use or inclusion in life support or life endangering applications, devices, or systems where failure or inaccuracy might cause death or personal injury. Skyworks customers agree not to use or sell the Skyworks products for such applications, and further agree to, without limitation, fully defend, indemnify, and hold harmless Skyworks and its agents from and against any and all actions, suits, proceedings, costs, expenses, damages, and liabilities including attorneys' fees arising out of or in connection with such improper use or sale.

Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks’ published specifications or parameters. Customers are solely responsible for their products and applications using the Skyworks products.

“Skyworks” and the Skyworks Starburst logo are registered trademarks of Skyworks Solutions, Inc., in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.