Si5347/46 Dual/Quad DSPLL Any-Frequency, Any-Output Jitter Attenuators

Frequently Asked Questions

This document is an attempt to answer some of the most frequently asked Si5347/46 questions in one place. If you do not find the answers you are looking for, you may contact Silicon Labs technical support at <http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>.

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# PCB Design and Layout Guidance

## Where can I find the IBIS model for the Si5347/46?

Silicon Labs clocks and oscillators IBIS models are available in the online Document Library search tool.

<http://www.silabs.com/support/resources.p-timing?query=IBIS>

## Where can I find the Si5347/46 schematic footprints and symbols?

Silicon Labs clocks and oscillators schematic footprints and symbols are available in the online Document Library search tool.

<http://www.silabs.com/support/resources.ct-schematic-and-layout-files.p-timing>

## Where can I find the package and PCB footprint information?

Please refer to the [Si5347/46 Datasheet](http://www.silabs.com/documents/public/data-sheets/Si5347-46-D-DataSheet.pdf) for package and footprint information.

## Do you have layout recommendations I should follow?

Yes. Please refer to the [*Si5347,Si5346 Rev.D Family Reference Manual*](http://www.silabs.com/documents/public/reference-manuals/Si5347-46-D-RM.pdf) for the crystal and device circuit layout recommendations.

## Do you have a list of recommended crystals?

Yes. Please refer to [*Si534x/8x Jitter Attenuators Recommended Crystals, TCXO and OCXOs Reference Manual*](https://www.silabs.com/documents/public/reference-manuals/si534x-8x-recommended-crystals-rm.pdf).

## I don’t want to use a crystal with the Si5347/46. Can I use an XO or TCXO as the XA/XB reference instead? And if so, how do I interface an external oscillator to the device?

Yes, but note that the XA/XB clock is the jitter reference for the device. The XO used must be a low phase noise / high-performance device to ensure clean output clocks. Please refer to:

1. [*AN905: Si534x External References; Optimizing Performance*](http://www.silabs.com/documents/public/application-notes/AN905.pdf),
2. [*Si534x/8x Jitter Attenuators Recommended Crystals, TCXO and OCXOs Reference Manual*](https://www.silabs.com/documents/public/reference-manuals/si534x-8x-recommended-crystals-rm.pdf) for a list of recommended crystals, XOs, TCXOs, and OCXOs, and
3. [*Si5347,Si5346 Rev.D Family Reference Manual*](http://www.silabs.com/documents/public/reference-manuals/Si5347-46-D-RM.pdf) for external reference clock connection options.

## Are there any power supply filtering requirements or recommendations?

It is recommended to use a 0402 1 μF ceramic capacitor on each power supply pin for optimal performance. If the supply voltage is extremely noisy, it might be necessary to use a ferrite bead in series between the supply voltage and the power supply pin.

## Is there any specific power supply sequencing requirement?

Four classes of supply voltages exist on the Si5347/46:

1. VDD = 1.8 V (Core digital supply)
2. VDDA = 3.3 V (Analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)
4. VDDS = 1.8/3.3 V ± 5% (Digital I/O supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. VDDS has no effect on output clock alignment.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT\_RST 0x001C[0] or Hard Reset 0x001E[1] register bits or driving the RSTB pin. Note that using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

## What serial interfaces does the device support?

I2C standard mode (100 kbps) and fast mode (400 kbps) are both supported. The device also supports both 3-wire and 4-wire SPI communication at a rate of up to 20MHz. Both I2C and SPI support I/O voltage of 1.8 V and 3.3 V.

Please consult the [[*Si5347,Si5346 Rev.D Family Reference Manual*](http://www.silabs.com/documents/public/reference-manuals/Si5347-46-D-RM.pdf)](https://www.silabs.com/documents/public/reference-manuals/Si5344H-42H-RM.pdf) and/or [*AN926: Reading and Writing Registers with SPI and I2C for Si534x/8x Devices*](http://www.silabs.com/documents/public/application-notes/AN926.pdf) for more information.

## How do I properly terminate input and output clocks?

Refer to the [[*Si5347,Si5346 Rev.D Family Reference Manual*](http://www.silabs.com/documents/public/reference-manuals/Si5347-46-D-RM.pdf)](https://www.silabs.com/documents/public/reference-manuals/Si5344H-42H-RM.pdf) for differential and single-ended input and output terminations. Be sure that there are no DC-connected shunt resistors on output pins. This is common for LVPECL but these devices do not support that termination scheme. Be sure to AC couple when necessary per the reference manual recommendations.

## Where can I get detailed material composition information on these devices?

Please refer to the Environmental Data Part Number search on the website for this information.

<http://www.silabs.com/support/quality/Pages/RoHSInformation.aspx>

## Is the part RoHS compliant?

Yes. Please refer to the Environmental Data Part Number search on the website for the certificate of compliance.

<http://www.silabs.com/support/quality/Pages/RoHSInformation.aspx>.

## What is the Moisture Sensitivity Level (MSL) rating for the Si5347/46?

These parts are shipped MSL 2.

## What is the recommend profile for solder reflow process?

The recommended reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# Frequency Plan and Clock Design Decisions

## What development software/tools do you have available to use with the Si5347/46?

The latest versions of ClockBuilder Pro, ClockBuilder Pro Project File Inspector, and other software development tools are available on the Silicon Labs website at <http://www.silabs.com/products/development-tools/software/clock>.

## Where can I find ClockBuilder Pro Documentation?

See the “CBPro Overview”, “CBPro Tools & Support for In-System Programming” and “CLI User’s Guide” on the ClockBuilder Pro Wizard home screen. The latter includes walkthroughs of frequency-on-the-fly and full/partial configuration programming scenarios

## How do I select proper jitter attenuation bandwidth?

This is a highly system-specific decision, requiring a careful balance and understanding of jitter attenuation v. jitter transfer. One place to start is to read the PLL Characteristics section of [*AN687: A Primer on Jitter, Jitter Measurement and Phase-Locked Loops*](http://www.silabs.com/documents/public/application-notes/AN687.pdf).

## Does the device support automatic input clock selection and does it support hitless switching?

Yes, please refer to the [*Si5347,Si5346 Rev.D Family Reference Manual*](http://www.silabs.com/documents/public/reference-manuals/Si5347-46-D-RM.pdf) and/or the [*AN1057: Hitless Switching using Si534x/8x Devices*](http://www.silabs.com/documents/public/application-notes/an1057-hitless-switching-using-si534x-8x.pdf) application note for more details.

## Is there a recommended full device programming procedure?

Yes. In some cases, the full procedure may not be needed in some cases, but the following is a general procedure recommended for most cases. (For Rev.D devices)

1. Preamble
	1. 0x0B24 = 0xC0
	2. 0x0B25 = 0x00
2. Wait 300 ms
3. Write all configuration registers
4. Soft reset and postamble
	1. 0x001C = 0x01
	2. 0x0B24 = 0xC3
	3. 0x0B25 = 0x02

## Can I change one output frequency without disturbing other output(s)?

Yes. This is what we called Frequency-On-The-Fly. See **Si5347 Frequency-On-The-Fly Example** slides 34-39 available from the ClockBuilder Pro Documentation -- “CBPro Tools & Support for In-System Programming”.

## Do I need to write pre-amble/post-amble for Frequency-On-The-Fly?

You need pre-amble/post-amble to write the base plan, but to switch among plans, do NOT write pre-amble or post-amble.

## Should I use Soft\_Rst\_All or Soft\_Rst\_DSPLLx for Frequency-On-The-Fly?

Use Soft\_Rst\_DSPLLx for the DSPLL that needs to be changed. You will have to manually write Px\_Update, Nx\_Update\_PLLx, and BW\_Update before the Soft\_Rst. These update bits can be found in the reference manual. However, if you use the CLI tool (follow the example in “CBPro Tools & Support for In-System Programming” or check out “CLI User’s Guide” for details), the generated script will include all register writes that are necessary.

## Do I need to update any divider if I write Soft\_Rst\_All?

No. But you need to write BW\_Update\_PLLx bits for modified DSPLL BWs (0x414[0],0x514[0],0x614[0],0x715[0] for DSPLLA,B,C,D respectively) before Soft\_Rst\_All.

## How do I do DCO mode?

Refer to app note [AN909: DCO Applications with the Si5347/46](https://www.silabs.com/documents/public/application-notes/AN909.pdf)

## Do I have to provide an input clock in DCO mode?

Yes.

## How do I calculate a frequency plan without CBPro?

Frequency planning is really complicated so we always recommend using CBPro. You can also use CLI tool (check out “CLI User’s Guide” for details) to generate multiple frequency plans. However if you have to calculated a frequency plan on demand, contact Silicon Labs technical support for specific cases.

## Does the Si5347/46 support Zero-Delay Buffer operation?

No.