PRODUCT SUMMARY

SKY4680x/xC: High-Performance Automotive Audio DSP

Applications

- Premium and mainstream automotive audio amplifiers
- OEM infotainment and head-unit systems
- Digital cockpit, zonal audio and multi-zone audio systems
- Centralized and distributed vehicle audio architectures
- Electric vehicle audio processing, active sound design and road noise cancellation systems
- Automotive voice enhancement, hands-free communication and Edge AI audio applications

Features

- Up to three programmable Cadence® HiFi 5 DSP cores clocked at 414. 72 MHz
  - Without customer-programmable MCU: One DSP core (SKY46801), two DSP cores (SKY46802) and three DSP cores (SKY46803)
  - With customer-programmable MCU: One DSP core (SKY46801C), two DSP cores (SKY46802C) and three DSP cores (SKY46803C)
- Integrated, customer-programmable Arm® Cortex®-M3 MCU (SKY4680xC parts only)
- Integrated shared and highly accessible 8 MB RAM
- Supported by the SLATE graphical programming environment for rapid audio system development
- Enables Skyworks Edge AI and third-party branded audio algorithms
- Autonomous self-boot from flash for accelerated time to audio
- Integrated asynchronous sample rate converters (ASRCs) for flexible audio clock-domain management
- Up to nine I^2S/TDM inputs and up to nine I^2S/TDM outputs
- Optional TDM mode with support for up to 32 input channels and up to 32 output channels
- Two SPI/I^2C ports
- Three SPI controllers (one with XIP for flash)
- JTAG/SWD, one I^2C controller, one UART
- 88-pin, 12 mm x 12 mm x 0.85 mm QFN with 0.5 mm pad pitch
- Moisture Sensitivity Level 2 (MSL2), 260 °C per JEDEC-J-STD-020
- Automotive temperature range of –40 to 105 °C
- AEC-Q100 qualified
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Description

The SKY4680x/xC family is a scalable automotive audio DSP platform designed for infotainment, digital cockpit, audio amplifier, and distributed vehicle audio applications. Available in pin-compatible configurations ranging from one (SKY46801/1C), two (SKY46802/2C), and three (SKY46803/3C) Cadence® HiFi 5 DSP cores, the SKY4680x/xC delivers the processing performance, memory capacity, and software flexibility required for next-generation automotive audio systems.

The SKY4680x/xC platform enables a broad range of audio applications, from traditional radio and infotainment audio processing to premium branded audio systems, immersive and spatial audio, active noise management, voice enhancement, communications processing, and Edge AI audio algorithms. A customer-programmable on-chip Arm® Cortex®-M3 MCU allows OEMs and Tier 1 suppliers to develop proprietary audio features and system control functions directly on the device, reducing software complexity and eliminating the need for additional processing resources.

Integrated on-chip SRAM eliminates the need for external DRAM, reducing PCB area, BOM cost, system power consumption, and design complexity. Combined with a scalable software architecture and flexible audio routing capabilities, the SKY4680x/xC provides a common platform that can be deployed across entry-level, mid-range, and premium vehicle programs while maintaining software reuse and reducing development effort.

The SKY4680x/xC supports comprehensive automotive audio connectivity, including multichannel I^2S and TDM interfaces. Flexible host interfaces support SPI and I^2C operation, while dedicated high-speed serial flash interfaces enable efficient boot, application storage, and software updates.

The SLATE graphical programming environment enables rapid development and customization of audio signal processing applications through a drag-and-drop design methodology. Engineers can create, configure, and optimize audio processing chains using a library of prevalidated audio functions, reducing software development effort and accelerating time-to-market.

The compact 12 mm × 12 mm QFN package, combined with the elimination of external DRAM, enables a highly optimized system design with reduced PCB area, lower BOM cost, and simplified implementation.

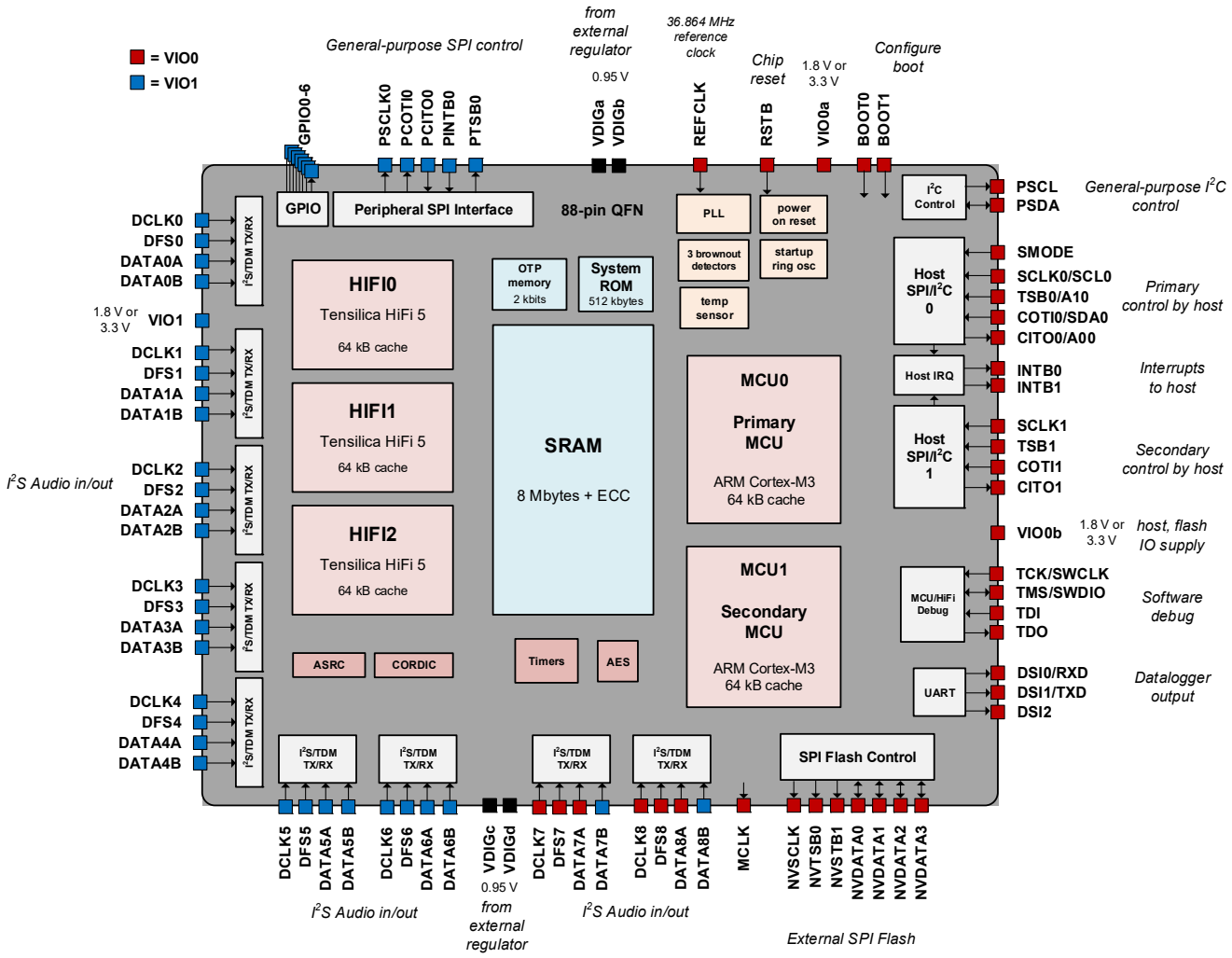


Figure 1. Functional Block Diagram

1. Pin Descriptions

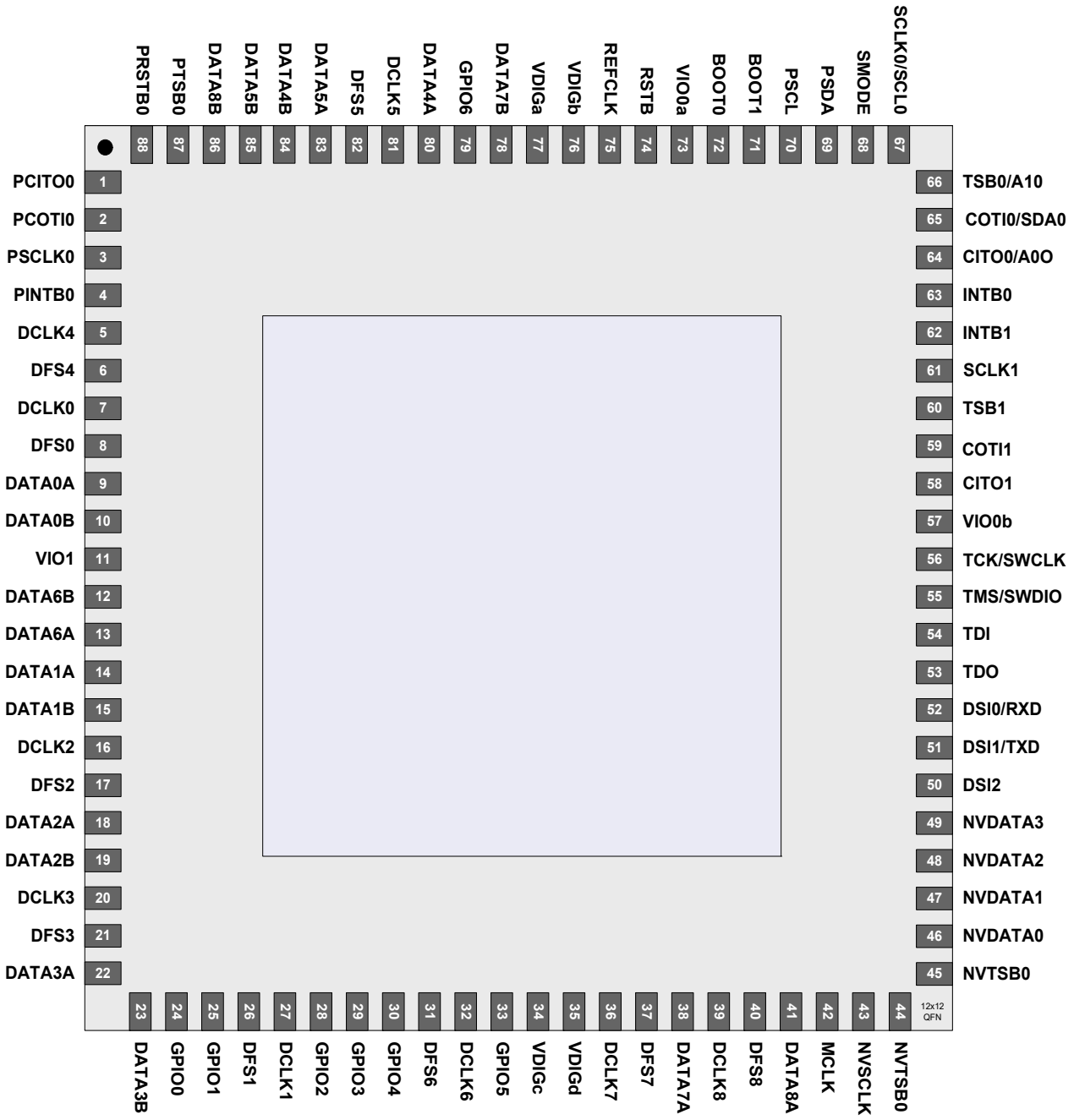


Figure 2. Pinout (Top View)

Table 1. SKY4680x/xC Pin Descriptions

Pin Number	Pin Name	Input/ Output	Power Domain	Description
1	PCITO0	I	VIO1	Peripheral SPI 0 data, controller in target out
2	PCOTI0	O	VIO1	Peripheral SPI 0 data, controller out target in
3	PSCLK0	O	VIO1	Peripheral SPI 0 clock
4	PINTB0	I/O	VIO1	Peripheral SPI 0 interrupt, active low
5	DCLK4	I/O	VIO1	Audio clock
6	DFS4	I/O	VIO1	Audio frame
7	DCLK0	I/O	VIO1	Audio clock
8	DFS0	I/O	VIO1	Audio frame
9	DATA0A	I/O	VIO1	Audio data
10	DATA0B	I/O	VIO1	Audio data
11	VIO1	Supply	VIO1	I/O supply for tuner interfaces
12	DATA6B	I/O	VIO1	Audio data
13	DATA6A	I/O	VIO1	Audio data
14	DATA1A	I/O	VIO1	Audio data
15	DATA1B	I/O	VIO1	Audio data
16	DCLK2	I/O	VIO1	Audio clock
17	DFS2	I/O	VIO1	Audio frame
18	DATA2A	I/O	VIO1	Audio data
19	DATA2B	I/O	VIO1	Audio data
20	DCLK3	I/O	VIO1	Audio clock
21	DFS3	I/O	VIO1	Audio frame
22	DATA3A	I/O	VIO1	Audio data
23	DATA3B	I/O	VIO1	Audio data
24	GPIO0	I/O	VIO1	GPIO
25	GPIO1	I/O	VIO1	GPIO
26	DFS1	I/O	VIO1	Audio frame
27	DCLK1	I/O	VIO1	Audio clock
28	GPIO2	I/O	VIO1	GPIO
29	GPIO3	I/O	VIO1	GPIO
30	GPIO4	I/O	VIO1	GPIO
31	DFS6	I/O	VIO1	Audio frame
32	DCLK6	I/O	VIO1	Audio clock
33	GPIO5	I/O	VIO1	GPIO
34	VDIGc	Supply	VDIG	Core/digital supply
35	VDIGd	Supply	VDIG	Core/digital supply

Table 1. SKY4680x/xC Pin Descriptions (Continued)

Pin Number	Pin Name	Input/ Output	Power Domain	Description
36	DCLK7	I/O	VIO0	Audio clock
37	DFS7	I/O	VIO0	Audio frame
38	DATA7A	I/O	VIO0	Audio data
39	DCLK8	I/O	VIO0	Audio clock
40	DFS8	I/O	VIO0	Audio frame
41	DATA8A	I/O	VIO0	Audio data
42	MCLK	I/O	VIO0	System clock for external I^2S peripheral
43	NVSCLK	O	VIO0	Serial flash SPI clock
44	NVTSB0	O	VIO0	Serial flash SPI target select 0, active low
45	NVTSB1	O	VIO0	Serial flash SPI target select 1, active low
46	NVDATA0	I/O	VIO0	Serial flash SPI data 0
47	NVDATA1	I/O	VIO0	Serial flash SPI data 1
48	NVDATA2	I/O	VIO0	Serial flash SPI data 2
49	NVDATA3	I/O	VIO0	Serial flash SPI data 3
50	DSI2	I/O	VIO0	Diagnostic and service interface
51	DSI1/TXD	I/O	VIO0	Diagnostic and service interface/UART transmit
52	DSI0/RXD	I/O	VIO0	Diagnostic and service interface/UART receive
53	TDO	O	VIO0	JTAG
54	TDI	I	VIO0	JTAG
55	TMS/SWDIO	I, I/O	VIO0	JTAG/serial wire debug I/O
56	TCK/SWCLK	I	VIO0	JTAG/serial wire debug clock
57	VIO0b	Supply	VIO0	I/O supply for host interfaces
58	CITO1	O/I	VIO0	Secondary host control SPI (1) data, controller-in/peripheral-out
59	COTI1	I, I/O	VIO0	Secondary host control SPI (1) data, controller-out/peripheral-in
60	TSB1	I	VIO0	Secondary host control SPI (1) target select, active low
61	SCLK1	I	VIO0	Secondary host control SPI (1) clock input
62	INTB1	I/O	VIO0	Host Interrupt 1, active low
63	INTB0	I/O	VIO0	Host Interrupt 0, active Low
64	CITO0/A00	O/I	VIO0	Primary host control SPI (0) data, controller-in/target-out/I^2C 0 A0 address select
65	COTI0/SDA0	I, I/O	VIO0	Primary host control SPI (0) data, controller-out/target-in/I^2C 0 data input/output
66	TSB0/A10	I	VIO0	Primary host control SPI (0) target select (active low)/I^2C 0 A1 address select
67	SCLK0/SCL0	I	VIO0	Primary host control SPI (0) clock input / I^2C 0 clock input
68	SMODE	I	VIO0	Set mode of primary host control serial port (0 = SPI, 1 = I^2C)
69	PSDA	I/O	VIO0	Peripheral data (I^2C device)
70	PSCL	O	VIO0	Peripheral clock (I^2C device)

Table 1. SKY4680x/xC Pin Descriptions (Continued)

Pin Number	Pin Name	Input/ Output	Power Domain	Description
71	BOOT1	I	VIO0	Boot control 1
72	BOOT0	I	VIO0	Boot control 0
73	VIO0a	Supply	VIO0	I/O supply for host interfaces
74	RSTB	I	VIO0	Host controlled reset, active low
75	REFCLK	I	VIO0	Reference clock
76	VDIGb	Supply	VDIG	Core/digital supply
77	VDIGa	Supply	VDIG	Core/digital supply
78	DATA7B	I/O	VIO1	Audio data
79	GPIO6	I/O	VIO1	GPIO
80	DATA4A	I/O	VIO1	Audio data
81	DCLK5	I/O	VIO1	Audio clock
82	DFS5	I/O	VIO1	Audio frame
83	DATA5A	I/O	VIO1	Audio data
84	DATA4B	I/O	VIO1	Audio data
85	DATA5B	I/O	VIO1	Audio data
86	DATA8B	I/O	VIO1	Audio data
87	PTSB0	O	VIO1	Peripheral 0 SPI target select, active low
88	PRSTB0	O	VIO1	Peripheral 0 reset, active low

2. Package Outline

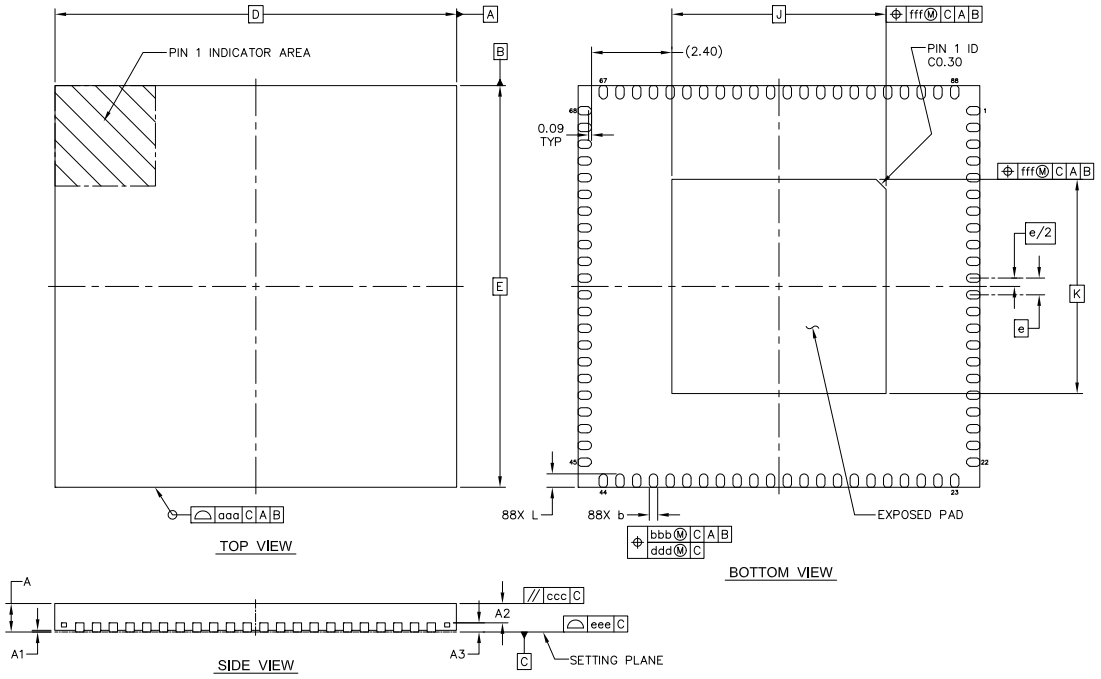


Figure 3. Package Dimensions

Table 2. Package Drawing Dimensions

Dimension	Min	Nom	Max
A	0.80 mm	0.85 mm	0.90 mm
A1	0.00 mm	—	0.05 mm
A2	—	0.65 mm	—
A3		0.203 REF	
b	0.20 mm	0.25 mm	0.30 mm
D		12.00 BSC	
E		12.00 BSC	
e		0.5 BSC	
J	6.30 mm	6.40 mm	6.50 mm
K	6.30 mm	6.40 mm	6.50 mm
L	0.35 mm	0.40 mm	0.45 mm
aaa		0.10 mm	
bbb		0.10 mm	
ccc		0.10 mm	
ddd		0.05 mm	
eee		0.08 mm	
fff		0.10 mm	

3. PCB Land Pattern

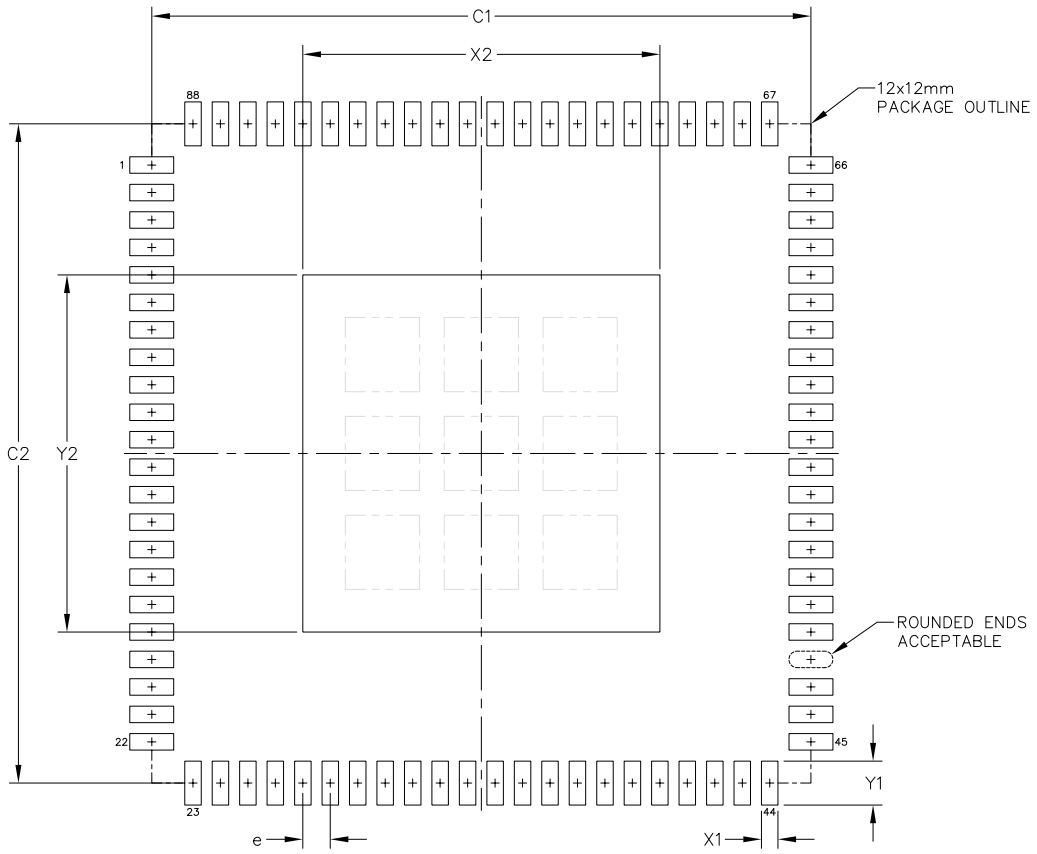


Figure 4. PCB Layout Footprint

Table 3. PCB Layout Footprint Dimensions

Dimension	Feature	mm	Notes
C1	Pad column spacing	12.00	**General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and tolerancing per ASME Y14.5M. 3. This land pattern is based on IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 0.060 mm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5.0 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 3 x 3 array of 1.35 mm square openings on a 1.80 mm pitch should be used for the center ground pad (shown in light lines above). **Card Assembly** 1. A no-clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
C2	Pad column spacing	12.00	
e	Pad row pitch	0.50 BSC	
X1	Pad width	0.30	
Y1	Pad length	0.80	
X2	Ground pad size	6.50	
Y2	Ground pad size	6.50	

4. Ordering Information

Table 4. SKY4680x Ordering Information

Part Number	Description	Package Type	Ambient Operating Temperature
SKY46801A1GE1AM	Single-core automotive audio DSP 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
SKY46801A1GC1AM	Single-core automotive audio DSP with customer-programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
SKY46802A1GE1AM	Dual-core automotive audio DSP 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
SKY46802A1GC1AM	Dual-core automotive audio DSP with customer-programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
SKY46803A1GE1AM	Triple-core automotive audio DSP 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
SKY46803A1GC1AM	Triple-core automotive audio DSP with customer-programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C

Table 5. SKY4680x Evaluation Hardware

Part Number	Description
SKY4680x-AADSP-EVB	Evaluation board for SKY4680x automotive audio DSP family

5. Revision History

Revision	Date	Description
A	November, 2026	Initial release.

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