

PRODUCT SUMMARY

SKY69115/SKY69116: NetSync™ Multi-PLL Synchronizer Clock

Applications

- Ethernet and optical core switches and routers
- Metro, access, and edge routers
- Single-board pizza box systems
- IEEE 1588 slave clocks (T-TSC, T-TSC-A, T-TSC-P)
- IEEE 1588 boundary clocks (T-TBC, T-TBC-A, T-TBC-P)
- IEEE 1588 grandmaster clocks (T-GM)
- O-RAN front-haul gateways and switches
- Wireless BBU and DU applications

Features

- Optimized for pizza box designs
- Programmable input-to-output delay
- Input-to-input and input-to-output delay measurements
- Integrated crystal reference (SKY69115 only)
- Integrated reprogrammable memory for power-up configuration, with factory pre-programming option (SKY69115 only)
- Temperature range –40 to +85 °C ambient
- Package options:
 - Thermally enhanced 10 x 10 mm 144-BGA (SKY69115)
 - Wettable-flank, 9 x 9 mm 64-QFN (SKY69116)
- Supports external TCXO/OCXO for low bandwidth operation and holdover
- ITU-T G.8262 and G.8262.1 Synchronous Internet (SyncE) compliant
- Supported by AccuTime™ synchronization software
- For RoHS and other product compliance information, see the [Skyworks Certificate of Conformance](#)

Description

The SKY69115/SKY69116 NetSync™ clocks are intended for pizza box-type applications or network synchronization applications in which time-of-day (ToD) is transferred independent of the DSPLL.

The SKY69115/SKY69116 uses sixth generation DSPLL® and MultiSynth™ technologies and an innovative multi-reference nested architecture to combine the functions of a network synchronizer and a jitter attenuator into a single device. The built-in crystal oscillator (SKY69115) or external XO (SKY69116) provides a low-jitter reference to the high performance PLL R.

An external OCXO or TCXO high-stability oscillator is used to support the low bandwidths needed for network synchronization functions, including Synchronous Ethernet and IEEE 1588 PTP, as well as providing extended holdover in the event of network sync failure.

A low-jitter mode is available for applications requiring jitter as low as 50 fs (12 kHz to 20 MHz) to allow direct connection to SERDES with speeds of 224 Gbps+ without needing additional jitter attenuators or buffers.

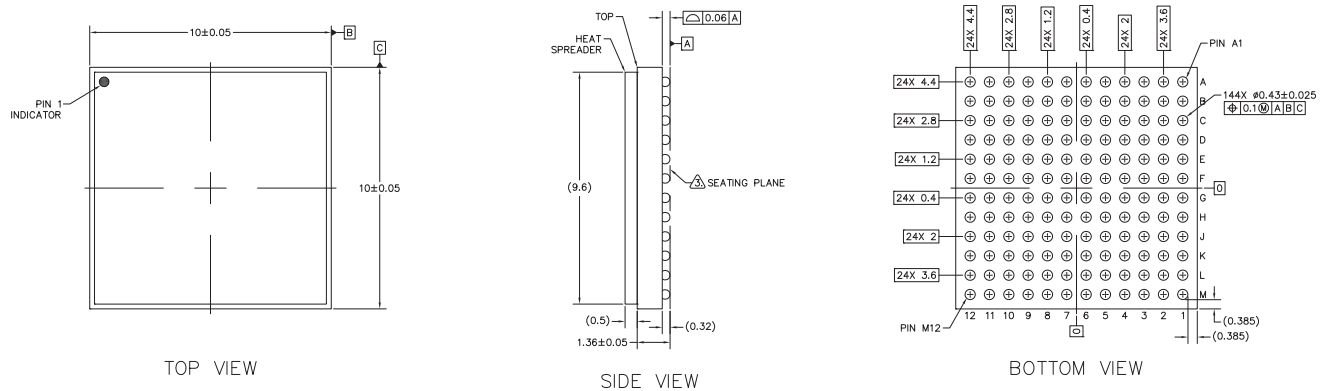
Integrated ToD counters are not supported on SKY69115/SKY69116. If integrated ToD is required for the DSPLL, refer to the SKY69110/SKY69112 and SKY69120/SKY69122 devices in the NetSync product family. The SKY69115/SKY69116 does, however, support embedded PPS and embedded SYNC (ePPS/eSYNC) input and output clocks.

Skyworks AccuTime software provides a complete synchronization software solution, including IEEE 1588 (PTP), for single and multi-processor pizza box architectures and complex blade-based systems.

Features

- Part of the NetSync network synchronizer clock family
- Utilizes 6th generation DSPLL and MultiSynth technologies
- Nested PLL architecture eliminates need for separate jitter attenuator in many applications
- Integrated crystal reduces external component count (SKY69115 only)
- Integrated flash memory supports in-field reprogramming of boot-up configuration (SKY69115 only)
- Orderable with factory-programmed custom configuration (SKY69115 only)
- Reference PLL (PLL R)
 - Provides reference to DSPLLs from the integrated VCO and crystal oscillator
 - Locks to external TCXO/OCXO to provide high-stability clock for low-bandwidth operation and holdover
 - Modulated by DSPLL A in low-jitter mode to support output jitter of 50 fs from Q-dividers
 - Programmable loop bandwidth from 20 Hz to 400 Hz
- Digital PLLs (DSPLL A, B, C, and D)
 - Four independent DSPLLs (DSPLLD only available on SKY69115)
 - Programmable loop bandwidth from 0.1 mHz to 4 kHz
 - Hitless input clock switching, automatic or manual input clock selection, and holdover mode
 - Compliant with ITU-T and other standards
 - Can lock to 1PPS and ePPS inputs, supports ref/sync pairs
 - Can generate 1PPS, ePPS, and PP2S outputs
 - Can be used as a MultiSynth fractional divider when not being used in DSPLL mode
 - Zero-delay mode (ZDM) utilizes external feedback to eliminate delay through DSPLL
- Additional MultiSynth NE (SKY69115 only)
 - One independent MultiSynth NE
 - Provides low-noise fractional division from PLL R or DSPLL D
 - Software/hardware controllable DCO with ppt-scale resolution
- SKY69115: Ten differential inputs and 14 differential outputs
 - Can be used as up to 15 single-ended inputs and 28 single-ended outputs total
- SKY69116: Nine differential inputs and nine differential outputs
 - Can be used as up to 13 single-ended inputs and 18 single-ended outputs total
- Flexible any-input, any-output frequency and format
 - Universal standard inputs
 - LVDS, S-LVDS, ac-coupled LVPECL, LVCMOS, slew-rate limited LVCMOS, HCSL, CML, custom differential
 - Output-to-output static delay adjustment (resolution, range): 20 ps, ± 10 ns
 - Output-output skew: ± 50 ps
 - Input-to-input and input-to-output delay measurement and delay adjust
- Status monitoring (LOS, OOF, PHMON, FLLO, and PLOL)
- On-chip temperature sensor and die temperature readout
- Serial interface: I²C or SPI (3 or 4-wire)
- Integrated MCU supports cross-product NetSync application programming interface (API) for device control
- ClockBuilder® Pro software tool simplifies device configuration
- Optional AccuTime host-based synchronization software
 - Field tested and proven PTP stack and time-recovery servo
 - Demonstration platform support with compliance reports

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM A AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 1. SKY69115 144-BGA with Heat Spreader Package Dimensions

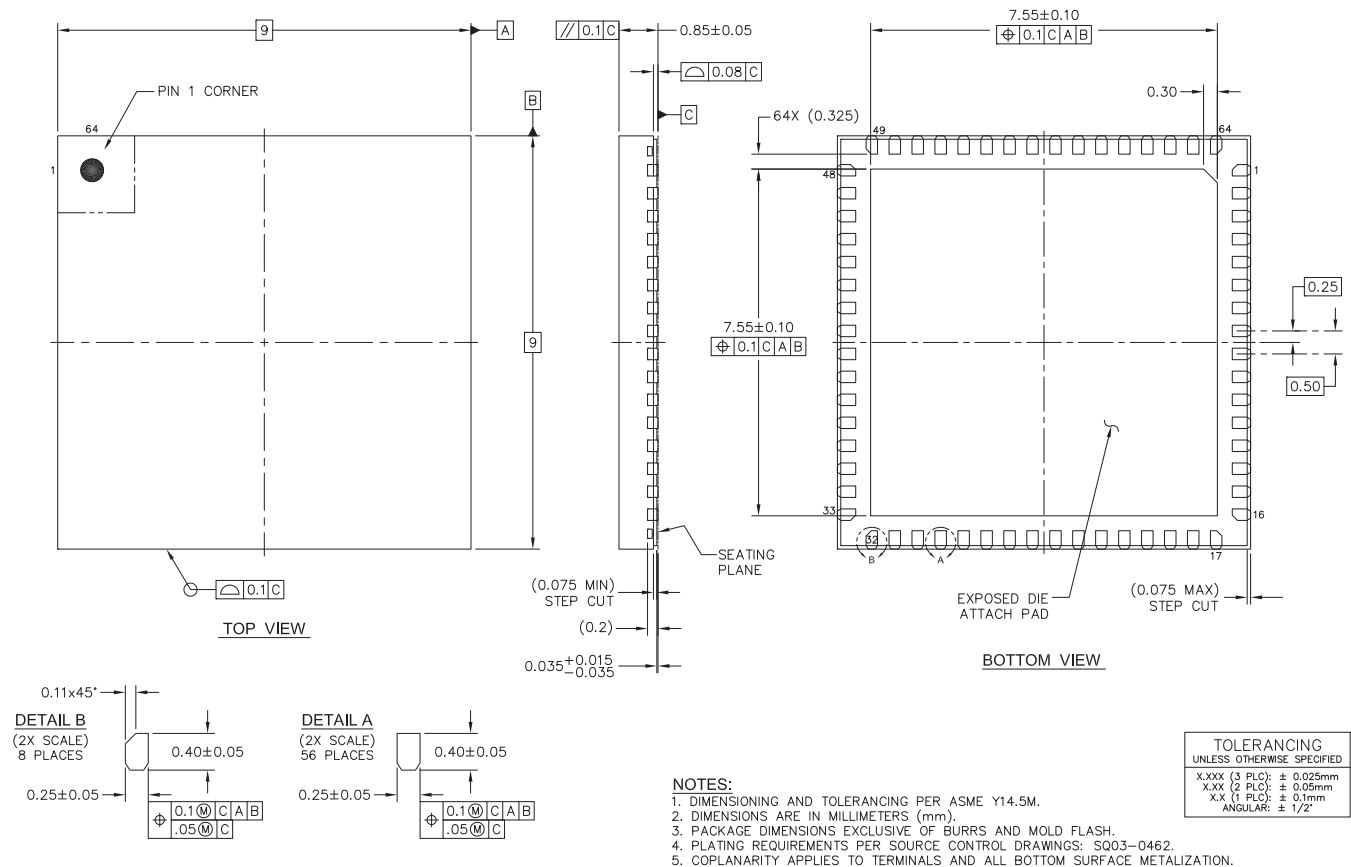
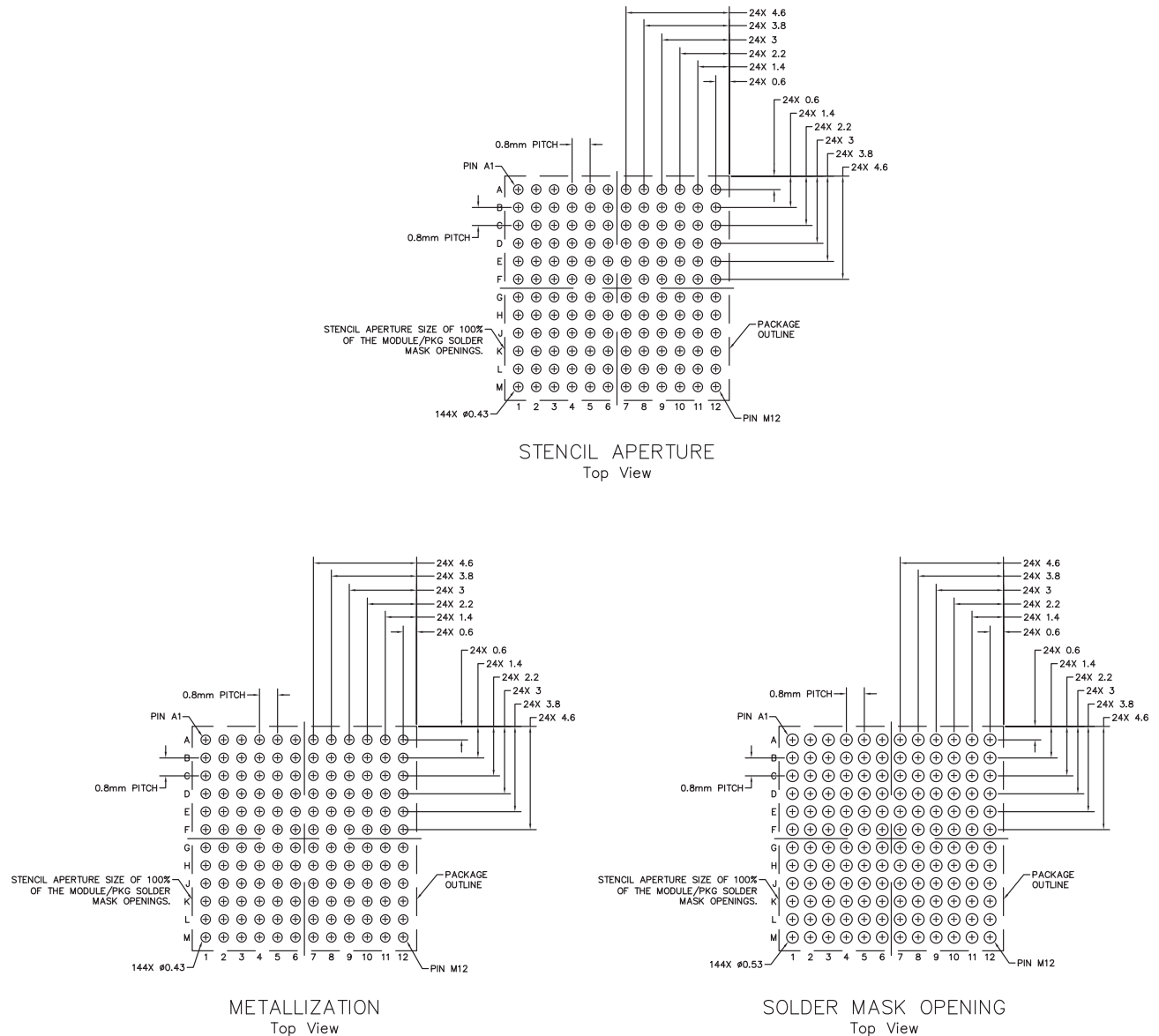


Figure 2. SKY69116 64-QFN Wettable Flank Package Dimensions

PCB Layout Footprint



Notes:

1. Dimensions are in millimeters, unless otherwise specified.
2. Thermal vias should be resin-filled and capped in accordance with IPC-4761 Type VII vias. 30 to 35 μm Cu thickness is recommended.

Figure 3. Recommended PCB Land Pattern, SKY69115 144-BGA

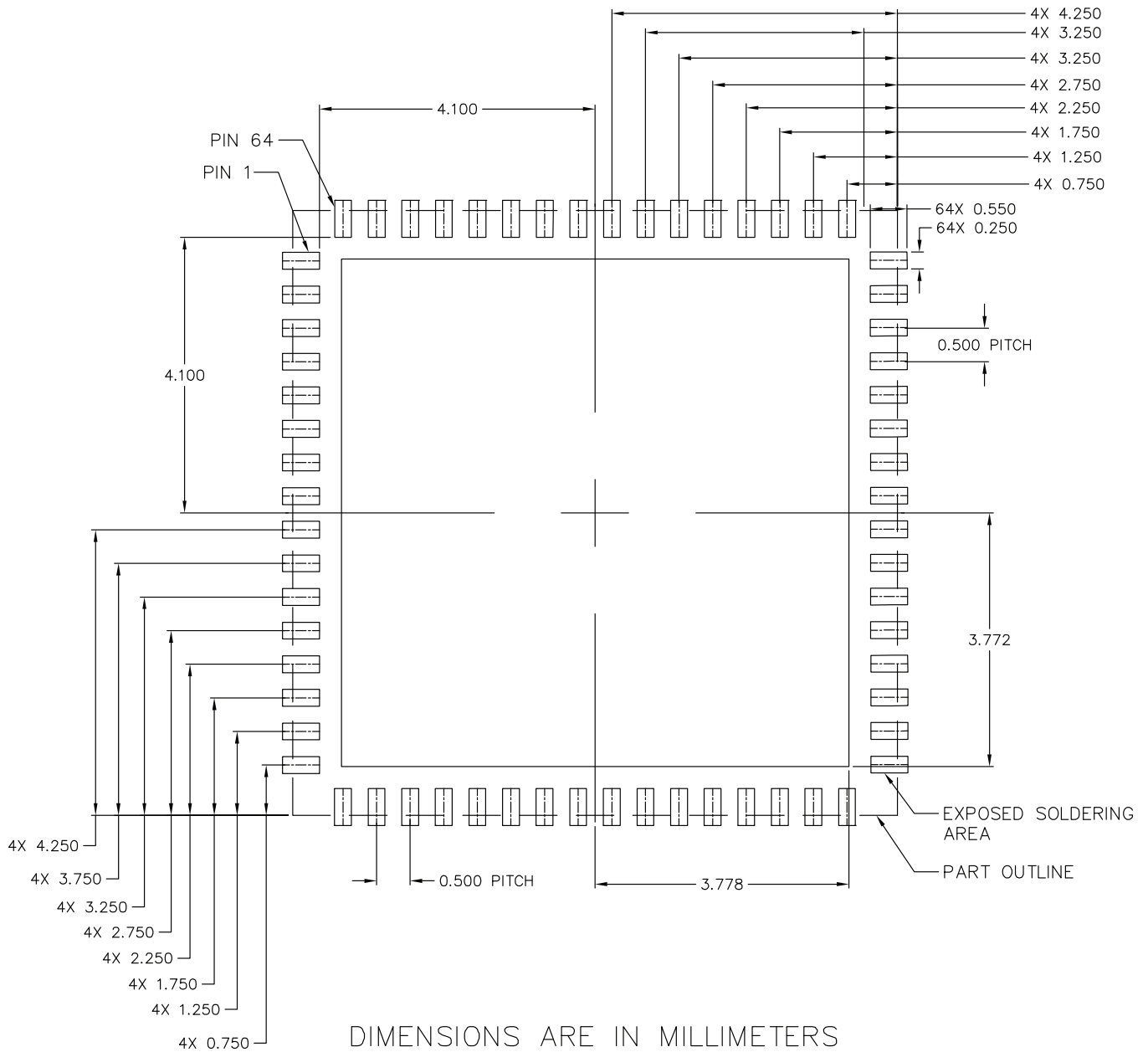


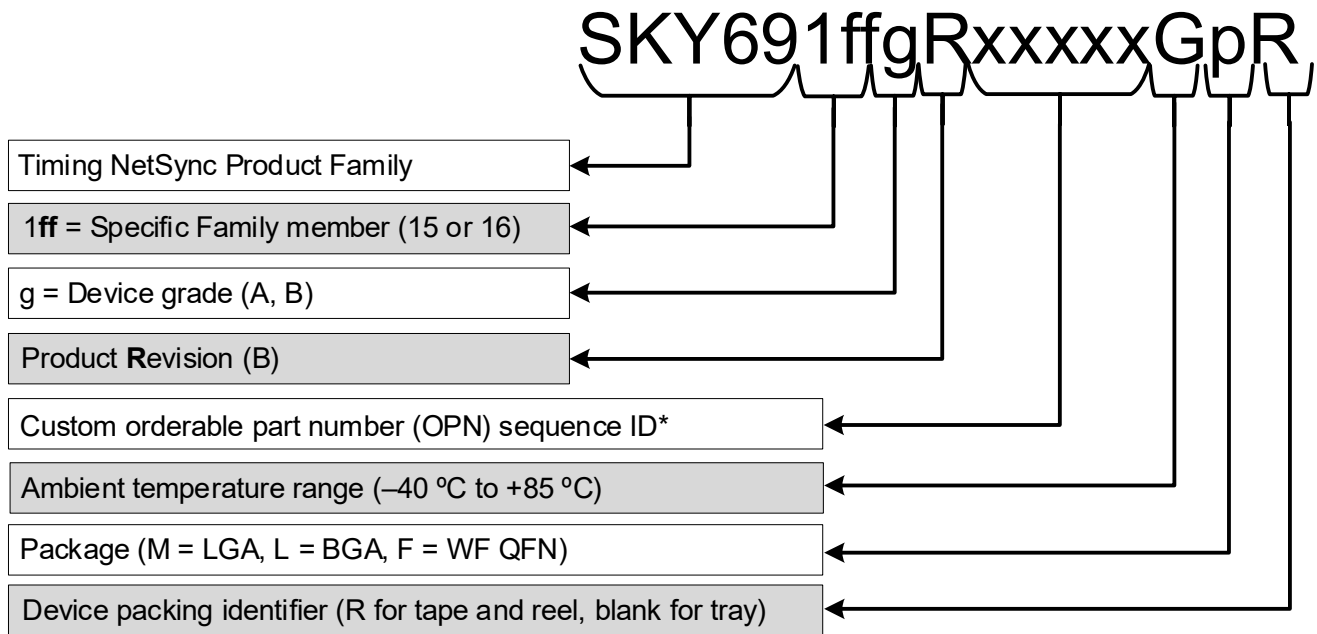
Figure 4. Recommended PCB Land Pattern, SKY69116 64-QFN Wettable Flank Package

Ordering Information

Table 1. SKY69115/SKY69116 Ordering Information

Orderable Part Number ^{1,2}	AccuTime™ IEEE 1588 Software Support ³	Package	Delivery Packing	Temperature Range
SKY69115ABxxxxxGL	No	144-ball BGA, 10 x 10 mm with heat spreader	Tray ⁴	–40 to 85 °C ambient ⁴ –40 to 105 °C board
SKY69115ABxxxxxGLR	No		Tape and reel ⁵	
SKY69115BBxxxxxGL	Yes		Tray ⁴	
SKY69115BBxxxxxGLR	Yes		Tape and reel ⁵	
SKY69116xxxxxxxxGfX <i>Contact Skyworks for ordering information</i>	–	64-lead, 9 x 9 mm wettable flank QFN	–	
SKY69115BB-BGA-EVB	Yes	–	–	Not specified

- 1. “xxxxx” should be replaced with the unique customer and/or application-specific sequence number created by ClockBuilder Pro or assigned by Skyworks.
- 2. For a given unique sequence number for SKY69115, the internal flash may be blank or factory programmed as defined within ClockBuilder Pro.
- 3. Use of AccuTime requires acceptance of a separate license agreement and may be subject to restrictions regarding supported platforms and applications.
- 4. Tray quantity = 50. Contact Skyworks for details about the tray format.
- 5. Reel quantity = 1000. Contact Skyworks for details about the reel format.



*5 digits; assigned by ClockBuilder Pro for Custom OPN devices.

Revision History

Revision	Date	Description
A	July, 2026	Initial release

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