

PRODUCT SUMMARY

SKY69120/SKY69122: Jitter Attenuator Clocks with Time-of-Day (ToD) Support

Applications

- Ethernet and optical core switches and routers
- Metro, access, and edge routers
- O-RAN front-haul gateways and switches
- Wireless BBU and DU applications
- IEEE 1588 slave clocks (T-TSC, T-TSC-A, T-TSC-P)
- IEEE 1588 boundary clocks (T-TBC, T-TBC-A, T-TBC-P)
- IEEE 1588 grandmaster clocks (T-GM)

Features

- Optimized for line card functions
- Companion to SKY69110/SKY69112 timing card NetSync™ devices
- Integrated time-of-day counters with multiwire ToDclk + FSync + ToD, or single-wire eToD or ePPS/eSYNC interface
- Compatible with multiple switch vendor products
- Programmable input-to-output delay
- Input-to-input and input-to-output delay measurements
- Integrated crystal reference (SKY69120 only)
- Integrated reprogrammable memory for power-up configuration, with factory pre-programming option (SKY69120 only)
- Temperature range –40 to +85 °C ambient
- Package options:
 - Thermally enhanced 10 x 10 mm 144-BGA (SKY69120)
 - Wettable-flank, 9 x 9 mm 64-QFN (SKY69122)
- Supported by AccuTime™ synchronization software
- For RoHS and other product compliance information, see the [Skyworks Certificate of Conformance](#)

Description

As networks evolve towards needing time alignment and distribution instead of the traditional frequency-only synchronization requirements, new challenges face designers, especially for multi-card systems. The SKY69120/SKY69122 NetSync™ jitter attenuation clocks are designed to support these network time and frequency synchronization demands.

The SKY69120/SKY69122 are targeted at line card applications for multi-blade systems or channel cards for wireless BBUs and DUs. These devices use 6th generation DSPLL® and MultiSynth™ technologies and an innovative nested PLL architecture to provide ultra-low jitter and frequency flexibility. The combination of technology and architecture enables the SKY69120/22 to achieve output jitter performance as low as 50 fs (12 kHz to 20 MHz) to support next generation SERDES rates up to 224Gbps+.

The SKY69120 offers an integrated crystal oscillator that provides a low-jitter reference to the high performance PLL R enabling the ultra-low output jitter. The SKY69122 is paired with an external XO. The low-jitter and large output count allow for direct connection to PHYs and switches without needing additional jitter attenuators or buffers. The devices also support additional DSPLLs for jitter attenuation and clock synthesis.

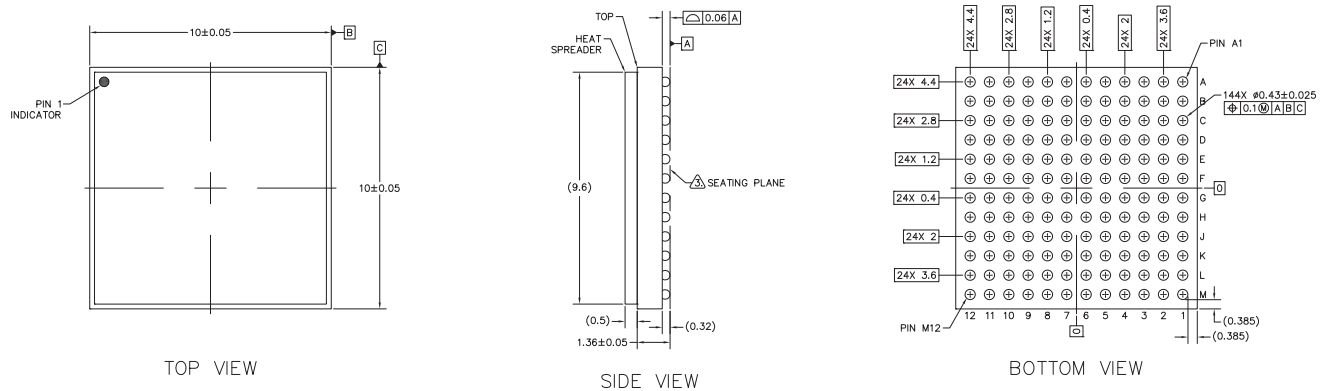
The SKY69120/22 include integrated time-of-day counters and timestampers and support flexible PWM-based formats for ToD and clock transmission over reduced pin-count connections (eToD), making them ideal for IEEE 1588 PTP applications.

Skyworks AccuTime software provides a complete synchronization software solution, including IEEE 1588 (PTP), for single and multi-processor pizza box architectures and complex blade-based systems.

Features

- Part of the NetSync jitter attenuator clock family
- Utilizes 6th generation DSPLL and MultiSynth technologies
- Integrated crystal reduces external component count (SKY69120 only)
- Integrated flash memory supports in-field reprogramming of boot-up configuration (SKY69120 only)
- Orderable with factory-programmed custom configuration (SKY69120 only)
- High-Performance PLL R
 - Provides reference to DSPLLs from the integrated VCO and crystal oscillator
 - Generates low-jitter clock outputs with jitter of 50 fs from Q dividers
 - Programmable loop bandwidth from 20 Hz to 400 Hz
 - Hitless input clock switching and automatic or manual input clock selection
 - Automatic free-run, locked and holdover mode switching
- Digital PLLs (DSPLL B, C, D for SKY69120 and DSPLL B, C for SKY69122)
 - Three independent DSPLLs
 - Programmable loop bandwidth from 20 Hz to 4 kHz
 - Hitless input clock switching, automatic or manual input clock selection, and holdover mode
 - Can generate 1PPS, ePPS, and PP2S outputs, supports ref/sync pairs
 - Can be used as a MultiSynth fractional divider when not being used in DSPLL mode
 - Zero-delay mode utilizes external feedback to eliminate delay through DSPLL
- Additional MultiSynth NA and MultiSynth NE (SKY69120 only)
 - One independent MultiSynth NE
 - Provides low-noise fractional division from PLL R or DSPLL D
 - Software/hardware controllable DCO with ppt-scale resolution
- SKY69120: Ten differential inputs and 14 differential outputs
 - Can be used as up to 15 single-ended inputs and 28 single-ended outputs total
- SKY69122: Nine differential inputs and nine differential outputs
 - Can be used as up to 13 single-ended inputs and 18 single-ended outputs total
- Flexible any-input, any-output frequency and format
 - Universal standard inputs
 - LVDS, S-LVDS, ac-coupled LVPECL, LVCMOS, slew-rate limited LVCMOS, HCSL, CML, custom differential
 - Output-to-output static delay adjustment (resolution, range): 20 ps, ± 10 ns
 - Output-output skew: ± 50 ps
- Status monitoring (LOS, OOF, PHMON, FLOL, and PLOL)
- Time-of-day (ToD) handling
 - Three 96-bit ToD counters (SKY69120), two 96-bit ToD counters (SKY69122)
 - Flexible PWM ToD encoders and decoders
 - Input-to-input and input-to-output delay measurement and delay adjust
- On-chip temperature sensor and die temperature readout
- Serial interface: I²C or SPI (3- or 4-wire)
- Integrated MCU supports cross-product NetSync application programming interface (API) for device control
- ClockBuilder® Pro software tool simplifies device configuration
- Optional AccuTime host-based synchronization software
 - Field tested and proven PTP stack and time-recovery servo
 - Demonstration platform support with compliance reports

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM A AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 1. SKY69120 144-BGA with Heat Spreader Package Dimensions

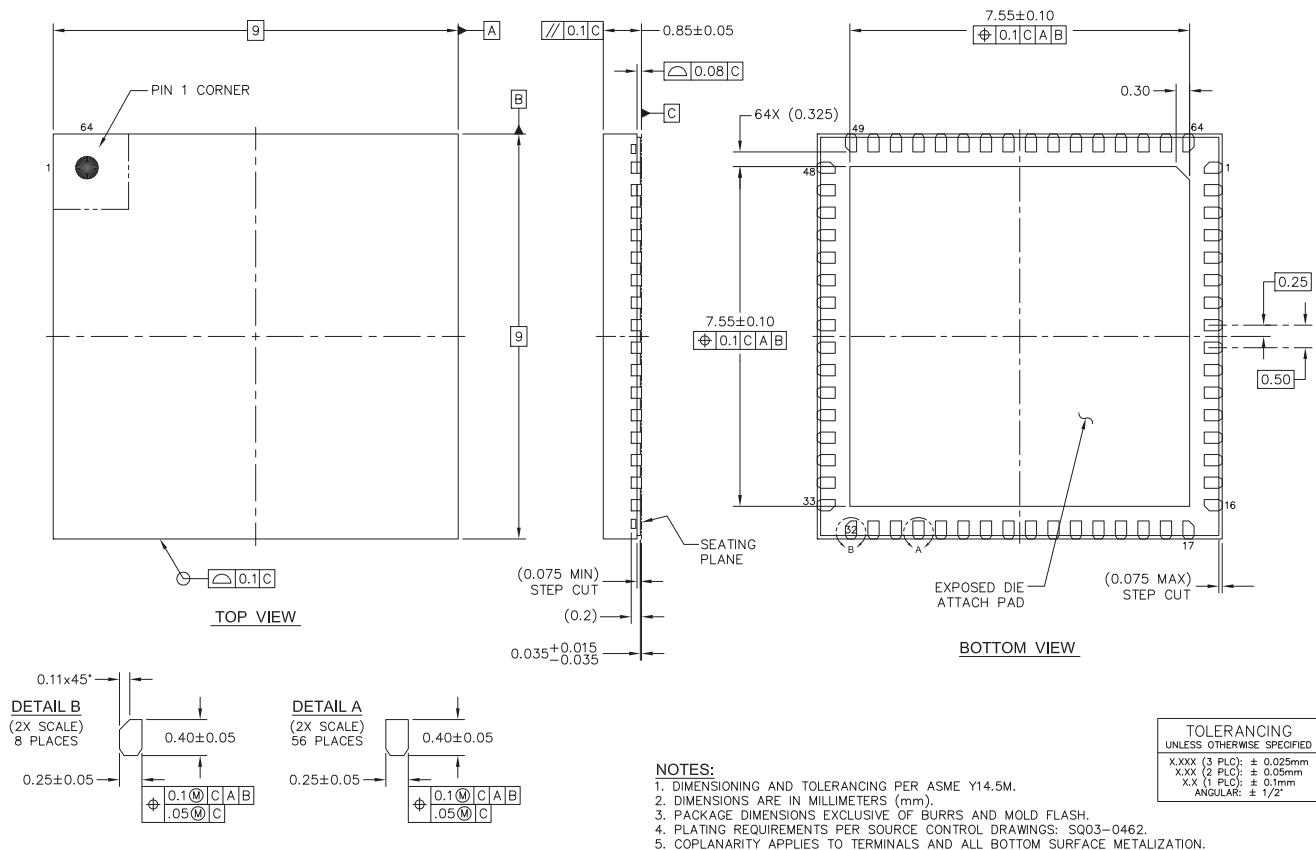


Figure 2. SKY69122 64-QFN Wettable Flank Package Dimensions

PCB Layout Footprint



Notes:

1. Dimensions are in millimeters, unless otherwise specified.
2. Thermal vias should be resin-filled and capped in accordance with IPC-4761 Type VII vias. 30 to 35 μm Cu thickness is recommended.

Figure 3. Recommended PCB Land Pattern, SKY69120 144-BGA

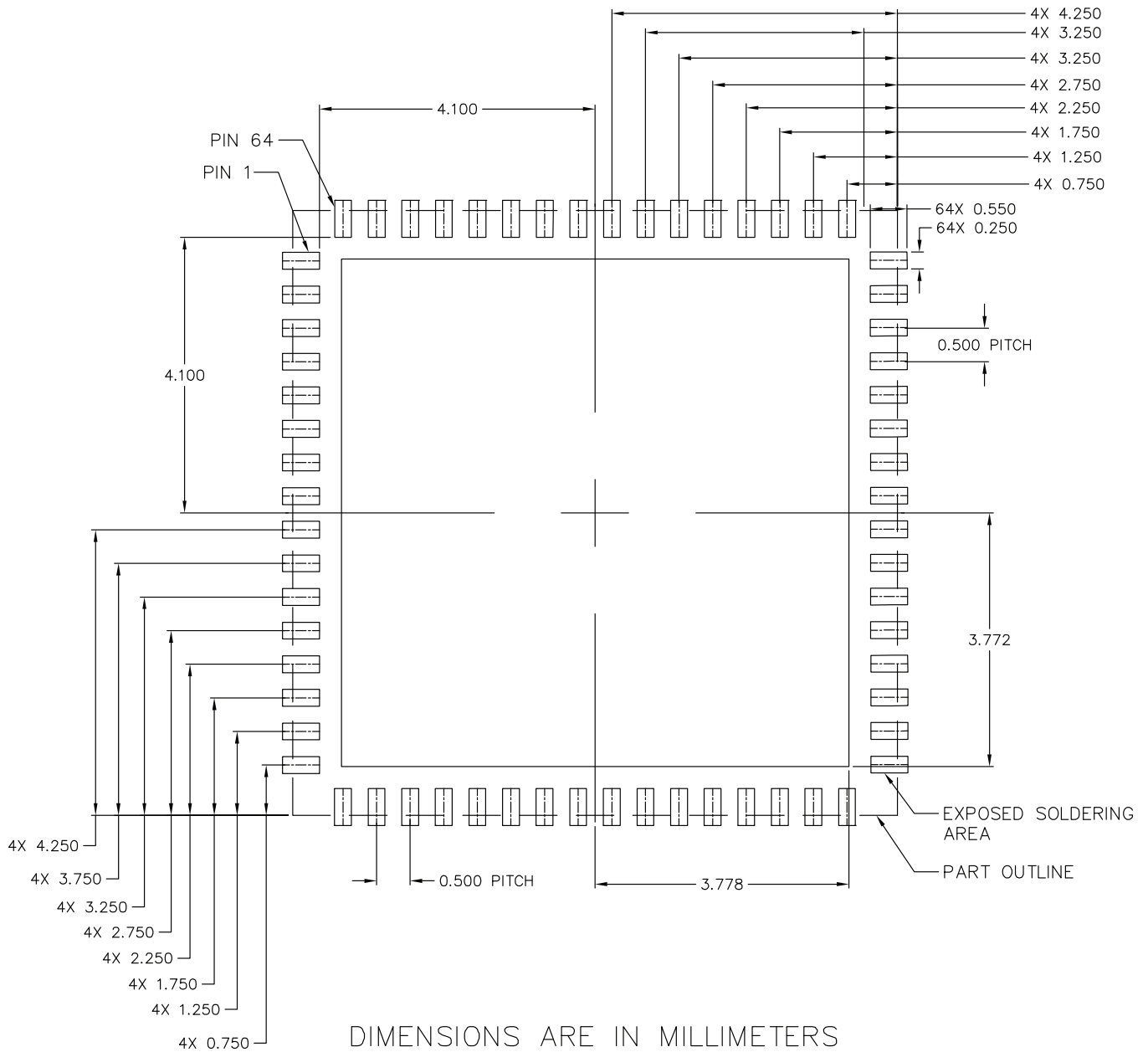


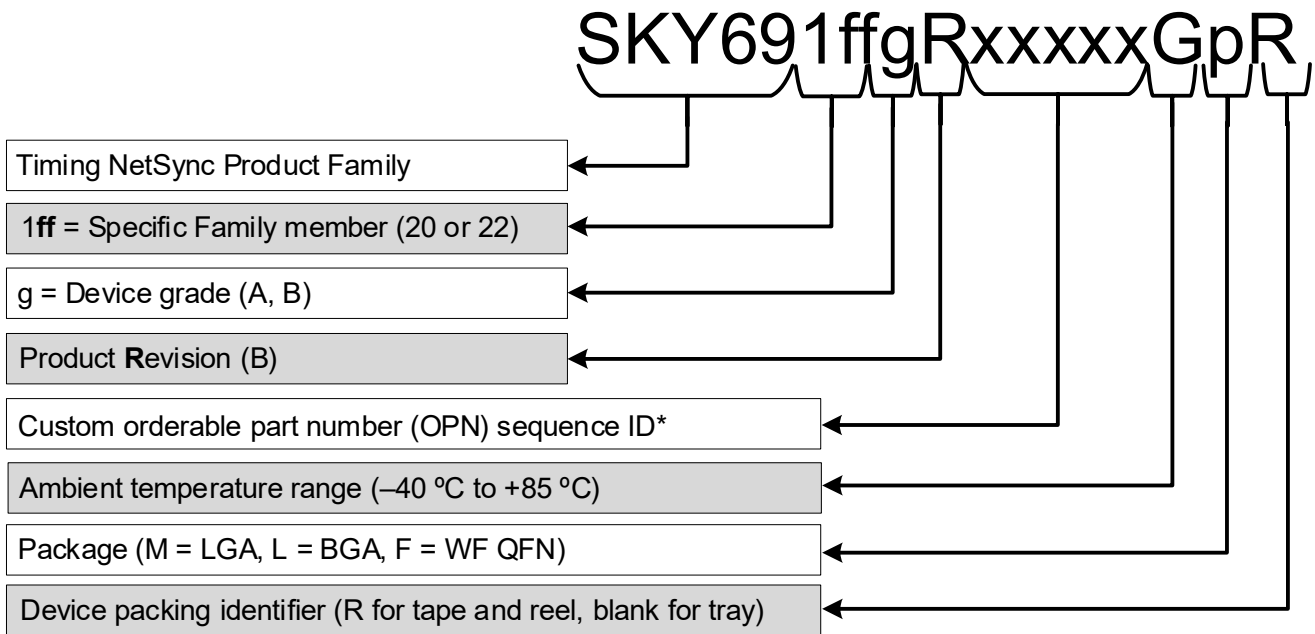
Figure 4. Recommended PCB Land Pattern, SKY69122 64-QFN Wettable Flank Package

Ordering Information

Table 1. SKY69120/SKY69122 Ordering Information

Orderable Part Number ^{1,2}	AccuTime™ IEEE 1588 Software Support ³	Package	Delivery Packing	Temperature Range
SKY69120ABxxxxGL	No	144-ball BGA, 10 x 10 mm with heat spreader	Tray ⁴	–40 to 85 °C ambient ⁴ –40 to 105 °C board
SKY69120ABxxxxGLR	No		Tape and reel ⁵	
SKY69120BBxxxxGL	Yes		Tray ⁴	
SKY69120BBxxxxGLR	Yes		Tape and reel ⁵	
SKY69122xxxxxxGFx <i>Contact Skyworks for ordering information</i>	–	64-lead, 9 x 9 mm wettable flank QFN	–	
SKY69120BB-BGA-EVB	Yes	–	–	Not specified

- 1. “xxxx” should be replaced with the unique customer and/or application-specific sequence number created by ClockBuilder Pro or assigned by Skyworks.
- 2. For a given unique sequence number for SKY69120, the internal flash may be blank or factory programmed as defined within ClockBuilder Pro.
- 3. Use of AccuTime requires acceptance of a separate license agreement and may be subject to restrictions regarding supported platforms and applications.
- 4. Tray quantity = 50. Contact Skyworks for details about the tray format.
- 5. Reel quantity = 1000. Contact Skyworks for details about the reel format.



*5 digits; assigned by ClockBuilder Pro for Custom OPN devices.

Revision History

Revision	Date	Description
B	July, 2026	Corrected the EVB ordering information in Table 1.
A	July, 2026	Initial release

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